Nano-Manufacturing Topical Conference
Room 2018 - Session NM+MS+IPF-MoA

Beyond CMOS: Emerging Materials and Devices

Moderator: C.M. Garner, Intel Corporation

2:00pm **NM+MS+IPF-MoA1 Technology Challenges: The Next 15 Years**, ***P. Gargini***, *C.M. Garner,* Intel Corporation **INVITED**

The semiconductor industry continues to introduce new technologies at the pace dictated by Moore's Law. The International Technology Roadmap for Semiconductors (ITRS) projects that devices can be manufactured with conventional process technology through at least 2020 even though there are significant challenges, but further extensions to extreme CMOS may require new 1D device materials. When extreme CMOS technology has reached the limits of scaling, new devices with potentially new architecture will be needed to provide continued performance improvements. For technologies beyond CMOS, research is proceeding on a number of new alternate "state" devices that would require radical materials with a silicon base. The introduction of new alternate state devices may require the introduction of new interconnect technologies and materials with nm control of properties. The challenges to driving to extreme CMOS and the options for alternate state devices will be discussed. For more information on the International Technology Roadmap for Semiconductors (ITRS): http://public.itrs.net

2:40pm **NM+MS+IPF-MoA3 Beyond CMOS - The Semiconductor Industry's Nanoelectronics Research Initiative**, *H. Coufal,* ***J. Welser***, Nanoelectronics Research Corporation **INVITED**

The tremendously powerful scaling of transistors, that has enabled Moore's Law for the past forty years, can not continue forever. Some of the reasons, such as the atomistic nature of matter, are obvious. Others are less obvious and will be briefly reviewed before some of the potential alternatives to charge based logic will be analyzed. Such an analysis had the semiconductor industry initiate a Nanoelectronics Research Initiative. The current status of this program will be reviewed.

3:20pm **NM+MS+IPF-MoA5 Nano Manufacturing Challenges**, ***M. Mayberry***, Intel **INVITED**

Not all "nano" is created equal. Nanostructures formed through tops down construction are widely used in the creation of electronics and have shipped in volume for several years. Nanomaterials that are formed through bottoms-up synthesis or self-assembly are at a comparably early stage in research and development. Combining the two approaches has considerable promise but also significant hurdles to overcome. To illustrate we will discuss three potential applications for nanomaterials and some of the challenges to successful implementation in manufacturing. First consider the problem of forming nanostructures as the size of the features begins to approach molecular dimensions. A 20nm wide structure would only consist of 10 resist molecules side by side if the resist molecule were 2nm in size. That introduces significant granularity which up to now has not been a key concern. This problem could be addressed by designing self-assembly molecules with the proper combination of sensitivity to illumination, chemical properties, and physical size. A second potential application is the formation of dielectrics between metal lines for interconnects. An ideal dielectric is an insulator, strong enough to withstand forces generated with temperature cycling, a barrier to migration of materials, and for performance reasons has a low dielectric constant. These could in principle be met through design of the right building blocks but there are complications with integration in the overall process flow. Finally nanodevices formed through self-assembly (ex. nanotubes) could in principle allow formation of very small devices but the challenge of precision formation, placement, and again integration are daunting. These challenges are not insurmountable but need to be addressed through the right research and development so that the promise of nanomaterials can be achieved.

4:00pm **NM+MS+IPF-MoA7 Metrology for Emerging Devices and Materials**, ***E. Vogel***, University of Texas at Dallas **INVITED**

Traditional scaling of the CMOS Field-Effect-Transistor (FET) has been the basis of the semiconductor industry for 30 years. The 15 year horizon of the International Technology Roadmap for Semiconductors (ITRS) is reaching a point which +IBw-challenges the most optimistic projections for the continued scaling of CMOS (for example, MOSFET channel lengths of roughly 9 nm).+IB0- As silicon CMOS technology approaches its limits, new device structures and computational paradigms will be required to replace and augment standard CMOS devices for ULSI circuits. These possible emerging technologies span the realm from transistors made from silicon nanowires to devices made from nanoscale molecules. One theme that pervades these seemingly disparate emerging technologies is that the electronic properties of these nanodevices are extremely susceptible to small perturbations in structural and material properties such as dimension, structure, roughness, and defects. The extreme sensitivity of the electronic properties of these devices to their nanoscale physical properties defines a significant need for precise metrology. This talk will provide an overview of emerging devices and materials, and, through example, an overview of the characterization needs for these technologies.

4:40pm **NM+MS+IPF-MoA9 Linking Proteins, Particles and Wires to make Functional Devices: Metrology, Materials and Properties**, ***D.A. Bonnell***, The University of Pennsylvania **INVITED**

Two issues that are critical, and projected to be limiting, to next generation device technology are metrology at the nanoscale and integration of diverse materials into manufactured devices. The first half of this talk will summarize advances in local measurements of properties and demonstrate new techniques that probe electronic structure and properties in nanostructures and molecular wires. These approaches will be illustrated on 3-terminal configurations that exhibit transistor or memory behavior. Opportunities for exciting advances on the horizon will be presented. The second half of the talk will present strategies for integrating a combination of metal and/or oxide nanoparticles, organic and/or biological molecules on oxide or polymeric substrates in device configurations. The processing approach, Ferroelectric Nano Lithography, induces variations in local electronic structure in substrates to direct assembly of nanostructures with diverse properties into complex patterns, thus overcoming one of the limitations of self assembly. The approach has been used to produce a molecular opto electronic switch.

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