Manufacturing Science and Technology
Room 2018 - Session MS-TuA

Process Integration and Modeling for Nano-scale Semiconductor Devices

Moderator: S. Shankar, Intel

2:00pm **MS-TuA1 Physics of Stress-Induced Performance Gain in Advanced MOSFET Devices***, **M.D. Giles**, S.M. Cea, T. Ghani, R. Kotlyar, P. Matagne, K. Mistry, B. Obradovic, R. Shaheed, L. Shifren, M.A. Stettler, S. Tyagi, X. Wang, C. Weber,* Intel Corporation **INVITED**

Stress-enhanced MOSFET channel mobility has become a key enabler for continued performance improvement in advanced silicon technologies. First introduced at the 90nm node,@footnote 1@ strain engineering is now being widely adopted for 65nm technologies and beyond, and gives a new degree of freedom in delivering improvements in transistor speed and power. Although the piezoresistance effect in silicon has been known for fifty years and biaxial strained silicon investigated for more than a decade, the large mobility gains possible with a dominantly uniaxial strain quickly raised the importance of fundamental understanding of device stress effects, particularly for PMOS. Developing technologies that utilize stress sources similarly requires an understanding of how materials interact to produce a channel stress distribution in the final device. This presentation will review the key physical effects at the process and device levels that contribute to stress-induced performance gain. Through the use of physically-based models of material properties, device fabrication, and device operation, the basis of stress-induced performance gains will be demonstrated and the performance differences between alternative stress configurations explained. @FootnoteText@ @footnote 1@T.Ghani, et al, IEDM Technical Digest, p. 978 (2003).

2:40pm **MS-TuA3 Defect Engineering by Short-Annealing-Time Methods for Ultrashallow Junction Formation***, E.G. Seebauer, **C.T.M. Kwok**, R. Vaidyanathan,* University of Illinois at Urbana-Champaign

Forming extremely shallow pn junctions with very low electrical resistance is becoming a large stumbling block to the continued scaling of microelectronic device performance according to Moore's Law. Manufacturing methods employ rapid thermal annealing after ion-implantation in order to increase the activation of dopants. Empirical results have shown that shorter annealing times and the millisecond time scale by flashlamp or laser methods generally improve dopant diffusion and activation behavior compared with conventional incandescent lamp annealing at 1-2 s time scales. However, an explanation for this effect has been lacking. Via mathematical modeling, we find that increasing the heating rate permits interstitial clusters with dissociation energies lower than the maximum of 3.5-3.7 eV to survive to higher temperatures. This improved survival delays the increase in Si interstitial concentrations near the top of an annealing spike, which decreases the profile spreading. In addition, we present experimental data showing that strong illumination nonthermally influences the diffusion of dopants such as arsenic and boron. Such effects can either enhance or inhibit diffusion depending upon temperature, and depend upon changes in average charge state of both lone interstitials and interstitial clusters. Illumination by incandescent lamps. flashlamps, and lasers employ light fluxes that differ by orders of magnitude, so such nonthermally stimulated diffusion can be used as an additional tool for defect engineering by suitable choice of light source.

3:00pm **MS-TuA4 Virtual Integrated Processing for IC Manufacturing***, R. Chalupa, D.G. Thakurta, L. Jiang, **H. Simka**, S. Shankar,* Intel Corporation

As each new semi-conductor technology becomes more complex, targeted simulations can lead to significant savings in process development time and cost. These are achieved by providing insights into process behavior and quantifying effects of process knobs on performance. Due to the complexity of physical phenomena involved, each process simulator may itself consist of multiple (possibly linked) modules each aimed at different length and/or time scales or different operating regimes. In Electroplating (EP) process for backend (BE) interconnect formation for example, wafer-scale events are often governed by electrostatic potential fields where current distributions are estimated based on local conductivities. Feature scale (less than 1-100 microns) events are often governed by transport-reaction events in shape-changing domains. Availability of accurate simulation tools allows investigations of dependence of a BE step to those preceding it, and its effects on subsequent steps. This "virtual processing" provides information useful in investigation of process input requirements, performance limits, scaling, and other integration issues. One example of process interaction modeling is in EP and CMP areas where models were used to explore film planarity for various realistic chip layouts. Our integrated BE simulator provides an effective way to explore solutions not readily accessible in experiments due to cost and time constraints. These model components have played key roles in developing advanced BE modules, including alternative deposition and planarization processes for 90 nm technology.

3:20pm **MS-TuA5 Semiconductor Materials Challenges and Opportunities for Energy Efficient Power Conversion Technologies***, **M.A. Briere**,* International Rectifier, US **INVITED**

There exists great opportunities to signifcantly impact the world wide energy consumption through the development and implementation of highly efficient power management and conversion technologies. Nearly 25 % of the worlds consumption of oil can be saved by the year 2025 through improvements in electronics used in lighting, transportation, motor control for appliances and power supplies for electronic devices. In order to achieve these results, implementation must be widespread. This requires that the solutions be available without additional system costs. The challenge of providing energy efficiency for free can be met through innovative system architecures and improved semiconductor devices. Significant advances in device and system performance can be achieved through the use of new semiconducting materials. A review of the relationship of device performance and semiconductor material properties for Si, SiC, Diamond and GaN will be presented, as well as a comparison of performance for device structures of diodes, FETs and IGBTs. Material growth techniques such as MBE and MOCVD will be compared for these purposes. A summary of the state of the art in the material properties and device characteristics for these alternatives to the present Si offerings will be made. Critera for large scale manufacturing using these materials and growth techniques will be presented.

4:00pm **MS-TuA7 Electrochemical Planarization of Copper Surfaces with Sub-Micron Features***, **R. Chalupa**, A.N. Andryushchenko, J. Han, T. Ghosh, S. Shankar, P. Fischer,* Intel Corporation

Electrochemical planarization (ECP) of copper surfaces in a phosphoric acid-based electrolyte solution is discussed. A first-principles, quantum-chemistry modeling work is presented that further validates the water-facilitated (and water rate limited) chemistry model for copper oxidation at the anode. This model has been previously deduced by other researchers@footnote 1,2,3@ based on electrochemical experiments. Resulting water-limited model is validated against experimental data and applied to study the planarization behavior of a set of surface features. Aspect ratios and dimensions of these features were chosen to represent realistic (non-idealized, low aspect ratio structures) post Damascene electroplate surface topography. Results are presented in a form of remaining feature amplitude versus mean copper thickness removed@footnote 4@ - allowing at-a-glance evaluation of the process against desired targets. The dominant effects of the mass transport boundary layer (BL) thickness on this planarization efficiency are discussed as are the challenges seen at typical flow conditions in ECP systems. Impact of changing the BL thickness and the requisite modulation of flow conditions analysis is included. Insights into practical challenges associated with BL build-up transient and associated surface roughening are summarized@footnote 5@. Challenges of applying ECP as a straightforward substitute to the robust CMP process are significant. Practical modifications to upstream process flow to enable ECP would include optimized electroplating process or a CMP pre-processing step. @FootnoteText@ @footnote 1@R. Vidal, A. C. West, J. Electrochem. Soc., 142, 2682 (1995). @footnote 2@R. Vidal, A. C. West, J. Electrochem. Soc., 142, 2689 (1995). @footnote 3@B. Du, I.I.Suni, J. Appl. Electrochem., 34, 1215 (2004). @footnote 4@A. C. West, I. Shao, H. Deligianni, J. Electrochem. Soc., 152, C652 (2005). @footnote 5@D. Padhi, J. Yahalom, S. Gandikota, G. Dixit, J. Electrochem. Soc., 150, G10 (2003).

4:20pm **MS-TuA8 Large-Scaled Line Plasma Production by Evanescent Microwave in a Narrow Rectangular Waveguide***, **E. Abdel Fattah**, S. Fijii,* ADTEC Plasma Technology Co. LTD, Japan*; H. Shindo,* Tokai University, Japan

Long line-shaped plasmas are attractive for use in material processing in manufacturing industries, such as .at panel displays (FPDs) and surface modification of large- area thin films. Several types of plasmas have been developed to meet those needs. In this study, long line-shaped microwave plasma was generated employing a narrow rectangular waveguide. The wavelength of a microwave in a waveguide increases in accordance with

the width of the waveguide. The objective of this work is to provide a method of large-scaled line plasma production by employing narrow width rectangular waveguide. A narrow and flattened rectangular waveguide was prepared with the internal dimensions of 1000mm length, 59 to 62mm width and 5mm height. The waveguide was connected to a TE10 mode rectangular waveguide (WST-AD standard). In this narrowed waveguide, the microwave is cutoff, but the evanescent wave is employed to produce the plasma. Two types of line-shaped plasmas was generated; one being a cavity type and the other a slit type. The cavity type line-shaped plasma has a quartz tube in the waveguide as a discharge tube and helium gas as well as argon was supplied into the quartz tube through orifices of the waveguide. The slit type line-shaped plasma has a slit on its side. A quartz tube as a discharge tube was set beside the slit and helium gas as well as argon gas is supplied into it. Electric field intensity and optical emission intensity were then measured. Uniformity of line-shaped plasmas was improved by reducing the width of the waveguide and the microwave power in both types of line-shaped plasmas. In particular, the uniform line plasma could be produced as long as 1000mm in length at 100 Torr pressure. The uniformity was confirmed by both the measurements of electric field and optical emission intensity.

4:40pm **MS-TuA9 Innovative Studies for Ultra High Aspect Ratio Deep Trench Etch***, **S. Pamarthy**, F. Ameri, D. Gutierrez, D. Scanlan, F. Schaeftlein,* Applied Materials

A key challenge that DRAM manufacturers are facing today is achieving very high aspect ratios in deep trench etch. Future DRAM technology shrinks require development of hardware and process solutions to etch deep trench features at aspect ratios >80:1, for which there is no known available solution today. This paper describes how this key technical challenge can be overcome to implement a manufacturing solution to meet the aspect ratio requirements for DRAM DT technology needs of 65nm and beyond. The entire development path is traced, from initial plasma generation and gas flow modeling studies, early concept experiments involving plasma characterization, and process condition explorations and eventually to a final reactor design, including the innovation of multiple uniformity tuning knobs. The paper also focuses on studies done with each of the following hardware/process tests: Gas Flow Ratio Control (FRC), Dual Zone Coolant Ceramic ESC and Independent Gas Injection (IGI) independently and the impact these tests have on some critical aspects of deep trench etch such as center to edge trench depth non-uniformity, center to edge bottom CD uniformity, mask selectivity, Top CD widening, and mask remaining uniformity across the wafer. The study shows that some of the limitations of the current production chambers can be improved with these potential features. The paper also talks about how a future reactor can potentially be the only chamber of its kind with a clear capability to tune the capacitance of each DRAM cell across the wafer using these innovative features. For selectivity improvements, studies with new silicon source gases such as SiF_4 and $SiCl_4$ as additional sources for re-deposition during the etch process are discussed.

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