Electronic Materials and Processing
Room 2003 - Session EM2-ThA

Electronic Properties of High-k Dielectrics, Ferroelectrics, and Their Interfaces

Moderator: R.M. Wallace, University of Texas at Dallas

2:00pm **EM2-ThA1 Ab Initio Study of High-k Gate Stack**, *J. Ha, B. Magyari-Kope, P.C. McIntyre,* Stanford University; ***K. Cho,*** UT Dallas **INVITED**

At nanometer scale, materials behave differently from their bulk properties. Material properties become a function of their size and shape at 1-100 nm scale due to strong quantum mechanical effects and surface effects. In this talk, we will apply quantum simulations to study high-k gate stack materials. We will focus the main discussion on the modeling study of high-k gate stack system with emphasis on two interface problems: silicon/high-k oxide and high-k oxide/metal gate electrode interfaces. For the silicon/high-k oxide interface, we examine the effects of interlayer SiO2 between silicon substrate and high-k oxide (HfO2 or ZrO2). The driving force for SiO2 formation at the silicon/high-k oxide interface is identified and the correlation between the interface atomic structure and the band offsets is elucidated. Furthermore, the internal SiO2-HfO2 interface is investigated to understand the source of fixed charge problems of high-k oxides. Our modeling study has identified the source of fixed charges, and we have proposed a practical solution to passivate the fixed charge source at the interface. For the high-k oxide/metal gate interface, we have studied the work function of candidate metal gate electrodes and identified the key mechanisms which control the work function of different metals at the interface. Our study has shown that the interface work function is determine by 1-3 monolayers of metal at the interface and that the work function control requires a direct control of atomic structures at the interface rather than the overall structure of electrode materials.

2:40pm **EM2-ThA3 Material and Electrical Properties of HfRuN Gate Electrodes on HfO@sub 2@**, ***M. Sawkar Mathur,*** *J.P. Chang,* University of California, Los Angeles

Many alternative gate dielectric candidates for future generation MOSFET devices, including Hf based dielectrics, will require the use of a metal gate, because of the instability issues, sheet resistance, gate depletion, and dopant penetration experienced with polysilicon gates. Hf based gate electrode materials are promising candidates because they are likely to reduce charge transfer and subsequent dipole formation at the interface as a result of the homo-nuclear bonds that form between the Hf in the metal gate and the Hf in the gate dielectric. This paper discusses the material and electrical properties of Hf-Ru and Hf-Ru-N gate electrodes deposited atop HfO@sub 2@. Four compositions of HfRu were synthesized with varying amounts of N (0 - 15 at.%), and their material characteristics before and after annealing, such as composition, interface bonding, and crystalline phases were determined by X-ray photoemission spectroscopy (XPS), Rutherford backscattering (RBS), and X-ray diffraction (XRD). Capacitance-voltage (C-V) and current density-voltage (J-V) characteristics of fabricated metal-oxide-semiconductor (MOS) capacitors are used to determine the effective work functions (EWFs), the barrier heights, and the leakage current density across the metal gate/HfO@sub 2@ interface. Pure Hf and pure Ru gate electrodes deposited on HfO@sub 2@ exhibited EWFs of 4.1 eV and 5.5 eV, respectively, which correspond well with what has been reported in literature.@footnote 1,2@ HfRu alloys with EWFs of 4.8eV and 5.2 eV have been achieved, and N incorporation was found to have a modest effect on the attained EWFs. Detailed analyses of EWFs as a function of alloy composition, microstructure, and interfacial bonding will be presented to determine the optimal composition for n-MOSFET devices and p-MOSFET devices. @FootnoteText@ @super 1@ P. Majhi, et. al., 2005 IEEE VLSI-TSA (2005).@super 2@ M. Tapajna, et. al., Materials Science in Semiconductor Processing 7, (2004).

3:00pm **EM2-ThA4 Spectroscopic Detection of Electronically Active Defects in Nanocrystalline Ti/Zr/Hf Elemental Oxides**, *G. Lucovsky, L.B. Fleming, M.D. Ulrich,* ***H. Seo,*** *N.A. Stoute,* NC State University; *J. Luning,* Stanford Synchrotron Radiation Lab

The performance and reliability of advanced Si field effect transistors (FETs) with high-k transition metal gate dielectrics are limited by intrinsic bonding defects within the nanocrystalline oxides, and at internal device interfaces with i) Si/other semiconductor substrates, and ii) gate metals. This paper employs (a) several spectroscopic approaches: i) near-edge soft-x-ray absorption spectroscopy (NESXAS), ii) soft x-ray photoelectron spectroscopy (SXPS), iii) ultra-violet photoelectron spectroscopy (UPS), and iv) visible and vacuum ultra-violet spectroscopic ellipsometry (VUV SE), and (b) ab initio molecular orbital (MO) theory to study band edge defects. Occupied O-vacancy defect states have been identified at Ti/Zr/HfO@sub 2@ valence band edges by SXPS and UPS. These states have different crystal field splittings for Ti, and Zr and Hf oxides, as expected from the respective 6-fold, and 8-fold coordinations to O. Additionally, occupied defect states display Jahn-Teller term-splittings that remove their respective d-state degeneracies. Transitions from the J-T split ground states to empty defect states below the respective conduction band edges have been identified in O K@sub 1@ NESXAS spectra, epsilon 2 spectra obtained from analysis of VUV SE response functions, and in photoconductivity. Defect densities are ~1-3x10@super -13@ cm@super -2@, consistent with vacancies being clustered along grain boundaries of nanocrystalline oxides. In contrast, these types of defects are not observed spectroscopically in non-crystalline Zr/Hf Si oxynitride alloys, or in ultra thin HfO@sub 2@ dielectrics that have been exposed to post deposition anneals (PDAs) in different nitrogen ambients.

3:20pm **EM2-ThA5 Combining Ferroelectric Oxides and Semiconductors for Smart Transistors**, ***J. Singh,*** University of Michigan, usa **INVITED**

Semiconductors have been exploited for decades in creating intelligent devices. However, oxides and other insulators have at most provided passive roles as insulators or passivation layers. Recent work has been showing that it is possible to grow reasonable quality oxide-semiconductor interfaces. Is it possible to have oxide-semiconductor heterostrucutres where the best of semiconductors and the best of oxides (polar charge, tailorable polarization, large bandgap, tailorable dielectric response etc.) can be exploited? There are a large number of potential material systems that have polar character which are not (yet) considered to be relevant to semiconductor technology. These include ferroelectrics, pyroelectrics and piezoelectric materials where polar charges as high as 1 electron per surface atom can be present.For these structures to make an impact a number of parameters need to be evaluated. These include: (i) band lineup; (ii) polarization vs. thickness; (iii) dielectric response vs. thickness; (iv) and most importantly defect structures. In absence of all this knowledge it is still possible to examine the potential of new heterostructures that exploit polar materials. Theoretical studies can provide estimates of the level of perfection needed to make new devices possible. Polarization differences at interfaces can be used to create very large band bending which in turn can be used to induce electron (hole) gas, create tunnel junctions, cause lateral as well as vertical band engineering. Most interestingly these structures can result in smart FETs which have high transconductance and respond not only to gate bias but to pressure, temperature variations, etc. At this point in time these structures can serve as test cases to examine the potential of oxide-semiconductor structures and to see if the interfaces can reach the needed quality for functional devices.

4:00pm **EM2-ThA7 Theoretical Analysis of the Interface between Zr(Hf)O@sub 2@ and Ge(100) for Ge-based MOSFET Devices**, ***T.J. Grassman,*** *S.R. Bishop, A.C. Kummel,* University of California, San Diego

In recent years there have been many attempts at the fabrication of high-quality Ge-based MOSFETs. One of the most successful dielectric materials used in these studies is ZrO@sub 2@, producing some of the best Ge-based MOS devices to date; HfO@sub 2@ has also found a fair amount of use in the field, with varying results. In order to better understand these MOS systems, and particularly the often-problematic SC/oxide interface, a systematic density functional theory study of the Zr(Hf)O@sub 2@/Ge(100) interfaces has been undertaken. Multiple initial first-layer bonding configurations of ZrO@sub 2@ and HfO@sub 2@ on Ge(100)-2x1/4x2 have been simulated in order to elucidate, through adsorption energy comparisons and comparison with experiments, what the interfacial configuration between the semiconductor and oxide actually is. These sites were also modeled for electronic structure in order to help explain or clarify the experimental results. It has been found that ZrO@sub 2@ bonds to the Ge(100) surface very strongly in both Zr- and O-end down configurations, with the Zr-end down geometry the strongest. It is also seen from the electronic structure calculations that the Ge-Zr bonds are covalent rather than metallic, and neither Zr- nor O-end down bonding configurations result in an increase in near-Fermi level DOS. Such results are consistent with the experimental findings that ZrO@sub 2@ is a good gate dielectric material for Ge(100). In addition, the calculations indicate that H-passivation of dangling bonds at the ZrO@sub 2@/Ge(100) interface, and potentially within the oxide itself, may be an effective method to improve MOS device properties. However, while H-passivation

of dangling bonds on both Zr and O atoms produces a considerable reduction of near-Fermi level DOS, only the passivation of the O atoms is thermodynamically stable enough to be achievable in device processing conditions. All of these same calculations are currently being performed on HfO@sub 2@.

4:20pm **EM2-ThA8 Sub-1 nm Equivalent Oxide Thickness Zirconium Doped Hafnium Oxide High-k Gate Dielectrics**, ***J. Yan***, *C.-H. Lin, A. Birge, J. Lu, Y. Kuo,* Texas A&M University

Implementation of high-k gate dielectrics for the continuous scale-down of MOSFETs requires the equivalent oxide thickness (EOT) be less than 1 nm.@footnote 1@ In order to achieve this kind of ultra-thin film with high dielectric quality, the gate dielectric deposition and post-deposition annealing (PDA) processes need to be carefuly studied. Previously, we reported that sub-2nm EOT Zr-doped HfO2 could be prepared by the reactive co-sputtering method.@footnote 2@ In this work, we report new results on preparing the ultra-thin, e.g., EOT as low as 0.89 nm, Zr-doped HfOx dielectric films by sputtering from a composite target. Effects of PDA conditions, such as temperature and gas atmosphere, on material and electrical properties were investigated. The interface layer formation mechanism, which is critical to the low EOT, low interface states density, and low charge trapping density, was studied. The resulting films have Dit E11 to E12 cm-2eV-1, hysteresis less than 4mV, and leakage current 4 orders of magnitude lower than that of SiO2. The interface and bulk film material properties were characterized with the angle-resolved x-ray photoelectron spectroscopy and AFM. @FootnoteText@ @footnote 1@ ITRS, SIA (2005).@footnote 2@ Y. Kuo, et al., ECS Proc. High Dielectric Constant Gate Stack III, in press (2005).

4:40pm **EM2-ThA9 Evaluation of Various Ru-insulator-Ru Capacitors with CVD-Ru Thin Films for Both Top and Bottom Electrodes**, ***B.S. Kim***, *C.S. Hwang, H.J. Kim,* Seoul National University, Korea*; S.Y. Kang, J.Y. Kim, K.H. Lee, H.J. Lim, C.Y. Yoo, S.T. Kim,* Samsung Electronics Co., Ltd., Korea

Ruthenium has been considered as one of the most promising materials for capacitor electrodes in gigabit-scale DRAM due to its low electrical resistivity and good dry etching property in addition to the capability of conductive oxide formation. To deposit the Ru thin films into a typical concave type storage node with a high aspect ratio, the development of metalorganic chemical vapor deposition (MOCVD) process, which provides an excellent conformality, is necessarily required. However, there are few reports about the structural and electrical characterization of Ru-insulator-Ru (RIR) capacitors, of which both the top and bottom Ru films were grown by MOCVD. Therefore, in this study, we fabricated the RIR capacitors with CVD-Ru and various dielectric materials and evaluated their properties by structural and electrical analysis. The Ru thin films were deposited by hot-wall MOCVD using liquid precursor of (2,4-Demethylpentadienyl)(Ethylcyclopentadienyl)ruthenium (DER) to fabricate the top and bottom electrodes. All the dielectric thin films such as ZrO@sub 2@, TiO@sub 2@ and SrTiO@sub 3@ were formed by atomic layer deposition (ALD) method. The electrical properties of the fabricated RIR capacitors were evaluated by the capacitance-voltage measurement combined with the current-voltage measurement. The thermal stability of as-grown capacitors was also tested under several annealing ambient and temperatures. The structural analysis to elucidate the relation with electrical properties was conducted by the x-ray diffraction (XRD), atomic force microscopy (AFM), scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

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