Electronic Materials and Processing
Room 2003 - Session EM-TuA

Materials for Power Electronics

Moderator: C. Eddy, Naval Research Laboratory

2:00pm **EM-TuA1 Processing of High-k Oxide Thin Films for High Energy Density Capacitors**, ***G. Sethi,*** The Pennsylvania State University, US*; M.T. Lanagan, M.W. Horn,* The Pennsylvania State University

Oxide thin films with a focus on zirconia on silicon and glass substrates were prepared with the aim of optimizing the thin film processing parameters to produce 0% crystallanity (amorphous) films. Reduction in the crystallanity will improve dielectric breakdown strength, dielectric losses and the energy density. Reactive magnetron sputtering with a metallic target (76mm) is used for producing smooth, stoichiometric and dense films with high deposition rate. It is hypothesized that crystallanity (quantified from XRD) of a film can be reduced either by high bombardment to inhibit the crystallization or by low bombardment to limit ion mobility and the crystallization. High bombardment was achieved by using a pulsed-dc deposition process at low pressure (<1.3Pa) and high power (400W). The crystallanity reduces from 70% to 40% with the high bombardment, in the 'poisoned' sputtering mode. With the transition into 'elemental' sputtering mode, the deposition rate increases (20Å/s) crystallanity reduces (22%) and films become smooth. However EDS and SEM analysis revealed that the films are highly oxygen deficient (4 wt.% O@sub 2@) and defect-full with high compressive stresses. Increasing the film oxygen content during sputtering to near-stoichiometry does not reduce crystallanity and lowers the deposition rate (1.6 Å/s). Low bombardment was achieved by using RF sputtering at high pressures (13.3Pa) and low power (<200W). As imagined, the crystallanity in the film reduces with bombardment to 5%, but the deposition rate is substantially lowered (0.3 Å/s) with maximum 100nm thickness. The films are stoichiometric and near-stress free (-200MPa). The substrate temperature rise to as low as 70°C during the sputtering is responsible for this small crystallization. The temperature rise and hence crystallanity will be reduced by using liquid Nitrogen cooled substrate. Finally, the correlation between crystal structure and dielectric properties will be presented.

2:20pm **EM-TuA2 Growth of Epitaxial @gamma@-Al@sub 2@O@sub 3@ Films on 4H-SiC**, ***C.M. Tanner,*** University of California, Los Angeles*; J. Lu, H.-O. Blom,* Uppsala University, Sweden*; J.P. Chang,* University of California, Los Angeles

The development of epitaxial high-k gate dielectrics has the potential to improve the performance of SiC power MOSFETs by improving the interface and enabling operation at a higher electric field. Al@sub 2@O@sub 3@ (k = 10) is a promising candidate due to its large bandgap and demonstrated stability in several crystalline phases. Al@sub 2@O@sub 3@ thin films were grown on chemically mechanically polished n-type 4H-SiC (0001) by atomic layer deposition (ALD) at 200°C using trimethylaluminum and water vapor. The films were stoichiometric with low carbon incorporation as evaluated by in-situ X-ray photoelectron spectroscopy (XPS). The as-deposited Al@sub 2@O@sub 3@ films were amorphous as determined by in-situ reflection high-energy electron diffraction (RHEED). Upon annealing in N@sub 2@ at 1100°C, the film crystallized to the @gamma@-Al@sub 2@O@sub 3@ phase as observed by RHEED, high-resolution transmission electron microscopy (HRTEM) and X-ray diffraction (XRD). Based on the Fourier transform of the HRTEM image, an epitaxial relationship of @gamma@-Al@sub 2@O@sub 3@ (111) on 4H-SiC (0001) was observed in which @gamma@-Al@sub 2@O@sub 3@ (-110) was oriented with 4H-SiC (-12-10). This orientation was further confirmed by XRD analysis in which only the @gamma@-Al@sub 2@O@sub 3@ (111) and (222) peaks were observed. An abrupt interface of both amorphous and crystalline Al@sub 2@O@sub 3@ with 4H-SiC was determined by HRTEM. Capacitance-voltage (C-V) and current-voltage (I-V) measurements of 4H-SiC MOS capacitors fabricated with 200 Å Al@sub 2@O@sub 3@ dielectric films were performed to compare the dielectric constant, fixed charge, density of interface states, and breakdown properties of epitaxial @gamma@-Al@sub 2@O@sub 3@ films with respect to those of amorphous Al@sub 2@O@sub 3@ as well as state-of-the-art thermal silicon dioxides.

2:40pm **EM-TuA3 SiC/SiO@sub2@ Interface and Near Interface Traps in SiC Based MOSFETs**, ***P.M. Lenahan,*** Penn State University, US*; M.S. Dautrich,* Penn State University*; A.J. Lelis,* US Army Research Labs **INVITED**

Considerable progress has been made in the development of metal oxide semiconductor (MOS) field effect transistors (MOSFETs) based on SiC/SiO@sub2@ structures.@footnote 1@ The most promising devices utilize the 4H SiC polytype. Although, SiC/SiO@sub2@ MOS technology holds great promise in high-power and high-temperature applications, at the present time, SiC based devices exhibit mediocre performance. The device performance is limited, in large part, by trapping centers at and very near the SiC/SiO@sub2@ interface. This presentation will deal with electron spin resonance (ESR) and conventional electronic measurements of SiC MOS devices which provide some understanding of the physical and chemical nature of these performance limiting traps.@footnote 2@ Most of the ESR results have been obtained through very sensitive electrically detected magnetic resonance (EDMR) measurements on fully processed transistors via spin dependent recombination (SDR). These measurements clearly demonstrate fundamental differences between the physical nature of the defects which limit the performance of conventional Si/SiO@sub2@ based MOSFETs and current day SiC- based MOSFETs. In Si/SiO@sub2@ MOSFETs, for example, most of the observed "interface traps" are located precisely at the semiconductor/insulator boundary. In SiC-base devices this is not the case. The magnetic resonance results clearly demonstrate the presence of fairly high densities of deep level centers which are intrinsic in nature. These defects extend below the SiC/SiO@sub2@ interface into the SiC. We argue that the dominating interface/near interface defect in 4H SiC transistors involves a vacancy center. The concentration and physical distribution of this center depends strongly upon processing variables. @FootnoteText@ @footnote 1@ J.C. Zolper and M. Skowronski, MRS Bulletin 30.4 (Apr 2005) p273-275@footnote 2@ M.S. Dautrich, P.M. Lenahan, and A.J. Lelis: To Be Published, Mater. Sci. Forum 2006.

3:20pm **EM-TuA5 Diffusion Barriers for High-Temperature Reliability of SiC Junction Field Effect Transistors**, ***S.E. Mohney,*** *C.M. Eichfeld, B.Z. Liu,* The Pennsylvania State University*; A.V. Adedeji, J.R. Williams,* Auburn University*; S.H. Wang, A. Owen,* The Pennsylvania State University*; S.-H. Ryu, S. Krishnaswami,* Cree

Tantalum-bearing diffusion barriers show considerable promise for the protection of contacts to SiC in air at high temperatures. Such barriers include Ta-Si-N, Ta-Si, Ta-Ru-N, and Ta-Ru. In this presentation, we report the high-temperature reliability of metallization stacks aged in air at 350°C for 5,000 h or longer. For many of the diffusion barrier compositions, the ohmic contacts beneath them maintain low specific contact resistances in the mid-10@super -5@ Ohm cm@super 2@ range as well as strong adhesion between the layers. We have also used Auger electron depth profiling to help us understand why some metallization stacks survive and others fail. Contrary to our original expectations, the addition of N can be detrimental to the Ta-Ru barriers because N is lost to the environment during aging, hastening oxidation. The most promising barriers have been successfully integrated into SiC JFETs, and the devices are now being aged at 350°C in TO-258 open cavity packages and periodically tested.

3:40pm **EM-TuA6 Boride-based Schottky Contacts to p-GaN**, ***L.F. Voss,*** *L. Stafford, J.-J. Chen, S.J. Pearton, F. Ren,* University of Florida

An important aspect of the improvement of GaN-based devices for high temperature/high power electronic devices is the development of more reliable and thermally stable Ohmic and Schottky contacts on both n-type and p-type GaN. While the most common Schottky contacts to GaN are based on Ni/Au and Pt/Au, there is an increasing interest for metallization schemes with higher melting temperatures and better thermodynamic stability. In this work, we examine the potential of boride-based Schottky contacts to Mg-doped GaN layers grown by Metal Organic Chemical Vapor Deposition. This investigation is realized using current-voltage (I-V), x-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy measurements. It is found that W2B and W2B5-based Schottky diodes exhibit an excellent thermal stability upon annealing up to ~500Â°C. At higher annealing temperatures, the diodes show deterioration in rectifying behavior due to the onset of metallurgical reactions with GaN. On the other hand, the temperature dependence of the I-V characteristics indicates that tunneling through a Schottky barrier (thermionic field emission) is the dominant transport mechanism of the diodes under forward bias conditions. The characteristic energy related to the tunneling probability is however higher (E@sub0@~80 meV) than that expected from the concentration of Mg acceptors alone (E@sub0@~50 meV). This is found to correlate with the presence of acceptor-like defects in the p-GaN

surface vicinity that enhance the tunneling probability (defect-assisted tunneling). This high concentration of defects is also believed to explain the unexpectedly high barrier heights extracted from the tunneling model (~4.5 eV) which is higher than that deduced from the heterojunction band offsets obtained from XPS measurements. The possible mechanisms for reverse-bias current are also discussed.

4:00pm **EM-TuA7 Materials Issues in Power Electronics: Silicon to Silicon Carbide**, ***K. Hobart***, Naval Research Laboratory **INVITED**

The continuous advance of silicon power electronics has been made possible due to a well established materials foundation that has allowed power switching transistors to incorporate sophisticated device concepts, e.g. superjunction, junction termination extension, etc. The push to very high voltage silicon devices is primarily limited by its modest critical electric field when compared to materials such as silicon carbide and gallium nitride which have ~10x better theoretical breakdown performance. Si may still benefit from exploratory technologies to achieve higher voltage operation. However, the trade-off between switching speed, blocking voltage, and forward voltage drop cannot be fundamentally overcome for bipolar devices as it has been for unipolar devices with the superjunction, which has pushed DMOSFETs to surprisingly new performance levels. Silicon carbide, an indirect semiconductor, is an excellent candidate for wide bandgap minority carrier device technologies with high blocking voltages and low forward voltage drop. Some limitations to ultimate performance are high quality thick epitaxial layers and surface electric field termination. These two issues have been the focus of intense research recently and progress has been steady. Stable 10kV P-i-N diodes have been evaluated in our lab at temperatures above 200°C, however more work is needed to see sufficiently long working lifetimes in both forward and reverse operation. Specific challenges lie in reducing the basal plane dislocation density within the thick epitaxial layers, which lead to stacking fault generation and reduced current flow, and finding alternative surface passivation layers to handle the high surface electric fields and high temperatures typical of SiC devices. For many power electronics applications in the 10kV or less regime, SiC unipolar devices are preferred over bipolar minority carrier devices primarily due to improved switching speed. Unipolar devices have recently demonstrated extraordinary switching performance and lower voltage (1.2kV) SiC Schottky barrier diodes are now commercial products. SiC DMOSFETs with blocking voltages over 10kV have been demonstrated with a specific on-resistance ~0.2 ohm-cm@super 2@. Common material challenges exist with bipolar devices in the area of electric field termination and high temperature, high electric field surface passivation. Additionally, reliable MOSFETs demand extremely high quality gate dielectrics with very low interface state density and low fixed charge. The wide bandgap of SiC places additional burden on the gate and passivation dielectrics against charge injection from the semiconductor. Material challenges in Si and SiC power devices will be reviewed with emphasis on the most recent results that show a trend of performance to much higher voltage operation. Beyond high voltage devices, characteristics necessary for reliable large area, high current power devices will be discussed.

4:40pm **EM-TuA9 Optimized RIE Process for High Performance SiC BJTs**, ***A.B. Goulakov***, *F. Zhao, I. Peres-Wurfl,* Microsemi Inc.*; B. Van Zeghbroeck,* Colorado University*; J. Torvik,* Microsemi Inc.

SiC high-power RF devices are slated to replace Si devices to enhance the system performance and to reduce overall cost. Because of mechanical stability and the lack of dopant diffusion in SiC at normal temperatures, a common SiC RF BJT fabrication process includes homoepitaxial growth of differently doped layers followed by several dry etching steps. In this paper we will focus on two critical etch processes and two inch SiC wafer fabrication. The first process is a deep (> 5 micron) etch for electrical isolation between BJT fingers. The second process is a shallow (< 0.3 micron) precise etch down to the base layer. Due to thin 100 -150 nm base layer in the vertical n-p-n structure, a non uniform RIE process is a "yield killer". In this paper, we present details on a novel etching process for SiC RF BJTs fabrication process by combining optimized RIE etch, conductivity measurements, and oxidation. RIE etch parameters were optimized resulting in smooth etched surfaces and sufficient etch depth uniformity of < 8% for shallow etch, and < 2% for deep etch across two inch SiC wafers. Our etching process provides a precision (± 10nm) emitter etch to the emitter-base junction, even when the actual epitaxial layer thicknesses are different than expected. This method was also used to measure the emitter layer thickness and resistivity uniformity across different wafers and lots, and data will be presented. Furthermore, precise etching of the emitter epitaxial layer results in improved RF performance of the BJT by optimizing the base sheet resistance. Using this RIE process, we successfully fabricated several lots of 50W UHF SiC BJTs with a dc probe yield > 90%.

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