Electronic Materials and Processing
Room 3rd Floor Lobby - Session EM-ThP

Electronic Materials and Processing Poster Session

EM-ThP2 Effect of the Oxygen Partial Pressure on the Photoluminescence Emission from Heterostructures SiO2/Si/SIO2 Growth by RF Reactive Sputter Magnetron, ***E. Mota-Pineda***, *M. Melendez-Lira, J. Falconi-Guajardo,* Cinvestav-IPN, Mexico*; J. Jesus-Araiza,* University of Zacatecas, Mexico*; W. Calleja-Arriaga,* NAOE, Mexico

We prepared heteroestructures SiO2/Si/SiO2 by sputter reactive magnetron deposition on Si (100) and corning glass substrates at 400Â°C. We employed a polycrystalline Si target with Ar and O2 as working gases. We investigate the effect of the partial pressure of oxygen and the thickness of the Si interlayer on the electronic properties of the heterostructure. Crystallographic properties were studied by X-ray diffraction and chemical composition was determinate by EDX. The electronic properties were determined by transmission and Raman spectroscopies at room temperature. The Raman spectrum of the as-deposited samples has two broad features due to scattering by TO and LA phonons in a-Si respectively. UV-Vis transmission spectroscopy shows that the absorption edge shifts as function of the thickness of Si interlayer. The FTIR absorption spectra of as-deposited films show absorption peaks associated with vibration modes of the SiO2 and Si-Si. The thicknesses of the films were determinate by scanning electron microscopy and vary between 500 and 600nm. We observed the superficial topography of the material through AFM. Transmission electron-microscope micrography confirms the growth of the SiO2/Si/SiO2 heterostructure and the electron diffraction pattern shows the presence of nanocrystalline phases. A broad lumininescent band (around 1.7 eV) appears by effect of the Si interlayer and its intensity increases with the Si layer thickness. The results are discussed in terms of a model of quantum confinement of Si embedded in a SiO2 matrix. The effect of rapid thermal annealing under Ar and O2 atmospheres on the photoluminescent characteristics are also discussed.

EM-ThP3 Light Emission from SiO@sub x@ Films Deposited on Silicon by Laser Ablation*, *J.G. Ramirez-Mora,* U. Autonoma de Zacatecas, Mexico*;* ***M. Melendez-Lira,*** Fisica, Cinvestav-IPN, Mexico*; J.J. Araiza-Ibarra,* U. Autonoma de Zacatecas, Mexico*; C. Falcony,* Fisica, Cinvestav-IPN, Mexico

We have produced SiO@sub x@ films by laser ablation employing a silicon target under a O@sub 2@ atmosphere. Films were prepared employing the 1064 nm and 532 nm wavelength obtained from a Nd:Yag pulsed laser. Power intensity applied to the target was modulated by focusing the laser beam. Film thickness was controlled by the number of pulses applied on the silicon target. Chemical composition obtained by EDX shows that films produced present an excess of silicon. This was corroborated from results of the refraction index value obtained by ellipsometry measurements. Raman spectroscopy results show the presence of amorphous silicon regions. Room temperature photoluminescence measurements were carried out with 632.8 nm and 457.9 nm wavelengths from a HeNe and Ar@super +@ lasers. A broad emission was detected under the HeNe excitation, a stronger intensity was obtained from the thinner films. For thicker films narrow peaks are developed on the broad emission. When luminescence is excited with the Ar@super +@ laser a narrow peak around 580 nm is observed. Surface topography obtained by AFM shows the presence of square columm-like features. We will present transmission electron micrographies. Results are discuss in terms of the presence of silicon clusters embedded within a SiO@sub 2@ matrix. @FootnoteText@ *work partially funded by CONACyT-Mexico.

EM-ThP4 UV-Detecting Top-Gate ZnO-TFTs with Polymer Dielectric for Optical Inverter Application, ***K.M. Lee***, *J.-M. Choi,* Yonsei University, Korea*; J.H. Park, E. Kim,* Hongik University, Korea*; C.S. Kim,* Yonsei University, Korea*; H.K. Baik,* Yonsei University, Korea, South Korea*; S. Im,* Yonsei University, Korea

Very recently ZnO thin-film transistors (TFTs) have attracted much interest from researchers and engineers because they have potentials to realize transparent electronics. However, most of the reported devices were based on bottom-gate structures. We have successfully fabricated ZnO-based TFTs of a top-gate structure with organic polymer dielectric and also realized optical inverters by using their UV-detecting properties. ZnO channel layers were patterned by rf magnetron sputtering on glass substrate, and then Al source/drain electrodes were deposited by thermal evaporation. PVP dielectric layers were subsequently deposited by spin casting. Finally, semi-transparent conducting NiOx gate windows were patterned on the PVP layers. In spite of the relatively lower mobilities (~0.01 cm@super 2@/Vs) than those of other bottom-gate ZnO TFTs with inorganic dielectric layers, our ZnO-TFT with polymer dielectric has a good UV responsity (at wavelength ~364 nm) as a photo-detector and showed a fast response for optical gating (including detecting and inverting actions). For these demonstrations of optical inverters, we set up an appropriate array of photo TFTs and load registers. Furthermore, we attempt to enhance the mobility and to lower the operating voltage of our top gate ZnO-TFTs by adopting a hybrid gate dielectric of high-k inorganic/organic (PVP) sandwich structure. More and advanced details will be discussed in the meeting.

EM-ThP5 Etching Characteristics of ZnO Thin Films using by BCl@sub3@/Ar Inductively Coupled Plasma, ***J.C. Woo***, *C.M. Kang, J.S. Kim, G.H. Kim, K.T. Kim, C.I. Kim,* Chung-Ang University, Korea

The specific electrical, optical and acoustic properties of Zinc Oxide (ZnO) are important for semiconductor process which has many various applications. Piezoelectric Zinc Oxide (ZnO) film has been widely used for transducers, bulk and surface acoustic- wave resonators, and acousto-optic devices. Also, it has advantages relative to GaN because of its availability in bulk, single-crystal form, and its larger exciton binding energy (~60 meV, cf. ~25 meV for GaN). Research and development of ZnO have been rapidly accelerated to improve materials for the last decades. But, etch properties of ZnO have not established yet. In this study, we investigated etch characteristics of dry etching of the ZnO thin films in the inductively coupled plasma etch system with (BCl@sub 3@/Ar) gas mixture. The etching characteristics of ZnO thin films were investigated in terms of etch rates and selectivity as a function of (BCl@sub 3@/Ar) gas mixing ratio, rf power, dc bias voltage and chamber pressure. The plasmas were characterized by optical emission spectroscopy (OES) and Langmuir probe analysis. The chemical states on the etched surface were investigated with x-ray photoelectron spectroscopy (XPS). Scanning electron microscopy (SEM) was used to investigate the etching profile.

EM-ThP6 Electroluminescence from ZnO Nanowire/Polymer Composite p-n Junction, ***C.-Y. Chang***, *F.-C. Tsao, C.-J. Pan, G.-C. Chi,* National Central University, Taiwan*; H.T. Wang, J.-J. Chen, F. Ren, D.P. Norton, S.J. Pearton,* University of Florida*; K.-H. Chen, L.-C. Chen,* National Taiwan University, Taiwan

Zinc oxide (ZnO) is an attractive candidate for UV light emission since it is an environmentally friendly material which be grown at low temperatures on cheap transparent substrates and has both a direct wide band gap of 3.3 eV and a very large exciton binding energy of 60meV,important for robust light emission. In addition, it has been suggested that semiconducting nanowires may offer additional advantages for light emission due to the increased junction area, reduced temperature sensitivity, enhanced polarization dependence of reflectivity and improved carrier confinement in 1-D nanostructures. The characteristics of a hybrid p-n junction consisting of the hole-conducting polymer poly(3,4-ethylene-dioxythiophene)-poly(styrene-sulfonate)(PEDOT/PSS) and n-ZnO nanorods grown on a n-GaN layer on sapphire are reported. To fabricate the nanowire light emitting devices, the nanowire array was first coated with polystyrene, followed by photoresist. Spin-coating of polystyrene was used to electrically isolate neighboring nanorods and a top layer of transparent conducting indium-tin-oxide (ITO) was used to contact the PEDOT/ PSS. Multiple peaks are observed in the electroluminescence spectrum from the structure under forward bias, including ZnO bandedge emission at ~383 nm as well as peaks at 430,640 and 748 nm. The threshold bias for UV light emission was <3 V, corresponding to a current density of 6.08 A.cm-2 through the PEDOT/ PSS at 3 V. These initial results show that a low-cost, low temperature process holds strong potential for ZnO-based UV light emission and reduces the requirement for achieving robust p-doping of ZnO films or substrates.

EM-ThP7 Reliability of Gate Dielectrics for ZnO Thin-Film Transistors Operating at Low Voltages, ***M.S. Oh***, *K.M. Lee, K.H. Choi, S. Im,* Yonsei University, Korea

ZnO-based thin-film transistors (TFTs) have attracted much attention from researchers and engineers because of their novel potentials: the realization of transparent TFTs, replacing amorphous Si-TFTs, and being a component of effective ultraviolet (UV) detecting devices. PECVD(Plasma Enhanced Chemical Vapor Deposition) SiN@sub x@ has been used as a gate dielectric in the fabrication of amorphous silicon (a-Si:H) TFT arrays for large area liquid crystal displays(LCDs). Since PECVD is a low-temperature process and the SiN@sub x@ layer is a transparent materials, SiN@sub x@ is one of the

powerful candidates for the dielectric layer in transparent electronics applications using ZnO-based TFTs. Additionally the dielectric constant of SiN_x is quite high (~7), so that we may drive the ZnO-TFTs at low voltage(~5V) if the dielectric is as thin as 200 nm (resultant capacitance ~31 nF/cm^2). We have fabricated the ZnO-based TFTs with 200 nm-thick SiN_x dielectric layers which were deposited by PECVD. The undoped ZnO was used for a channel layer and was deposited by rf sputtering at room temperature. For the source/drain electrodes, we have used the Al and the substrate was an ITO glass. The field mobility of our ZnO-TFT was ~0.7cm^2/Vs while the turn-on voltage was less than ~5V. However, our ZnO-TFT also showed inferior on/off current ratio of less than 10^3 and unreliable gating with a large gate voltage hysteresis, of which the origin is not clear but probably related to deposition-induced-hydrogen in SiN_x. In the present work, the reliability of SiN_x dielectric for ZnO-TFT will be discussed in detail and another results from adopting different gate dielectric such as rf sputter-deposited AlO_x will also be presented.

EM-ThP8 Metal Oxide Gas Microsensors for Sensing & Recognition of Low Concentrations of Hazardous Chemicals*, **J.K. Evju**, B. Raman,* National Institute of Standards and Technology*; Z. Boger,* OPTIMAL - Industrial Neural Systems, Israel*; D.C. Meier, K.D. Benkstein, C.B. Montgomery, S. Semancik,* National Institute of Standards and Technology

Considerable motivation exists for developing solid-state microdevices that can reliably detect chemical hazards. We describe our efforts on metal oxide-based conductometric sensor arrays, where the semiconducting oxides on the elements transduce surface chemical interactions into measurable electronic signals. The temperature dependent adsorption, desorption and reaction processes on the thin metal oxide sensing film surfaces give rise to carrier concentration changes that are readily measured on our microhotplate chemical sensor arrays. By utilizing addressable heating of individual sensor elements, together with thermally activated chemical vapor deposition (CVD), we grow different types of oxides onto our microhotplate gas sensor array elements in a self-lithographic process. The selectivity offered by these oxides, coupled with rapid temperature modulation of individual sensor elements, provides a basis of tunability that we take advantage of for gas sensing and recognition. We will illustrate how we harness information from the physical surface processes on our individually addressable sensor array elements, that are comprised of controlled temperature MEMS based microhotplate devices. Our focus will be on challenges associated with recognition of chemical warfare simulants (CWSs) and toxic industrial chemicals (TICs) at low concentrations (ppt to ppb) in air.

EM-ThP9 Micro-Optical Switch Device Based on Semiconductor-To-Metallic Phase Transition Characteristics of W-doped VO_2 Smart Coatings*, **M. Soltani**, M. Chaker,* INRS-Energie, Matériaux et Télécommunications, Canada*; E. Haddad, R.V. Kruzelecky,* MPB Communications Inc.*; J. Margot,* Université de Montréal, Canada

Thermochromic vanadium dioxide (VO2) smart coatings undergo a reversible semiconductor-to-metallic phase transition (SMT) at a transition temperature of Tt = 68°C. This phase transition is accompanied by an important modification of the electrical resistivity, optical transmittance and reflectance in the infrared region. The Tt can be controlled by doping the coating with donor-like or acceptor-like centers. In addition, the SMT of VO2 thin films can be controlled by external parameters such as temperature, pressure, photo-carrier injection into a VO2 heterostructure, and an electric field. VO2 smart coatings are thus excellent materials for technological applications such as optical fiber switching devices,[1] smart radiator devices for spacecraft,[2] all-optical and electro-optical switching devices.[3] Recently, we have optimized the reactive pulsed laser deposition (RPLD) parameters to grow either an undoped or metal (W and Ti) doped VO2 smart coatings on large area substrates[4] as well as on small area substrates such as ends of cleaved fibers and optical fibers connectors. Also, we were able to control the SMT of the VO2 layers by photo-excitation (i.e., all-optical switching), as well as by an external electric-field (i.e., electro-optical switch). In this paper, we present our recent results on the fabrication and characterization of micro-optical switch device exploiting the semiconductor (on) to metallic (off) states of W-doped VO2 active layers driven by an external voltage. The active layers were synthesized on sapphire substrate by means of RPLD. The micro-optical switch was patterned by photolithography and plasma etching. While the NiCr electrical contacts were patterned by means of the lift-off process. The transmittance switching (on/off) of the fabricated device was investigated at λ = 1.55 µm as a function of the applied voltage through the NiCr electrical contacts. An extinction ratio (on/off) as high as 20 dB was achieved with this device.

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[2] R.V. Kruzelecky, E. Haddad, W. Jamroz, M. Soltani, M. Chaker, and G. Colangelo, Proc. SAE, Paper 2005-01-2906 (2005).
[3] M. Soltani, M. Chaker, E. Haddad, and R. V. Kruzelecky, Meas. Sci. Technol.17, 1052 (2006).
[4] M. Soltani, M. Chaker, E. Haddad, R. V. Kruzelecky, and J. Margot, Appl. Phys. Lett. 85, 1958 (2004).

EM-ThP10 Characteristics of Ohmic Contact Properties on N-polar Face n-type GaN with Dry and Wet Etching Method*, **T. Jang**, Y.J. Sung,* Samsung Advanced Institute of Technology, Korea, South Korea*; O.H. Nam, Y. Park,* Samsung Advanced Institute of Technology, Korea

Recently, remarkable progress on the development of blue and violet laser diode (BV-LD) has been made by several companies (Nichia, Sony and Samsung). BV-LD is a key component as a light source for high density optical storage systems and large scale display systems. Most of the commercialized high-power BV-LDs are fabricated on the free standing GaN wafers because of their high thermal conductivity, ease of cleaving and simple fabrication process. Free standing GaN wafer has a wurtzite crystal structure which has two different polarities along the c-axis direction, (0001) Ga face and (0001(_)) N face, respectively. The (0001) surface is composed of three nitrogen dangling bonds which points upward the c-plane surface, while (0001(_)) surface has a single nitrogen dangling bond that points upward. This difference in surface structure affects the device characteristics, especially ohmic contacts properties. Instead of using just Ga-face surface (0001), both Ga-polar face (0001) and N-polar face (0001(_)) surfaces would be used with free standing GaN wafers to fabricate LDs. One of the serious concerns in the fabrication of high-power BV-LDs is the difficulty of achieving reliable ohmic contact property on N-polar face n-type GaN. In this study, the effects of surface treatments such as ICP (Inductively Coupled Plasma) and wet etchings prior to the ohmic contact formation were investigated by measuring the contact resistivity of TLM (Transfer Length Method). Ohmic contact materials comprised of the layer sequence of Al/Ti and Pd/Ti/Al were deposited and contact resistivities were measured with respect to the annealing temperatures. The results of contact resistivity and AFM (Atomic Force Microscopy) confirmed that the area of contact is directly related to the improvement of ohmic contact property on N-polar face n-type GaN.

EM-ThP12 The Structural and Optical Properties of InN Layers Grown by High Pressure CVD*, **M. Alevli**, G. Durkaya,* Georgia State University*; W. Fenwick,* Georgia Institute of Technology*; A. Weerasekara, V.T. Woods,* Georgia State University*; I. Ferguson,* Georgia Institude of Technology*; U. Perera, N. Dietz,* Georgia State University

Indium nitride (InN), with its high mobility and small effective electron mass among the nitrides, is a promising material for advanced optoelectronic device applications. Indium-rich alloys, e.g. $(Ga_{1-y-x}Al_yIn_x)N$ will enable the fabrication of high-efficient light emitting diodes tunable in the whole visible spectral region, as well as advanced high speed optoelectronics for optical communication. The present limitation in this area is the growth of high quality InN and indium-rich group III-nitride alloys as documented in many controversial reports on the true physical properties of InN. The difficulties arise from the low dissociation temperature of InN that requires an extraordinarily high nitrogen overpressure to stabilize the material up to optimum growth temperatures. We developed a novel high-pressure chemical vapor deposition (HPCVD) system, capable to control and analyze the vast different partial pressures of the constituents. Our results show that the chosen HPCVD pathway leads to high-quality single crystalline InN, demonstrating that HPCVD is a viable tool for the growth of indium rich group III nitride alloys. The structural analysis of InN deposited on GaN-sapphire substrate by XRD show single phase InN(0002) peaks with full width half maximum (FWHM) around 430 arcsec. Infrared reflectance spectroscopy is used to analyze the plasmon frequencies, high frequency dielectric constants, the free carrier concentrations and carrier mobilities in these layers. For nominal undoped InN layers, free carrier concentrations in the mid 10E+19cm-3 and mobilities around 600 cm+2-V-1-s-1 are observed. A further improvement is expected as the growth parameters are optimized. At present, the growth of InN is carried out at temperatures as high as 1150 K for reactor pressures around 15 bar, which is a major step towards the fabrication of indium rich heterostructures due to the closer match to the ideal processing temperatures of (Ga1-y-xAlyInx)N.

EM-ThP13 Reliability Performance and Electrical Comparison of TiB@sub 2@ ,CrB@sub 2@ and W@sub 2@B@sub 5@ Based Ohmic Contacts on n-GaN*, R Khanna, S.J. Pearton, F. Ren, I.I. Kravchenko,* University of Florida

Three different metal borides (TiB@sub 2@, CrB@sub 2@ and W@sub 2@B@sub 5@) were examined for use in Ti/Al/boride/Ti/Au Ohmic contacts on n-type GaN and the reliability compared to the more usual Ti/Al/Ni/Au metal scheme. The minimum specific contact resistance obtained was in the range 10@super -5@ @ohm@.cm@super 2@ with CrB@sub 2@ and W@sub 2@B@sub 5@ and approximately an order of magnitude lower with TiB@sub 2@. In all cases, the minimum contact resistance is achieved after annealing in the range 700-900°C. The main current transport mechanism in the contacts after this annealing is tunneling as determined by the absence of any significant measurement temperature dependence to the contact resistance. The TiB@sub 2@ and CrB@sub 2@ contacts retain smooth morphology even after annealing at 1000° C. Auger Electron Spectrosopy depth profiling indicated that formation of an interfacial TiN@sub X@ layer is likely responsible for the Ohmic nature of the contact after annealing. All three boride-based contacts show lower contact resistance than Ti/Al/Ni/Au after extended aging at 350°C.

EM-ThP14 Decay Mechanism of Negative Electron Affinity (Cs/O Activated)InP(100) Photocathodes*, D.-I. Lee,* Stanford University, U.S.*; Y. Sun, Z. Liu,* Stanford Synchrotron Radiation Laboratory*; S. Sun,* Stanford University*; P. Pianetta,* Stanford Synchrotron Radiation Laboratory

Negative Electron Affinity (NEA) III-V photocathodes prepared by Cs and oxygen co-deposition have been widely used in technological applications of image intensifiers and e-beam sources due to its beam properties such as high quantum efficiency (Q.E), high spin-polarization, and low energy spread. One of the concerns raised in the usage of these photocathodes is the relatively short lifetime since industry desires that photocathodes last for a long period of time without losing its reliable performance. This lifetime issue is induced by the fact that very thin Cs oxide layer is extremely sensitive to contamination, which destroys the NEA properties of the surface and reduces its Q.E. The lack of understanding of the very thin Cs oxide activation layer, however, prevents researchers from providing a profound way to achieve long-lifetime stability especially when the photocathode is not in a sealed tube. In this study, we have investigated the decay mechanism of Cs/O activated InP(100) photocathode by Synchrotron Radiation Photoemission (SR-PES) and Energy Distribution Curve (EDC) measurements. We found that decay of Q.E. and the increase of electron affinity are due to the transformation of Cs peroxide into Cs superoxide and subsequent oxidation of InP substrate. These changes can be explained by thermodynamics. Furthermore, a simplified lateral distribution model of Cs oxide layer on the surface is proposed based on the angular dependence of O1s and valence band spectra. The redeposition of Cs was performed in order to simulate the sealed photocathode tube, and it is found that redeposited Cs recovers Q.E. by building up partial dipoles, and prevents Cs peroxide from transforming into Cs superoxide by acting as a protective layer.

EM-ThP15 Electronic Properties of Adsorbates on GaAs(001)-c(2x8)/(2x4)*, D.L. Winn, M.J. Hale, A.C. Kummel,* University of California, San Diego

The key issue in fabricating a III-V MOSFET is forming an unpinned interface between the gate oxide and the semiconductor. A systematic experimental and theoretical study has been performed to determine the causes of oxide pinning and unpinning on GaAs(100). Scanning tunneling spectroscopy (STS) and density functional theory (DFT) were used to study four different adsorbates (O@sub 2@, Ga@sub 2@O, In@sub 2@O, and SiO) bonding to the GaAs(001)-c(2x8)/(2x4) surface. The STS results revealed that out of the four adsorbates only one left the Fermi level unpinned, Ga@sub 2@O. DFT calculations were used to elucidate the causes of the Fermi level pinning. Two distinct pinning mechanism were identified: direct (the adsorbate induced states in the band gap region) and/or indirectly pinning (generation of undimerized As atoms). In the cause of O@sub 2@ adsorbing onto GaAs the Fermi level pinning was found to result only from indirect case, while, In@sub 2@O was shown to pin the Fermi level directly. SiO however, was found to exhibit both indirect and direct (build-up of local charge, and formation of partially filled dangling bonds on some of the Si atoms) Fermi level pinning. The close correlation between experiment and theory suggest that DFT can be used to predict oxide pinning and unpinning on III-V semiconductors.

EM-ThP16 Bonding Geometries of In@sub 2@O on InAs(001)-(4x2)*, J. Shen, D.L. Winn, N.M. Santagata, A.C. Kummel,* University of California, San Diego

The key to fabricating a high mobility MOSFET is forming an electrically passive oxide-semiconductor interface on a very high molibity semiconductor. The absence of As-As dimers makes the InAs(001)-(4x2) surface ideal for gate oxide deposition, since the surface should not readily react with deposited oxides. Scanning tunneling microscopy (STM) and density functional theory (DFT) were used to definitively identify the InAs(001)-(4x2) reconstruction along with ascertaining how In@sub 2@O adsorbates bond onto the clean surface. The clean surface consists of single In-In dimers that run in the [110] direction. Between the row dimers is a trough region that contains 2 additional In-In dimers. After the InAs(001)-(4x2) reconstruction was identified, In@sub 2@O was deposited onto the clean surface using MBE. The lowest coverage In@sub 2@O adsorption site was identified as an In atom from In@sub 2@O bonding to a tricoordinated As atoms at the edge of the row. When this occurs, it causes the second In atom in In@sub 2@O to bond nonspecifically in the trough region. Evan at low coverage (20% monolayer (ML)), the In@sub 2@O adsorbates formed islands that are elongated in the [110] direction. Prior to all the first layer sites being occupied with In@sub 2@O molecules, second layer growth was observed on the islands. This was attributed to the In atom, in the In@sub 2@O molecule, that protruded into the trough region being highly reactive. Most importantly, the In@sub 2@O adsorbates never causes the abstraction of any surface atoms on the InAs(001)-(4x2) surface. This is consistent with the formation of a smooth interface between the oxide and the semiconductor. STS measurements are being performed to determine the electronic properties of the interface.

EM-ThP17 High Thermal Stability Ag-based Ohmic Contacts for InAlAs/InGaAs/InP High Electron Mobility Transistors*, L. Wang, W.F. Zhao,* ***I. Adesida,*** University of Illinois at Urbana-Champaign

InAlAs/InGaAs/InP HEMTs are promising for microwave applications due to their high-frequency and low-noise characteristics. Low-resistive and high thermal stable ohmic contacts are desirable to fully exploit their potential. The Au-Ge-Ni contacts used for GaAs are also applied in InP-based devices with further optimization. However, the optimum annealing temperatures of these contacts are low (~250 °C). Due to the high diffusivity of Au and low eutectic point of AuGe alloy, these contacts are intrinsically unstable when subjected to thermal processes of fabrication or electrical stresses during operation. We showed that the optimum contact resistance of Au-Ge-Ni is achievable only within a narrow window of ~50 °C which makes the reliable control of device performance problematic. Ge/Ag/Ni ohmic contacts with excellent contact resistance of 0.07 Î©-mm were obtained after annealing at 425 °C. These contacts have a large processing window of >130 °C. A SiNx layer deposited prior to annealing could suppress the degradation of the devices. Storage tests at 215 and 250 °C indicate that this metallization is far superior to the Au-based contacts in term of thermal stability. TEM studies confirm that metal spikes successfully link the 2DEG layer with the metal layer to produce excellent ohmic characteristics. The spikes are mainly Ag and Au, respectively, as identified by EDS. For the optimum annealed samples, the Ag and Au spikes have similar area density and penetration depth. This is a logical result since the injection properties/efficiencies of the metal spikes, which are dictated by the density, size, and shape of the spikes, determine the ohmic performance. The formation of liquid Au-Ge eutectic phase in Au-Ge-Ni at 300 °C and the fast diffusion of Au are believed to be the reason of overannealing. The eutectic temperature of Ag-Ge is 300 °C higher rendering Ag-contacts a higher annealing temperature and a wider processing window.

EM-ThP18 Ion-channeling Damage Profiles in Ferromagnetic Mn-implanted Si*,* ***C. Awo-Affouda,*** *M.B. Huang, V.P. LaBella,* University at Albany-SUNY

Semiconductor devices which exploit the spin of the electron have potential to produce devices with increased functionalities. Making conventional semiconductors such as GaAs and Si ferromagnetic via doping with Mn will aid in fabricating these future spintronic devices. It has been suggested that the residual implant damage after post implant annealing plays a role in the magnetic behavior of Mn-implanted Si. To further investigate this, lattice disorder depth profiles were obtained from RBS-channeling experiments on Mn implanted p-type Si samples. These profiles reveal a strong influence of the Mn fluence and the post implant annealing temperatures upon the defects generated from implantation. Specifically, above 800C, the back scattering yield from Si lattice defects decreases

which is coincident with a decrease in the magnetization. Modeling is also performed to help understand the type of defects and their distributions.

EM-ThP19 Ferroelectric Properties of Na@sub 0.5@ K@sub 0.5@ NbO@sub 3@ Thin Films for Nonvolatile Ferroelectric Random Access Memory*, **K.T. Kim**, C.I. Kim,* Chung-Ang University, Korea

The ferroelectric sodium-potassium niobate Na@sub 0.5@ K@sub 0.5@ NbO@sub 3@ (hereafter NKN, a solid solution of KNbO@sub 3@ and NaNbO@sub 3@) thin films have received the intent attention for their excellent ferroelectric, crystalline properties and lead-free materials. It was shown that NKN thin films are able to overcome the drawbacks of other materials, such as SBT and PZT, for nonvolatile memory applications. The NKN thin films were prepared by using metal organic decomposition method. The structure and morphology of the films were analyzed by x-ray diffraction (XRD), atomic force microscope (AFM), and Scanning electron micrograph (SEM). SEM and AFM showed uniform surface of the films. From the XRD analysis, the NKN thin films were grown using a Pt bottom electrode showed a polycrystalline phase. The remanent polarization Pr and coercive field is 13.5 µmC/cm@super 2@ and 89 kV/cm. The BLT thin films on Pt bottom electrode exhibited no significant degradation of switching charge at least up to 5 x 10@super 9@ switching cycles at a frequency of 50 kHz below cycling fields of 5 V.

EM-ThP20 Fatigue Characteristics of PZT Thin Film Capacitors with Controls of CMP Process Parameters and Slurry Contaminations*, **Y.-K. Jun**, N.H. Kim, W.-S. Lee,* Chosun University, Korea

Pb(Zr,Ti)O@sub 3@ (PZT) is very attractive ferroelectric materials for ferroelectric random access memory (FeRAM) applications because of its high polarization ability and low process temperature. In this study, PZT thin film capacitors were fabricated by damascene process instead of plasma etching process. Damascene process of PZT thin film was first applied for the densification of devices and the protection of plasma damages including ion charging. However, chemical mechanical polishing (CMP) pressure and velocity must be carefully adjusted because FeRAM shrinks to high density devices. The probability of CMP damage such as microscratch surely existed although the removal rate of PZT thin films increases and the yield improves through the each increase of CMP pressure and velocity. The contaminations such as slurry residues due to the absence of the exclusive cleaning chemicals are enough to influence on the degradation of PZT thin film capacitors. The fatigue characteristics of the degradations of PZT thin film capacitors were investigated by the change of process parameters and the cleaning process. Both the low CMP pressure and the cleaning process must be employed, even if the removal rate and the yield were decreased, to reduce the fatigue of PZT thin film capacitors fabricated by damascene process. Like this, fatigue characteristics were partially controlled by the regulation of the CMP process parameters in PZT damascene process. And the exclusive cleaning chemicals for PZT thin films were developed in this work. Acknowledgement: This work was supported by Korea Research Foundation Grant (KRF-2004-005-D00007).

EM-ThP21 Molecular Beam Epitaxy of YMnO@sub 3@ on c-plane GaN*, **C.B. Keenan**, T. Liu, K. Lee, R.P. Tompkins, E.D. Schires, Y. Chye, D. Lederman, T.H. Myers,* West Virginia University

Ferroelectric oxide thin films on semiconductors have attracted attention for their potential applications in nonvolatile memory, piezoelectric, and microwave devices. Interest is now emerging in the potential of new devices based on active interfaces between ferroelectric oxides and polar semiconductors such as GaN or ZnO. YMnO@sub 3@ is an obvious candidate of oxide films on GaN because they both have a hexagonal lattice structure and the lattice constant of YMnO@sub 3@ is approximately twice that of GaN. Here we report on the epitaxial growth of YMO thin films directly on GaN using MBE. YMnO@sub 3@ films are grown on GaN (0001)-on-sapphire templates using MBE. The structure of the films as characterized by in-situ RHEED, x-ray diffraction, and atomic force microscopy will be discussed. Atomic force microscopy revealed that the YMnO@sub 3@ films grown at different temperatures have significantly different morphologies. Samples grown at the optimal growth temperature are ferroelectric at room temperature, and magnetic at low temperatures. The YMnO@sub 3@ samples exhibit a remnant polarization of approximately 3.2 @micro@C/cm@super 2@ and saturation polarization of about 12 @micro@C/cm@super 2@. The difference between magnetic field-cooled and zero-field-cooled behavior at low temperatures suggests the presence of either antiferromagnetic frustration or ferromagnetic behavior. The effects of different growth temperatures and post-growth annealing will also be discussed. This research was supported by US Office of Naval Research (Grant N00014-02-1-0974), the US Air Force Office of Scientific Research (MURI Grant F49620-03-1-0330), and by the US National Science Foundation through the West Virginia EPSCoR program.

EM-ThP22 Integration of Barium Ferrite on the Wide Bandgap Semiconductor 6H-SiC Through Molecular Beam Epitaxy*, **Z. Cai**, Z Chen, T.L. Goodrich, V.G. Harris, K.S. Ziemer,* Northeastern University

Integration of nonreciprocal ferrite microwave devices with semiconductor platforms would allow for reduced volume and weight in phased array radar electronics, in addition to enhanced bandwidth and power management. Barium hexaferrite (BaM, BaFe@sub 12@O@sub 19@) is ideal for microwave device applications because of its large (17kOe) uniaxial magnetocrystalline anisotropy, high resistivity and permeability at high frequencies (>40GHz). The performance of current ferrite devices would be enhanced and novel devices would be possible if BaM were integrated with wide bandgap semiconductors (e.g. SiC), which can function in high-temperature, high-power, and high-frequency environments. However, oriented, single-crystalline BaM films with the desired magnetic properties (high saturation magnetization and low FMR linewidth) have not yet been successfully grown on any semiconductor substrate. In order to produce BaM thin films with desired stoichiometry, structure, and magnetic properties needed for microwave device applications, the nucleation and growth mechanisms of BaM on 6H-SiC were investigated using a remote oxygen plasma source producing a chamber oxygen pressure of 5x10@super -6@ Torr, and solid source Ba and Fe effusion cells. In-situ x-ray photoelectron spectroscopy (XPS) and reflection high-energy electron diffraction show oxygen rich (@>=@69%) and iron deficient (@<=@20%) polycrystalline films, which suggest complex surface reactions among the metals and the oxygen. Preliminary XPS studies of BaM films deposited by pulsed laser deposition (PLD) show different compositions and O bonding states with respect to the thickness of the films. Films grown on SiC by PLD are porous with either FMR linewidth of >500 Oe or no FMR at all. Using a MgO interlayer structure between the BaM and SiC has been shown to prevent silicon diffusion into BaM films and reduce bond mixing at the interface, which results in FMR linewidths

EM-ThP23 Ferroelectric and Dielectric Properties of BLT Capacitors Fabricated by Damascene Process using Chemical Mechanical Polishing*, **S.H. Shin**, P.J. Ko, N.H. Kim, W.-S. Lee,* Chosun University, Korea

Nonvolatile memory devices using ferroelectric thin films such as PZT, SBT and BLT have attracted attention because of their non-volatility and high-speed operations. However, commercial use of PZT ferroelectric memory devices has been hindered largely by fatigue, defined as the decrease of switchable polarization with electric field cycling in ferroelectrics. Whereas, as a fatigue-free material, SBT is limited in the practical application due to its small polarization and high processing temperature. More recently, BLT is of particular interest, as it is not only crystallized at relatively low processing temperature, but also shows highly fatigue resistance and large remanent polarization. Meanwhile, these submicron ferroelectric capacitors were fabricated by a damascene process using Chemical mechanical polishing (CMP). The fabricated capacitors consisted of BLT thin film with top and bottom electrodes. The P-E characteristics of BLT capacitors fabricated by CMP were examined at various voltages and room temperature. Remanent polarization was identified by the measuring of electric hysteresis loops for the capacitors. Dielectric property and loss factor (dissipation factor) were investigated as a function of frequency with LCR meter. Ferroelectric BLT capacitors were practicable by a damascene process using CMP, which realized a vertical sidewall.

EM-ThP24 P Incorporation during Si(001):P Gas-Source Molecular Beam Epitaxy: Effects on Growth Kinetics and Surface Morphology*, **B. Cho**, J. Bareno,* University of Illinois at Urbana-Champaign*; Y.L. Foo,* Institute of Materials Research and Engineering, Singapore*; S. Hong,* Seoul National University, Korea*; T. Spila, I. Petrov, J.E. Greene,* University of Illinois at Urbana-Champaign

The effects of P doping on growth kinetics and surface morphological evolution during Si(001):P GS-MBE from Si@sub2@H@sub6@ and PH@sub3@ at temperatures T@subs@ = 500-900 °C have been investigated. With increasing PH@sub3@/Si@sub2@H@sub6@ flux ratio J@subP/Si@ at constant T@subs@, we observe a decrease in the film growth rate R, accompanied by increased surface roughening and pit formation. At constant J@subP/Si@, R increases with increasing T@subs@, while the incorporated P concentration C@subP@ initially increases, reaches a maximum at T@subs@ = 700 °C, and then decreases at higher growth temperatures. We use in-situ D@sub2@ temperature programmed

desorption (TPD) to follow changes in film surface composition and dangling bond density @theta@@subdb@ as a function of J@subP/Si@ and T@subs@. Measurements on both as-deposited Si(001):P layers and P-adsorbed Si(001) reveal @beta@@sub1@ and @beta@@sub2@ peaks due to D@sub2@ desorption from Si monohydride and dihydride species, respectively, as well as the formation of a third peak @beta@@sub3@ corresponding to D@sub2@ desorption from mixed Si-P dimers. Dissociative PH@sub3@ adsorption on Si(001) results in a decrease in @theta@@subdb@ and an initial increase in P surface coverage @theta@@subP@ with increasing T@subs@. @theta@@subP@ reaches a maximum value of 0.95 ML at T@subs@ = 550 °C, and decreases with T@subs@ > 600 °C due to the onset of P@sub2@ desorption. Comparison of @theta@@subP@(T@subs@) with C@subP@(T@subs@) results obtained during film growth reveals the presence of strong P surface segregation. From measurements of @theta@@subP@ vs. C@subP@ in Si(001):P layers, we obtain a P segregation enthalpy @DELTA@H@subs@= -0.86 eV. Using the combined set of results, we develop a predictive model for C@subP@ vs. T@subs@ and J@subP/Si@, incorporating the dependence of the PH@sub3@ sticking probability S@subPH3@ on @theta@@subP@, which provides an excellent fit to the experimental data.

**EM-ThP25 Solid Source Phosphorous Doping in Si*, G.G. Jernigan,* ***P.E. Thompson,* U.S. Naval Research Laboratory

Phosphorus doping in Si is being pursed as a possible single spin qubit for quantum computing and as a delta layer for use in a resonant interband tunnel diode. We are using a unique doping source, based on the decomposition of GaP, to produce P in a solid source molecular beam epitaxy machine. This has advantages over the use of phosphine gas decomposition due to the use of lower sample temperatures (< 500 °C) and higher surface coverages (due the absence of hydrogen). We will present a study of the adsorption and desorption of P in the temperature range of 25-800 °C on a Si (100) surface using in vacuo XPS and STM. P is found to adsorb up to one complete monolayer (ML) between 25 and 500 °C and does not form a multilayer. The surface consists of long rows of P dimers separated by vacancy lines. Beginning with 1 ML, P desorbs from Si between 500 and 800 °C. A simple Redhead analysis indicates a second order desorption with an activation energy of ~29 Kcal/mol. Desorption disrupts the P dimer morphology resulting in individual P atoms moving on the surface. STM IV analysis indicates that layer conductivity changes when the dimers break and when P begins to desorb. Compared to a Si surface without P, we find that annealing a surface with a submonolayer of P produces a surface whose step edges are very highly kinked. The relevance of P surface coverage and surface morphology, along with the co-deposition of P and Si, to device applications will be discussed.

EM-ThP28 Local Structure Around Germanium Atoms in SiGe Thin Films*, Y. Uehara,* *K. Kawase,* Mitsubishi Electric Co., Japan*; J. Tsuchimoto,* Renesas Co., Japan

SiGe thin films are widely studied in order to apply them as the channel layer for LSI of the next generation, because they show superior electronic properties than the current silicon channel. More germaniums in film enhance the electron mobility, while the lattice mismatch of the film with the substrate becomes large, so it is important to control the concentration of germanium in the film. Also, it should be important to control how the germanium atoms are involved in the film, however, there are few information on them. In this study, we have applied XAFS technique to investigate the local structure around germanium atoms in SiGe thin films. SiGe films were prepared by CVD method on Si(100) wafers. Si/Ge ratio of the films was controlled by the flow rate of the origin gases. The germanium concentration and the thickness of the films were confirmed by X-ray locking curve method and X-ray reflectivity method, respectively. XAFS measurements at Ge-K absorption edge were performed at BL16B2 of SPring-8. The Si(311) double crystal monochromator and the Rh-coated cylindrical mirror were used, and electrons emitted from the sample surface were collected using a conversion electron yield detection system. We could not find any changes in the Ge-K XANES region among the samples with different germanium concentration. The standard EXAFS analysis was performed to elucidate the local structure around the germanium atoms in the films. The curve fitting analysis revealed that the germanium atoms in as-deposited SiGe thin films make complete solid solution with silicon, do not conform micro-clusters of germanium, at least when the germanium concentration is less than 20%.

EM-ThP29 Inspection and Analysis of Voiding Defects in Copper Interconnects on a Test Wafer*, S. Suzuki,* *Y. Nakano, K. Umemura, T. Sato,* Hitachi High-Technologies Corporation, Japan

For improvement of yield of LSI, it is necessary to use the analysis system that consists of inspection of defects of a wafer, analysis of defects and countermeasures. Voiding of Cu interconnects affect yield and reliability of ULSI, therefore it is so useful to detect efficiently voids of Cu layer in the manufacturing process. In this study, we have investigated the efficient analysis technique of voids by using the system. Void and etching stopped defects were intentionally on a 200mm wafer with 160nm diameter Cu via pattern made by typical single damascene process. Inspection of the wafer was done by electron beam (EB) inspection and optical inspection equipments, for cross section analysis samples from the wafer were made by focused ion beam (FIB) equipment, and defects were observed by scanning transmission electron microscope (STEM) with energy dispersive X-ray spectroscopy (EDS).The 2 types of defects (called one gray defect, the other dark defect), which contrast were different, were detected by EB inspection. The STEM results confirmed that gray defect was a void defect; dark one was an etching stopped defect. By cross section observation of 10 defects, there is a coincidence that all gray defects were voids and all dark were etching stopped. In the gray defect Cu was partially missing and only Ta/TaN layer remained, and it was estimated that voiding was finally occurred at annealing step of process because Cu seed layer also was missing. We are able to explain that difference of contrast is caused difference of electrical current through via, which depends on resistivity, for example a single via with 180nm height void is 10 times resistivity of that without void by rough calculation. In addition, we tried to quantify SEM image of the 2 types of defects, and actually measure resistivity of via by means of electrical probing equipment with SEM. Finally we find that EB inspection and quantification of SEM image is an efficient method to detect and classify defects.

EM-ThP30 Oxidation of Thin Y-Si Film on Silicon*, S.Y. Chiam,* Imperial College, United Kingdom*; W.K. Chim,* National University of Singapore*; A.C. Huan,* Nanyang Technological University, Singapore*; J. Zhang,* Imperial College, UK*; J.S. Pan,* Institute of Materials Research & Engineering, Singapore

Oxidation studies are investigated on sputtered films in the formation of yttrium silicate by a two step process. Firstly, an in-situ low temperature annealing of yttrium (Y) metal on silicon (Si) is performed to obtain a Y-Si film. The Y-Si film is then oxidized ex-situ in a horizontal furnace of either nitrogen (N2) or oxygen (O2) ambient. Deposited films are investigated by depth profiling X-ray photoelectron spectroscopy (XPS). We report on self-limiting formation of yttrium silicate at room temperature which is insensitive to annealing ambient. We also found that oxygen pressure plays an important role in the extent of Si oxidation at mid-annealing temperature. Finally, we report that a relatively high temperature is needed for the complete oxidation of Y-Si films in the formation of yttrium silicate films. This is attributed to a high diffusion barrier for oxygen caused by initial yttrium silicate films formed on the top of the film which is the limiting mechanism for the oxidation of Y-Si film.

EM-ThP31 Effects of NO Addition on Chemical Dry Etching of Silicon Oxide Layers in F2/Ar and F2/Ar/N2 Remote Plasma Processing*, Y.B. Yun,* *D. Kim,* Sungkyunkwan University, Korea*; Y.-C. Jang, G. Bae,* Atto Inc in Korea

Chemical dry etching and cleaning process of silicon oxide layers in Si device manufacturing fabs have been carried out using PFCs. Etching process utilizing F@sub 2@gas is of a great interest. We carried out etching experiments using F@sub 2@/Ar, F@sub 2@/Ar/N@sub 2@ remote plasma generated from a toroidal-type remote plasma source in a commercial PECVD system. And the effect of directly-injected NO gas on the SiO@sub 2@ etching in F@sub 2@/Ar/N@sub 2@ remote plasmas was investigated. Etching experiments were carried out by varying the gas flow ratio, flow rate, RF power, and temperature. The effects of NO addition to F@sub 2@/Ar, F@sub 2@/Ar/N@sub 2@ etching were characterized by measuring the etch rates and by analyzing the emitted species during etching. The results showed that the addition of NO gas increased the etch rates significantly. The mechanism for etch rate enhancement will be discussed in detail in conjunction with the gas emission analysis using FT-IR and RGA and chemical composition of the etched oxide surface using XPS.

EM-ThP32 Yield improvement of 0.13 µm Cu/Low-k Dual Damascene Interconnection by Organic Cleaning Process*, H.K. Lee,* Chung-Ang University, Korea*; N.H. Kim,* Chosun University, Korea*; S.Y. Kim,* DongbuAnam Semiconductor Inc., Korea*; C.I. Kim, E.G. Chang,* Chung-Ang University, Korea

Cu/low-k dielectrics are required to reduce RC delay and parasitic capacitance of the back-end-of-line (BEOL) interconnection. Integration of Cu/low-k dielectrics for BEOL interconnection in the 0.13 µm technology has gained wide acceptance in the microelectronics industry in recent years. In this paper, we discuss the process integration issues of the 0.13 µm Cu/low-k (Black Diamond) dual damascene integration for SRAM device yield. The same scheme of 0.13 µm Cu/ fluorinated silicate glass (FSG) based device was used for full process in making low-k based device. Black diamond was used as a low-k material with a dielectric constant of 2.95. To reduce the damage of low-k and improve the yield of low-k based device, H@sub 2@O ashing, organic cleaning, and low down pressure in chemical mechanical planarization (CMP) were selected for the study. Specially, the organic cleaning process after ashing process is very effective on the removal of organic residues in via and trench, and surface contaminant. There is an increase of 40% SRAM device yield, compared to low-k based device which is uncleaned after ashing process. As a result, we successfully integrated 0.13 µm Cu/low-k (Black Diamond) dual damascene interconnection with excellent yield performance after process improvement of organic cleaning.

EM-ThP33 Etch Induced Sidewall Damage Evaluation in Porous Low-k MSQ Films*, **B. Kong**,* Sungkyunkwan University, Korea*; T. Choi, S. Sirard,* Lam Research Corporation*; D. Kim,* Sungkyunkwan University, Korea

As device feature sizes shrink down to 45nm and below, films with lower dielectric constants (k) are needed to reduce the RC delay in copper backend applications. The plasma etch-induced damage (carbon depletion, moisture uptake, silanol formation) of porous low-k methyl silsesquioxane (MSQ, k=2.2) films was investigated. Etch-induced damage was characterized on both blanket and trench patterned MSQ materials. The MSQ materials were etched with CF4 and C4F8-based chemistries under various process conditions. Simple CF4/O2 chemistry minimized the damage of porous MSQ during plasma etching. The addition of Ar or H2 increased the damage. The highest damage levels were observed with simultaneous Ar, H2 and N2 addition. Also, the use of higher powers and/or lower pressures resulted in more etch-induced damage.

EM-ThP34 Arsenic Ultra Shallow Junction Deactivation Investigated by Multi-Technique Analytical Approach*, **M. Bersani**, G. Pepponi, D. Giubertoni, S. Gennaro, M. Anderle,* ITC-irst, Italy*; R. Doherty, M.A. Foad,* Applied Materials

New processes are needed to satisfy the requirements of modern ULSI C-MOS fabrication. In particular for source and drain extension laser sub-melt annealing has arisen as an emerging tool able to produce high level of dopant activation together with ultra shallow distribution. Nevertheless arsenic (the most used n-type dopant) is known to easily deactivate when further thermal annealings are carried out after laser treatment. A detailed study is required in order to understand its behavior in high concentration regime and in close proximity of the surface as in the case of ultra shallow distribution. In this work ultra shallow arsenic implants (2 keV implant energy, dose ranging from 3E13 to 3E15 at/cm2) laser sub-melt annealed have been submitted to further thermal processes in conventional furnace. The samples so produced have been characterized by a multi-technique analytical approach: Secondary Ion Mass Spectrometry (SIMS), Hall Effect measurements, Extended X-ray Absorption Fine Structure (EXAFS). This approach has been chosen to enable the correlation among dopant electrical activation, spatial distribution and the local order structure around arsenic atoms. Results show how Arsenic diffusion and electrical behavior after post laser treatment depend on laser annealing conditions.

EM-ThP37 Effects of Additive C@sub 4@F@sub 8@ on Dry Etching of TaN/HfO@sub 2@ Gate Stack Structure using Inductively Coupled BCl@sub 3@/Ar Plasma*, **J.H. Ko**, M.S. Park, D.-Y. Kim,* Sungkyunkwan University, Korea*; S.S. Lee, J. Ahn,* Hanyang University, Korea*; N.-E. Lee,* Sungkyunkwan University, Korea

As the advanced nano-scale CMOS (complementary-metal-oxide-semiconductor) device dimensions continue to be scaled down below 50 nm, development of advanced high-k gate dielectrics with metal gate electrodes and their integration has obtained considerable interests. Among many integration issues, selective etching processes of metal gate electrodes over the high-k gate dielectrics and the high-k gate dielectrics over the Si substrate are expected to be the critical steps in the process integration of the front-end of the line (FEOL). In this work, we compared the etching characteristics of the TaN/HfO@sub 2@ gate stack structure and etch rate selectivity of the TaN over the HfO@sub 2@ layer in the BCl@sub 3@/Ar and BCl@sub 3@/C@sub 4@F@sub 8@/Ar plasmas by varying the process parameters such as the top electrode power, the DC self-bias voltage (V@sub dc@), and BCl@sub 3@/C@sub 4@F@sub 8@ gas flow ratio. To understand the role of etch gas chemistry in ICP etching, the relative change in the densities of ions and radicals in the plasma and chemical binding states of etched TaN and HfO@sub 2@ surfaces were measured by optical spectroscopy (OES) and X-ray photoelectron spectroscopy (XPS), respectively. The results of the etch rates and etch selectivity measured as a function of the various process parameters will be discussed in detail in conjunction with the OES and XPS analysis data. Keywords: HfO@sub 2@, TaN, plasma etching, ICP (inductively coupled plasma), metal gate stack.

EM-ThP38 Characteristics of the Laminated HfO@sub2@/Al@sub2@O@sub3@ High-k Gate Oxides for Thin Film Transistors*, **S.W. Jeong**, K.-S. Kim, J.-Y. Son,* Sungkyunkwan University, Korea*; Y. Roh,* Sungkyunkwan University, Korea, Republic of Korea

Recently, high-k materials are under consideration as replacements for SiO@SUB2@. Among some metal oxides, HfO@sub2@ is an attractive candidate due to their high dielectric constant and thermal stability in contact with silicon. And Al@SUB2@O@SUB3@ is an another attractive candidate because Al@SUB2@O@SUB3@ can remain amorphous at temperature higher than 900@degree@C. The aim of this study is to investigate the thermal stability of the HfO@sub2@ based films with Al@sub2@O@sub3@. Hf metal films were deposited on the (100) p-type Si/Al@sub2@O@sub3@ substrates (100) p-type Si wafers in sequence by non-reactive magnetron sputtering at room temperature. The Hf metal films deposited on the Si/Al@sub2@O@sub3@ substrate were then subjected to oxidation in O@sub2@ ambient at 500 @degree@C for 60 minutes in furnace. We proposed a new technique to grow Al@sub2@O@sub3@/HfO@sub2@ films on the Si substrate at 500 @degree@C. Oxidation followed by annealing of sputtered Hf metal films on the Si substrate both at 500 @degree@C results in multi-layered Al@sub2@O@sub3@-HfO@sub2@ gate insulator. HfO@sub2@/Al@sub2@O@sub3@ laminate structure ware maintained, and Al@sub2@O@sub3@ layer was not useful for blocking oxygen diffusion due to interfacial layer growth. Crystallization temperature of the HfO@sub2@/Al@sub2@O@sub3@ thin films which has Al@sub2@O@sub3@ was delayed up to 900 @degree@C, and as concentration of the Al@sub2@O@sub3@ in HfO@sub2@/Al@sub2@O@sub3@ thin films increases, thermal stability improved. As an annealing temperature increases, HR-TEM analyses of the all the HfO@sub2@/Al@sub2@O@sub3@ flims show the increased interfacial layer thickness. Therefore, our results show the addition of Al@sub2@O@sub3@ is not useful for blocking oxygen diffusion through the HfO@sub2@/Al@sub2@O@sub3@ thin film. From the C-V and I-V measurements, calculated leakage current of the HfO@sub2@/Al@sub2@O@sub3@ thin films was ~16, and as an annealing temperature increases, the leakage current of the films was improved.

EM-ThP39 High-k Dielectric Lanthanum Oxide Thin Films Deposited by Spray Pyrolysis*, S. Carmona, G. Alarcon,* CICATA-IPN, Mexico*; J. Guzman-Mendoza, M. Garcia-Hipolito,* IIM-UNAM, Mexico*; M. Aguilar,* CICATA-IPN, Mexico*; **C. Falcony**,* CINVESTAV-IPN, Mexico

Lanthanum oxide thin films were deposited on silicon substrates using the spray pyrolysis technique. Several chemical solution concentrations of lanthanum acetylacetonate dissolved in acetylacetone were prepared to obtain the films at substrate temperatures in the range of 450-550 ÂºC. The total thickness of the deposited layers was of the order of 50 Ã.. At low temperatures the films resulted amorphous. In addition, the films were characterized by Ellipsometry (single wavelength and spectroscopic), Infrared Spectroscopy, Atomic Force Microscopy, and Electron Microscopy. The chemical composition was studied by Energy Dispersive Spectroscopy, and by means of nuclear reactions. The electrical behavior of the films (I-V and C-V), is discussed when they are incorporated in Metal-Oxide-Semiconductor structures. The growth of an interfacial layer of silicon oxide in the films was controlled by means of the addition of a water/ammonium hydroxide mist applied during the deposition process.

EM-ThP40 Suppression of Chemical Phase Separation in Hf and Ti Si Oxynitride Alloys with High Silicon Nitride Content, ***S. Lee***, *G. Lucovsky,* NC State University*; J. Luning,* Stanford Synchrotron Radiation Lab

There are two significant materials issues that limit implementation of high and medium k dielectrics into MOS devices. These are grain-boundary defects in high-k transition metal(TM)/rare earth elemental/complex oxides, and chemical phase separation (CPS) at temperatures too low for thermal budget requirements, 35%, and approximately equal concentrations of ZrO_2 and SiO_2, ~ 30-32%, are stable for annealing in inert ambients at temperatures to 1100°C. The results of this paper demonstrate essentially the same behaviors with respect to low and high Si_3N_4 content for Hf Si oxynitrides, Ti Si oxyntirdes, and equally importantly, for Hf-Ti alloy Si oxynitrides. Three different spectroscopies have been used to detect CPS, or the absence of CPS: Fourier transform infrared spectroscopy, derivative x-ray photoelectron spectroscopy for the O 1s core level, and derivative near edge x-ray absorption spectroscopy (NEXAS) for the O K_1 and N K_1 edges. The NEXAS spectra also provide direct confirmation of a chemical bonding self-organization that prevents nucleation and growth of a nanocrystalline TiO_2 or HfO_2 phase that is a necessary precursor to a CPS process.

EM-ThP41 Room-Temperature Magnetron-Sputtered High-k Titanium Silicate Thin Films for MIM and MOS Device Applications, ***D. Brassard,*** INRS-Énergie, Matériaux et Télécommunications, Canada*; L. Ouellet,* DALSA Semiconductor, Canada*; M.A. El Khakani,* INRS-Énergie, Matériaux et Télécommunications, Canada

There is a tremendous ongoing effort for the development of a high dielectric constant (high-k) material that will replace the traditional SiO_xN_y insulator in both metal-oxide-semiconductor (MOS) transistors and metal-insulator-metal (MIM) capacitors. In this context, we report on the development of a room-temperature magnetron co-sputtering process for the growth of high-k titanium silicate ($Ti_xSi_{1-x}O_2$) thin films. $Ti_xSi_{1-x}O_2$ mixed oxide films constitute a highly promising high-k material candidate because they offer the prospect of achieving the best trade-off between the high-k value of the TiO_2 phase and the unpaired insulating behavior of SiO_2. The sputter-deposited $Ti_xSi_{1-x}O_2$ films were integrated into both MIM and MOS capacitors and their structural and electrical properties systematically investigated as a function of the relevant growth conditions (particularly the substrate bias) and the film composition (i.e., the Ti/Si ratio). It is shown that the application of an optimal bias voltage value (of ~ -15 V), during the film growth, leads to a significant densification of the films which in turn is found to improve drastically their electrical properties. Under the optimal growth conditions, the $Ti_{0.5}Si_{0.5}O_2$ films are shown to exhibit an excellent combination of electrical properties, namely: a k of ~17, a leakage current as low as ~10 nA/cm^2 (at 1 MV/cm), and a breakdown field > 4 MV/cm. Moreover, titanium silicate based MIM capacitors showing both high capacitance density of 10 $fF/\mu m^2$ and good capacitance linearity (α < 1000 ppm/V^2) were achieved. Finally, despite the inherent presence of a ~2 nm-thick SiO_2 interfacial layer, $Ti_xSi_{1-x}O_2$ based MOS capacitors with a relatively low density of defects (D_{it} ~$2x10^{11}$ $eV^{-1}cm^{-2}$) were achieved after annealing under forming gas.

EM-ThP42 A Study of High-k Removal by Plasma Etching and its Effect on Gate Dielectric Characterization, ***B.S. Ju***, *S.C. Song, J. Barnett,* SEMATECH*; B.H. Lee,* IBM

A process to remove high-k gate dielectric films (HfO_2 and Hf silicate) from the source and drain (S/D) areas after gate electrode etching was investigated to improve the performance and increase the packing density of CMOS transistors. A vertical gate stack profile can be achieved by replacing the conventional method to remove high-k dielectric films that combined physical bombardment and wet etching. This method has been effective to remove crystallized high-k film, but causes notching in Hf silicate or footing in HfO_2. We propose a new advanced high-k dry etch process using high temperature (250°C) and high density chlorine plasmas (BCl_3/Cl_2). The plasma etch process was optimized to enhance etch selectivity to Si, thus enabling the complete removal of high-k films without any substrate recess in the S/D active regions. Optical emission spectroscopy was used to identify the plasma etching by-products, which were mainly chlorinated hafnium, during plasma etching. After plasma etching, no remaining high-k film on the S/D area was detected with Auger electron spectroscopy (AES) measurement and no residual high-k films or structural weaknesses were found with high-resolution transmission electron microscopy (HRTEM). The new process to remove high-k on a CMOSFET device was electrically compared with the conventional wet chemical removal process. A significant amount of plasma damage on high-k films at the gate edge was found to be induced during dry etching, which generated leakage sources in the gate for both HfO_2 and Hf silicate devices. In situ surface oxidation after plasma removal of the high-k films cured the damage, which dramatically improved leakage current and simultaneously reduced off current, particularly in the short channel, for both PMOS and NMOS devices.

EM-ThP43 Scanning Probe Microscopy Study of Atomic Layer Deposited Hafnium Based High-k Dielectric Films, ***X.-D. Wang***, *D.H. Triyoso, R.I. Hegde, D. Roan, R. Gregory,* Freescale Semiconductor, Inc.

Here we report on surface topography and tunneling current characteristics of atomic layer deposited hafnium based dielectric (HfO_2, $Hf_xZr_{1-x}O_2$ and $Hf_xTi_yO_z$) films with different processing conditions. The process conditions explored here are: dielectric deposition temperature, post deposition anneal, with and without capping layers for the dielectric during annealing. Atomic force microscopy (AFM) was used to characterize the surface morphology. Conducting AFM (C-AFM) provided the unique capability to characterize the film uniformity by measuring the spatial distribution of the tunneling current through the film. X-ray diffraction (XRD), transmission electron microscopy (TEM) and electrical measurements were also used for the understanding of the film properties. With optimized Ti or Zr ratios, the roughness of the dielectric films is significantly improved and resulted in smaller and more uniform grain size distribution. The addition of Ti or Zr resulted in improved uniformity of tunneling current distribution. However, without a cap layer, significant re-crystallization and roughing were still observed upon 1000°C annealing. This resulted in significant leakage at grain boundaries as revealed by C-AFM images. Adding a metal capping layer prior to annealing greatly improved the stability of the films with only minor increase in surface roughness compared to as-deposited films. Films capped with metal during annealing showed dramatically improved leakage characteristics by eliminating most of the apparent grain boundaries and by improvement of overall film roughness. With the optimized Ti or Zr ratio and metal cap during annealing, better electrical characteristics were achieved based on C-V measurements.

EM-ThP44 Dependence of the Nitrogen Depth Profile on Annealing In HfSiON/SiON/Si(001) Ultrathin Films, ***A. Herrera-Gomez,*** University of Texas at Dallas and CINVESTAV-Queretaro, Mexico*; F.S. Aguirre-Tostado, G. Pant,* University of Texas at Dallas*; M.A. Quevedo-Lopez, P.D. Kirsch,* SEMATECH*; B.E. Gnade, R.M. Wallace,* University of Texas at Dallas

The chemical depth profile of nitrided hafnium silicate dielectric films has been the subject of many studies. Properties such as channel peak mobility and crystallinity depend on the distribution of the nitrogen content. The stoichiometry of hafnium silicate films deposited on a thin layer of silicon oxide was studied with angle resolved x-ray photoelectron spectroscopy (ARXPS). Through a self consistent analysis it was possible to determine the influence of rapid thermal annealing on the compositional depth profile of the film. Upon nitridation, the nitrogen was distributed throughout the films. However, after rapid thermal annealing the N left the hafnium oxide layer and diffused into the underlying silicon oxide layer. Also discussed are important issues regarding the extraction of quantitative information from ARXPS data, such as a proper characterization of the beam shape and analyzer focus area.

EM-ThP45 Electrical and Chemical Analyses of $SrTiO_3/Y_2O_3$ MIM Capacitors, ***C. Vallee***, *M. Kahn, E. Defay, C. Dubourdieu, M. Bonvalot, O. Joubert,* LTM/CNRS, France

The voltage linearity of MIM capacitors is usually described by the following equation: $\Delta C/C$ = (C(V)-C0)/C0 = ?V2 + ?V , where C0 is the capacitance value at zero applied voltage, and ? and ? are the quadratic and linear coefficients of the capacitance. According to ITRS specifications, ? must be less than 100 ppm/V2 for RF bypass devices and ? should be as small as possible. As of this date, none of the dielectric materials put on trial for MIM applications shows acceptable voltage linearity with high capacitance density value, their C(V) curve having either a positive or a negative bending. An experimental strategy consists in elaborating bi-layer of dielectric materials exhibiting opposite voltage linearity behaviour. By tuning the thickness of these two dielectrics with respect to each other, we expect to adjust their relative contribution to the overall ? value. Thus, perfectly stable capacitance density values should be observed with varying

applied voltage. In this study, SrTiO3 (STO)-Y2O3 bilayer MIM capacitors are developed. Indeed, STO and Y2O3 show respectively negative and positive ?. STO layers with several thicknesses have been prepared by dual ion beam scattering (DIBS) on Pt/TiO2/SiO2/Si stacks. A post deposition annealing treatment is carried out in order to induce crystallisation. Y2O3 layers are deposited by pulsed injection PE-MOCVD. Metal-dielectric and dielectric-dielectric interfaces are analyzed by XPS, XRR and SE in the FUV range. These dielectrics are then electrically characterized by C(V) measurements with gold electrodes in order to extract ? values and to estimate the overall dielectric constant.

EM-ThP46 Nitrogen Incorporation in Hf-based High-k Dielectrics Upon Thermal and Plasma Treatments*, **F.S. Aguirre-Tostado,*** University of Texas at Dallas*; A. Herrera-Gomez,* University of Texas at Dallas and Cinvestav-Qro, Mexico*; M.J. Kim, B.E. Gnade, R.M. Wallace,* University of Texas at Dallas*; M.A. Quevedo-Lopez,* Texas Instruments assignee at SEMATECH*; P.D. Kirsch,* IBM assignee at SEMATECH

Nitridation of SiO@sub 2@ has been demonstrated to increase the dielectric constant allowing for further scaling in conventional CMOS fabrication. The same applies for Hf-based high-k dielectrics such as HfSiO and HfO@sub 2@. For HfO@sub 2@, nitrogen incorporation helps to suppress crystallization after high temperature activation anneals. In this work we systematically study the incorporation of nitrogen in HfSiO and HfO@sub 2@ using plasma assisted nitridation and thermal treatments in ammonia. The nitrogen concentration and chemical interactions are studied using x-ray photoelectron spectroscopy, x-ray diffraction, and high-resolution transmission electron microscopy. The role of nitrogen on the electrical properties is also discussed.

EM-ThP47 Cyclic Chemical Vapor Deposition of TiAlO Ultra-Thin Films*, **X. Song**, C.G. Takoudis,* University of Illinois at Chicago

Cyclic-chemical vapor deposited TiAlO films, a few nanometers-thick, were prepared on H-passivated Si substrates using trimethyl Aluminum (TMA), tetrakis(diethylamino)titanium (TDEAT) and O@sub 2@. The depositions were carried out in a low pressure chemical vapor deposition chamber. The reaction pressure was on the order of 1 Torr and the reaction temperature was 300°C. The film thickness was probed using spectroellipsometry. The surface roughness of both as-deposited and annealed films were measured with atomic force microscopy (AFM). Rutherford backscattering spectroscopy (RBS) was utilized for the composition analysis. The atomic compositions and interfacial reactions were probed using x-ray photoelectron spectroscopy (XPS). The morphology of the films was analyzed using x-ray diffraction (XRD). Our studies show that the properties of TiO@sub 2@ are improved even with the addition of a few percent of Al@sub 2@O@sub 3@. XRD analyses indicate that as-deposited TiAlO films have amorphous structure. Upon annealing the as-deposited film in Ar at 500°C for 5 min, the film still maintains amorphous character, while TiO@sub 2@ crystallizes at these conditions. The surface of TiAlO films is found to be smoother than that of TiO@sub 2@. Sample annealing increases the roughness of the TiAlO films but the film roughness is still much lower than that of as-deposited TiO@sub 2@ films. There is no detectable formation of interfacial silicon oxide in as-deposited TiAlO films, based on XPS analyses. The thermal stability of TiAlO is also studied at different Ti contents. The carbon absence in the RBS analyses indicates that carbon (detected by XPS) is contamination on the sample surface most likely from the ambient. Electrical characterization of the TiAlO films will also be discussed.

EM-ThP48 Preparation of Yttrium and Aluminum Oxide Thin Films through Supercritical Carbon Dioxide Assisted Deposition*, **Z. Chen**, T. Gougousi,* UMBC

Aluminum and yttrium oxide thin films were deposited on silicon at low temperatures (<150°C) through a chemical route, where the metal-organic precursors and oxidizing agents were delivered in liquid and supercritical carbon dioxide. Aluminum acetylacetonate (99%) (Al(acac)@sub3@), aluminum hexafluoroacetyl-acetonate (min. 98%) (Al(hfac)@sub3@), and tris(2,2,6,6-tetramethyl-3,5-heptanedionato) yttrium(III), (98+%, 99.9%-Y) (Y(tmhd)@sub3@) were used as precursors and a 30% aqueous solution of hydrogen peroxide, tert-butyl peroxide, and di-tert-amyl peroxide as oxidants. Depositions were carried out in a hot wall reactor at pressures ranging from 2100 to 3500 psi at 70-140°C. The deposited thin films were investigated by using X-ray photoelectron spectroscopy (XPS) and transmission Fourier transform infrared spectroscopy (FTIR). XPS and FTIR results indicated the formation of metal oxides thin films with some bonded carbon present in the film. Substitution of the aqueous hydrogen peroxide solution by the organic peroxides resulted in substantially lower OH and carbonate content in the films. For Al@sub2@O@sub3@ deposition from Al(acac)@sub3@ and tert butyl peroxide a very narrow temperature window (110 -120°C) existed for film formation. However, for Y@sub2@O@sub3@ deposition from Y(tmhd)@sub3@ and the same oxidant we find a much broader deposition window ranging from 80 to 130°C. The results demonstrate the feasibility of the technique for the deposition of metal oxide films.

EM-ThP49 Influence of the Bottom Electrode Material in Y@sub 2@O@sub 3@ MIM Capacitors*, **M. Bonvalot**, M. Kahn, C. Vallee, J. Ducote, O. Joubert,* LTM/CNRS, France

High quality MIM capacitors are seeing increased use in CMOS, BICMOS and bipolar chips. The economic demand for smaller devices directly leads to the request for higher MIM charge storage densities. Therefore new high @kappa@ dielectric materials, such as Al@sub 2@O@sub 3@, Ta@sub 2@O@sub 5@ and HfO@sub 2@, are being evaluated as MIM dielectrics and will be used in future applications. Nevertheless, most of these materials show very large variations of their capacitance with applied bias voltage (so-called voltage linearity, characterized by a quadratic coefficient - alpha); thus, they cannot be used for analog MIM applications. TiN/Y@sub 2@O@sub 3@/Au capacitors have already been investigated. They exhibit good electrical properties with large breakdown electrical field values (7-8 MV/cm), low leakage currents, and a capacitance density of 5 fF/µm@super 2@. The Y@sub 2@O@sub 3@ is grown by pulsed liquid injection MOCVD. The aim of the present work is to study the impact of the bottom electrode materials on the interfacial layer between the metal and the yttrium oxide and hence, on the MIM electrical properties (C(V) and I(V) characterizations). Several electrode materials will be put on trial, such as WSi@sub x@(x=1, 2, 3), Ni and Pt. Their influence on the interface will be chemically characterized by means of XPS, SE in the FUV-visible range (up to 8 eV), and SIMS. The electrical behavior C(V) will be analyzed based on the work function of the metal electrode and on the nature of the interface with Y@sub 2@O@sub 3@.

EM-ThP50 Synthesis and Dielectric Characteristics of Poly Paraxylene-C Thin Films*, P. Tewari, M.T. Lanagan,* Pennsylvania State University*; **G. Sethi**,* Pennsylvania State University, US

Poly paraxylene-C thin films are particularly useful in both biomedical and electronic applications. In the current work the synthesis and electrical properties of Poly paraxylene-C (parylene-C) thin films were investigated. Parylene-C has high breakdown strength and dielectric constant of 2.8. Parylene-C thin film were deposited by pyrolitic vapor decomposition of substituted paraxylene, followed by its polymerization on metallic substrates. During the deposition, base pressure was maintained at 21mtorr while evaporator and pyrolysis furnaces were maintained at 160°C and 690°C respectively. Crystallinity of Paralyne-C thin films was analyzed with the variation of pressure in deposition chamber. Reduction in chamber pressure has shown to improve film morphology. Dielectric constant and dissipation factor variation with temperature and frequency were analyzed with LCR meter and impedance gain phase analyzer. 1µm thick parylene thin film were shown to have a dielectric constant of 3.1 at frequency of 1MHz and room temperature. A dielectric relaxation following Maxwell- Wagner behavior was noticed around 20KHz frequency. Current-voltage characteristic was analyzed to distinguish between regions of Ohmic and non-Ohmic conduction. Deposited Parylene-C thin film will be used to analyze interfacial effects in multilayer Parylene-C - Silica laminar structures.

EM-ThP51 Chemical Structure of the Bilayer Ag/Li@sub 2@O Cathode Interface in Organic Light-Emitting Diodes*, **M.H. Joo**,* LG Electronics Institute of Technology, South Korea, Korea (South)*; M.K. Baik, J.K. Choi,* LG Electronics Institute of Technology, South Korea

The chemical structure of the interface between Ag with Li2O and tri (8-hydroxyquinoline) aluminum (Alq) was investigated by using in-situ characterization of x-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS). Li2O on Ag had lower barrier height than LiF on Ag. XPS and UPS results show the interaction between Li2O and Alq leads to gap state formation in HOMO of Alq.

EM-ThP52 Thickness Dependence of High Capacitance-Gate Dielectric Layer on Electrical, Structural Characteristics and OTFT Device Performance*, **C.S. Kim**, H.K. Baik,* Yonsei University, South Korea

In this study, pentacene TFTs operating at low voltage (-2V) were successfully fabricated using the CeO2-SiO2 dielectric layer with optimum thickness. The field effect mobility and on/off current ratio, at operating voltage of -2V, were 0.97cm2/Vs and 10^4, respectively. Threshold voltage

and subthreshold slope were -0.4V and 0.58V/dec, respectively. We have also shown the correlation of surface morphology and leakage current density. In the thick films, the leakage current is not bulk limited but rather it depends on the surface roughness, which increases with film thickness. The realization of low voltage and low leakage devices make the OTFTs excellent candidates for future flexible display and electronics applications.

EM-ThP53 Luminescence Properties of Organic Light Emitting Diodes using Chemical Mechanical Polishing Process, ***G.-W. Choi***, *W.-S. Lee,* Chosun University, Korea; *Y.J. Seo,* Daebul University, Korea, South Korea; *P.-G. Jung,* Chosun University, Korea

Indium tin oxide thin film has attracted intensive interest because of their unique characteristics of good conductivity, high optical transmittance over the visible wavelength region, excellent adhesion to the substrate, stable chemical properties and easy patterning ability. ITO thin films have found many applications in solar battery, illuminators, optical switches, liquid crystal displays, plasma display panels, and organic light emitting displays. However, some problems such as peaks, bumps, large particles, and pin-holes on the surface of ITO thin film were reported, which caused the destruction of color quality, the reduction of device life time, and short-circuit. The interface between the electrode and organic layer in OLEDs has been reported as an important factor to influence the electrical and luminescent properties. Chemical mechanical polishing (CMP) process is one of the suitable solutions, which could solve the above-mentioned problems. In this work, we report the effect of polished ITO surface on the luminescent performance of the OLEDs. This work was supported by a Korea Research Foundation grant (KRF-2004-005-D00007).

EM-ThP54 Electrical Properties of Organic Light Emitting Diodes by Indium Tin Oxide-Chemical Mechanical Polishing Process, *G.-W. Choi,* ***W.-S. Lee,*** Chosun University, Korea; *Y.J. Seo,* Daebul University, Korea, South Korea; *Y.-K. Jun,* Chosun University, Korea

Indium tin oxide (ITO) thin film is a transparent electrode, which is widely applied to solar battery, illuminators, optical switches, liquid crystal displays (LCDs), plasma display panels (PDPs), and organic light emitting displays (OLEDs) due to its easy formation on glass substrates, good optical transmittance, and good conductivity. However, some problems such as peaks, bumps, large particles, and pin-holes on the surface of ITO thin film were reported, which caused the destruction of color quality, the reduction of device life time, and short-circuit. Chemical mechanical polishing (CMP) process is one of the suitable solutions, which could solve the problems. CMP performances can be optimized by several CMP components such as equipment and consumables. In this study, the optimum process parameters and the influences of process parameters were investigated for ITO-CMP with the sufficient removal rate and the good planarity. In this work, we studied the electrical characteristics of OLED with the structure of glass/ITO/MEH-PPV/Al using polished ITO surface as a bottom electrode (anode). And then, the optical property such as transmittance and absorption efficiency were discussed in order to evaluate the possibility of CMP application for ITO film.

EM-ThP55 Strongly Enhanced Thermal Stability of Crystalline Organic Thin Films Induced by Aluminum Oxide Capping Layers, ***S. Sellner***, *A. Gerlach, F. Schreiber,* Universit@um a@t T@um u@bingen, Germany; *M. Kelsch, N. Kasper, H. Dosch,* Max-Planck-Institut f@um u@r Metallforschung, Germany; *S. Meyer, J. Pflaum, M. Fischer, B. Gompf,* Universit@um a@t Stuttgart, Germany

We present a detailed study of the strongly enhanced thermal stability of organic thin films of diindenoperylene encapsulated by sputtered aluminum oxide layers. We study the influence of capping layer thickness, stoichiometry, and heating rate on the thermal stability of capped films and their eventual breakdown. Under optimized encapsulation conditions (thick and stoichiometric capping layer), the organic films desorb only at temperatures 200 Â°C above the desorption of the uncapped film. Moreover, the capped organic films retain their crystalline order at these elevated temperatures, whereas they would normally (i.e., uncapped) be in the gas phase. This study therefore also shows a way of studying organic materials under temperature conditions normally inaccessible. Considering results from complementary techniques, we discuss possible scenarios for the eventual breakdown. The results have implications for the performance and long-term stability of organic devices for which stability against elevated temperatures as well as against exposure to ambient gases is crucial. @FootnoteText@ S. Sellner et al., J. Mater. Res. 21 (2006) 455. S. Sellner et al., Adv. Mater. 16 (2004) 1750.

EM-ThP57 Sol-Gel Derived SiO2-TiO2 Dielectric Layer for Organic Thin Film Transistor, ***S.W. Lee,*** *H.K. Baik,* Yonsei University, South Korea

Solution processible gate dielectric using SiO2-TiO2 composite oxide were prepared by sol-gel method for OTFT application. The composition, crystal structure, bonding configuration and electrical properties of SiO2-TiO2 composite oxide were analyzed using X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectroscopy (FTIR) and current-voltage (I-V) measurement. Si/Ti ratio was 1:1 and annealing temperature was 300^C. Dielectric constant around 8 was obtained by capacitance-voltage measurement. The modification of microstructure and chemical bonding configuration in the SiO2-TiO2 film by the annealing temperature and its influence on electrical properties are discussed. We have fabricated OTFT device using SiO2-TiO2 composite oxide as a dielectric layer. Electrical properties of OTFT show that solution processible dielectric layer produce almost same results as vacuum process. We expect this process can replace conventional vacuum process due to its simplicity and low price consumption.

EM-ThP58 Plasma Treatment Effects on the Device Performance of Organic Thin Film Transistors, ***S.J. Jo,*** *C.S. Kim, S.W. Lee, H.K. Baik,* Yonsei University, Korea

We investigated electronic effects of plasma treatment on device properties of pentacene based thin film transistors (TFTs) with ITO (indium-tin-oxide) source and drain electrodes. The treated ITO electrodes were investigated by both contact angle measurements and X-ray photoelectron spectroscopy (XPS). The TFTs with plasma treated ITO electrodes show significantly improved performance over the devices without plasma treated ITO. The plasma treatment of the ITO surface improved the TFT performance by enhancing the hole injections from the electrode. The change in performance was attributed to the removal of contaminants and to the change in work function of ITO.

EM-ThP59 Synthesis, Characterization, and Properties of Flexible Side-Chain-Containing Polyimides, ***C.-L. Cheng,*** Chung-Yuan University, Taiwan; *L. Wang,* National Taiwan University

Aromatic polyimides have found a wide range of applications in advanced aerospace, automobile, microelectronic and printed circuit industries because of their distinguished thermal stability, high chemical resistance, good mechanical strength and excellent dielectric properties. However, conventional polyimides are often categorized as an insoluble, intractable, and infusible material owing to their rigid backbone structure. These disadvantages make them extremely difficult to process and greatly limit their commercial uses. Various attempts have been developed to overcome these deficiencies, including the use of noncoplanar or alicyclic monomers and the introduction of flexible segments into the polymer backbone. The strategies of these methods are the reduction of chain crystallinity, inter-molecular charge-transfer and electronic polarization interactions. An alternate successful approach involves the incorporation of pendant groups onto the rigid polyimide backbone. These works have shown that the presence of bulky groups could effectively prevent the coplanarity of aromatic rings and reduce the packing efficiency of molecular chains without sacrificing thermal properties. In this study, we synthesized two series of polyimides containing alkyl side groups in different sizes and investigated the effect of the molecular structure of pendant groups on the thermal and dielectric properties of polyimides.

EM-ThP61 Jet-printed Organic Electronics: Display Backplanes without Vacuum Processing, ***J.H. Daniel,*** *A.C. Arias, B. Krusor, R.A. Street,* Palo Alto Research Center

Most electronic circuit fabrication relies on vacuum tools for the deposition or removal of materials. In large-area electronics, particularly for active-matrix display backplanes, these vacuum tools represent a considerably increased engineering challenge due the growing substrate size and the requirements on uniformity. Moreover, the capital cost is substantial. With the development of new materials, solution-based processes are being studied which will potentially enable extremely low-cost large-area electronics on flexible substrates. We are investigating low-temperature (<150degC) all-additive processes for the fabrication of flexible active matrix thin-film transistor (TFT) backplanes. The metal conductors for gate/data lines and pixel pads are defined by jet-printing of silver nano-particle solutions. The active regions of the TFTs consist of jet-printed polymeric semiconductor (PQT-12). Various polymeric gate dielectrics were investigated, including the epoxy SU-8. SU-8 strongly cross-links at temperatures below 150 degC making it chemically inert to subsequent processing steps and the surface energy of SU-8 is compatible with the printing solution to form narrow continuous lines. We were able to coat

SU-8 layers with a thickness around 200-300nm with low pin-hole density. Pixel circuits were printed on rigid and flexible substrates. The transistor performance was measured and the pixel response was determined using a picoprobe. When combined with our reflective electrophoretic display media these all-printed backplanes are promising for electronic paper or signage applications.

EM-ThP62 An Improved Method for the Derivation of Depth Profile Information from Angle Resolved XPS Data*, P. Mack*, *R.G. White,* Thermo Electron Corporation, UK*; T. Conard,* IMEC, Belgium

The construction of depth profiles from angle resolved XPS (ARXPS) data is currently receiving much attention. This is mainly due to the increasing technological importance of layers whose thickness is of the order of a few nanometres. Transistor gate dielectric layers and self-assembled monolayers are good examples of such layers. The construction of profiles from ARXPS data can be accomplished using methods involving maximum entropy but there are limits to the accuracy and repeatability of these methods if used in isolation. In this paper, we will show that the quality of the profiles can be improved by making use of additional, readily available, information. For example, the composition of the substrate is usually known as is the oxidation state of the elements in the thin film because these are available from the XPS spectrum. This information can be used to refine the profiles derived using maximum entropy thus improving the reliability of the result. The method will be described in detail and illustrated by reference to layers of nitrided hafnium oxide on silicon. The nitrogen profiles obtained using this method will be compared with those derived from other experimental techniques.

EM-ThP63 An Investigation of Thermal Management in Laser Diode Structures*, D. Roberts*, *G. Triplett,* University of Missouri-Columbia

As electronic device feature sizes decrease to several nanometers, the ability to effectively remove heat through the packaging remains a technical challenge. Thermal management issues in electronic systems have been a limiting factor for high-power as well as optoelectronic device applications. In optoelectronic applications, thermal issues dramatically affect device operation, particularly in laser diodes. The active region in laser diodes (which can be several microns thick) are particularly sensitive to heat as it pertains to the lasing threshold because of large injection current density. Whereas larger bandgap materials are less temperature dependent, they are inappropriate for optical-fiber applications. This large injection current density also results in shorter device lifetimes. Current heat removal techniques involve fluidic cooling, epi-down packaging, and thermoelectric coolers. These techniques have several advantages; however, certain limitations exist with these solutions. The ability to effectively remove heat at a rate that supports higher-power (~1kW/cm@super2@) operation remains a technical barrier. Our approach is to focus on the substrate for heat removal. In their current form, substrates lack the thermal conductivity required to deal with these operating conditions. In this paper we will discuss thermal management issues in laser diodes and discuss an additional approach to device cooling via substrate manipulation. This approach will involve neutron transmutation doping (NTD) to reconfigure the substrate properties.

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