Thursday Morning, November 16, 2006

Electronic Materials and Processing
Room 2003 - Session EM+AS-ThM

High-k Dielectric Characterization

Moderator: A. Rockett, University of Illinois, Urbana-Champaign

8:00am **EM+AS-ThM1 A Study of High Dielectric Constant Magnesium Oxide Film Interfaces with Si***, **L. Yan**, R.P. Shrestha, E.A. Irene,* University of North Carolina-Chapel Hill*; L. Zhong, I. Kim, O. Auciello,* Argonne National Lab

In a recent report we have identified MgO as a potential high dielectric constant (@Kappa@) gate dielectric because of its chemical inertness enabling sharp interfaces and wide band-gap (7.3 eV) for large band offsets with silicon (Si) to minimize leakage. Our prior investigation of reactively sputtered MgO on Si revealed impressive interfacial electronic properties as compared with the conventional SiO@sub 2@/Si, in particular comparable interface trap densities (D@sub it@). The present study is aimed at a closer exploration of MgO thin films, prepared using two different oxidizing agents: molecular and atomic oxygen on reactively sputtered Mg. In situ XPS, Mass Spectrometry of Recoiled Ions (MSRI) and spectroscopic ellipsometry (SE) were used to monitor the evolution of the interfaces with MgO. This, coupled with post-deposition, ex situ cross-sectional TEM, provided an accurate materials description of the MgO/Si interface. Electronic measurements, including capacitance versus voltage (C-V), conductance (G(@omega@)) versus gate voltage (G(@omega@)-V), and current flux versus electric field (J-E), were conducted on capacitor structures to determine @Kappa@, D@sub it@, and leakage current, respectively. Our results show that thin MgO films can provide a superior high-@Kappa@ dielectric for many electronic applications. This work is supported by the National Science Foundation (NSF) Materials Research Division.

8:20am **EM+AS-ThM2 Channel Drift Mobility in High-k Transistors from Galvanomagnetic Measurements***, **R.T. Bate**, W.P. Kirk, R. Agrawal,* University of Texas at Arlington*; R.M. Wallace, B.E. Gnade, G. Pant,* University of Texas at Dallas

Effective mobility µ@sub eff@ in high-k transistors can be degraded by enhanced scattering of carriers and by trapping. The drain current is proportional to the product of the channel carrier density n and the drift mobility µ, and the capacitance measurement used to determine channel carrier density cannot distinguish between free and trapped charge. The result is that trapping can cause µ@sub eff@ to underestimate µ. We combine Hall effect and magnetoresistance (MR) measurements to determine µ of carriers in the channel. Then effective mobility reductions due to increased scattering can be separated from loss of carriers due to trapping. In the past, Hall effect measurements have been used to measure Hall mobility in MOSFET and MISFET channels, and µ has been estimated by making assumptions about the magnitude of the Hall factor r@sub H@ which is the dimensionless ratio of the Hall mobility to the drift mobility, (i.e. r@sub H@ = µ@sub H@/µ). r@sub H@ is usually assumed to be close to unity. Theory indicates that r@sub H@ is strongly dependent on the type of carrier scattering in the channel, which is usually not known a priori. This uncertainty is currently the main drawback of the Hall effect as a means of determining channel drift mobility. We propose to use the MR to estimate r@sub H@ . Analysis based on the silicon 100 inversion layer shows that the MR is strongly correlated with r@sub H@, regardless of the scattering mechanism. This is being experimentally verified on MOSFET structures where r@sub H@ and µ can be independently determined, and the results are being carried over to high-k MISFETs. Knowing r@sub H@ permits µ to be estimated, not only from Hall measurements, but also, for routine diagnosis, from MR measurements on conventional transistors (not Hall devices), even in the presence of significant trapping. @FootnoteText@ Partial support by Texas Advanced Technology Program of THECB #003656-0029-2003.

8:40am **EM+AS-ThM3 Interface Composition and Band Alignment in Nano-electronics***, S. Rangan, E. Bersch, R.A. Bartynski, L.V. Goncharova, T. Gustafsson, **E. Garfunkel**,* Rutgers University **INVITED**

We outline some key issues relevant to characterization of interfaces in next-generation highly-scaled CMOS devices. Selected experimental results as well as conceptual approaches to addressing the structure, bonding and band alignment problems will be discussed. The semiconductor/high-K and high-K/metal interfaces will be the primary focus of the discussion. Ion scattering, photoemission, inverse photoemission, electron microscopy, and other methods have been used to examine (i) amorphous high-K gate dielectrics and their interfaces on Si, Ge and GaAs, (ii) epitaxial oxides on Si, and (iii) metal-dielectric interfaces for gate metallization. From a comparison of experimental and theoretical results we are able to develop a better understand the electronic properties of the different structures. We find that the band gap, barrier height and dielectric response of this class of materials are very phase-dependent. An understanding and control of band alignment for charge injection and carrier confinement must be realized if novel materials are to be incorporated in future nano-electronic devices.

9:20am **EM+AS-ThM5 Band Offsets Measurements of Metal/High-k/Semiconductor Structures***, **S. Rangan**, E. Bersch, R.A. Bartynski, E. Garfunkel,* Rutgers University

The study of high-k dielectrics and metal gate electrodes has been ongoing in order to thoroughly understand the properties of these materials and to contribute to their implementation in Metal/Oxide/Semiconductor Field Effect Transistors. The band offsets are an important property of Metal/Oxide/Semiconductor (MOS) stacks in that the leakage current depends directly on them. An understanding of the band offsets, particularly the role played by the interface dipole, may enable the development of tunable band offsets at the interfaces. We have used in situ photoemission and inverse photoemission as well as synchrotron photoemission to measure the band offsets between the layers of MOS stacks. UV, X-ray, and inverse photoemissions give us a direct measurement of the bandgap of the dielectric and offsets between dielectric and semiconductor bands. With sequential metallization (Al, Ru, Ti) shifts of the band edges are measured as a function of metal coverage. The band offsets we measure for the metal/oxide and oxide/semiconductor interfaces are, to first order, in good agreement with the modified Schottky Mott model which treats the interface with bare bulk (metal, oxide or semiconductor) properties. But as expected, photoemission reveals much more complicated interfaces, and in particular strong effects on the chemistry of the entire stacks upon metal deposition. We report here the energy gap and band offsets of several HfxSi1-xO2 oxides on a Si substrate, as well as the effect of Ru (high work function metal) and Al (low workfunction metal) deposition on theses dielectrics. Both Ru and Al induce an energy shift of the core levels (Hf4f, Si2p), the valence and conduction bands â?" the shift depends both on the oxide and on the metal choice. Ru stays metallic upon deposition on the oxide, whereas Al is shown to be oxidized even at room temperature. We will show that the source of oxygen can be the dielectric or the interface layer between the substrate and the oxide.

9:40am **EM+AS-ThM6 A Soft-X-Ray Photoelectron Spectroscopy Study of D-State Contributions to Valence Band States in Nanocrystalline HfO2, TiO2, and Hf1-xTixO2 Alloys***, **L.B. Fleming**, M.D. Ulrich,* NC State University*; J. Rowe,* University of North Carolina at Chapel Hill*; C.C. Fulton, G. Lucovsky,* NC State University

This paper compares d-state contributions to valence band, and valence band edge defect states determined from i) synchrotron soft x-ray photoelectron spectroscopy (SXPS) at photon energies between 40 and 80 eV, with d-state contributions determined from ii) ultra-violet photoemission spectroscopy (UPS) at 21.2 eV. Measurements have been performed on thin films of HfO@sub 2@, TiO@sub 2@ and Hf@sub 1-x@Ti@sub x@O@sub 2@ alloys prepared by reactive evaporation, and subjected to post deposition annealing at 700°C. The atomic Hf, Ti and O contributions to the valence band states in the SXPS and UPS spectra are at approximately the same energies with respect to the Fermi level, but have different spectral weighting. The only significant differences in the USP and SXPS spectra are defect state features at, and above the valence band edge. The UPS spectra, limited by the incident photon energy, yield a single feature with a spectral peak ~1 eV above the valence edge, whereas SXPS spectra, performed with higher incident photon energies can defect electronic states deeper into the forbidden band gap. The SXPS spectra confirm the band edge features, as well as identifying a second defect states at higher energy, ~3 eV above the valence band edge. The defect states in TiO@sub 2@, and the alloys are interpreted in as O-atom vacancy states in which the formal valence of Ti is 3+ rather than 4+. This assignment is based on comparisons between SXPS spectra, and epsilon 2 spectra obtained from analysis of reflection spectra of Ti@sub 2@O@sub 3@ over a spectra range from 0.01 eV to 10 eV. Defect states in HfO@sub 2@ are similar, and assigned to d-states of Hf@super 3+@ at O-atom vacancies.

10:00am **EM+AS-ThM7 Line-Width and Symmetry Changes in Jahn Teller Term-Split Sc 3d-States in LaScO3 as a Function of Deposition and Annealing Temperatures***, **H. Seo**,* NC State University*; L.F. Edge, D.G. Schlom,* Penn State University*; N.A. Stoute, G. Lucovsky,* NC State University

$LaScO_3$ conduction band states are derived in part from Jahn-Teller-split Sc 3d-states in distorted octahedral arrangements of O-neighbors. Conventional XRD for films deposited at ~300°C, and annealed to 700°C display no evidence for crystallinity, while films annealed to >800°C display strong crystalline features. New studies of conduction band states by i) vacuum ultra-violet spectroscopic ellipsometry (VUV SE), and ii) x-ray absorption spectra (XAS) for transitions from (a) spin-orbit split Sc 2p core states (Sc $L_{2,3}$) and (b) the O 1s core state (O K_1), are compared, providing insights into scales of order. XRD results are indicative of grain sizes >5 nm for >800°C anneals, but do not distinguish between i) amorphous films, and ii) nanocrystalline films with grain sizes

10:20am **EM+AS-ThM8 Trends in Core Level Binding Energies of Mixed Oxide Candidates for High-κ Dielectrics***, **A. Mathew**,* University of Delaware*; L. Bao,* Dupont Inc.*; K. Demirkan,* University of Delaware*; C.-G. Wang, G.D. Wilk,* ASM America Inc.*; R.L. Opila,* University of Delaware

Hafnium silicates and lanthanum aluminates are among the many proposed candidate materials for replacing the SiO_2 gate dielectric in transistors for low standby power applications. Photoelectron spectroscopy with its sensitivity to local chemical bonding is an invaluable tool for investigating these interfaces. Hafnium silicates were deposited using Atomic Layer Chemical Vapor Deposition (ALCVD^{TM}), and the lanthanum aluminates were sputter deposited. Systematic trends in core level binding energies are observed for the unannealed mixed oxide systems as a function of composition. The degree to which such shifts occur is seen to be a function of both the amount of charge transfer between the component cations as well as the local lattice potential, both initial state effects. The O 1s photoemission peak and the N 1s peak (in the case of nitrided films) reflects the local bonding environment in the film, and its variations with different concentrations of a number of cations are studied as well. The O 1s and N 1s peaks can be deconvoluted into components arising from its bonding with a higher or lower electronegativity cation, and their relative intensities vary with composition. These insights into the local bonding structure are important for improving our capability to engineer the ideal semiconductor / high-κ interface for optimal device performance.

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