Manufacturing Science and Technology
Room 207 - Session MS-TuA

Advanced Manufacturing Processes for Silicon Devices
Moderator: A.C. Diebold, SEMATECH

2:00pm **MS-TuA1 Magnetoresistive Random Access Memory - Manufacturing Challenges**, ***G.W. Grynkewich***, *B. Butcher, J. Chan, W. Feil, G. Kerszykowski, K. Kyler, J. Martin, J. Molla, K. Nagel, J. Ren, K. Smith, J.-J. Sun, R. Williams,* Freescale Semiconductor, Inc. **INVITED**

Magnetoresistive random access memory (MRAM) combines a magnetic tunnel junction (MTJ) with standard silicon-based CMOS to provide a unique combination of high speed read and write, non-volatility, and unlimited read and write endurance. We have produced the world's first commercially viable MRAM circuits. After a brief description of the fundamentals of an MTJ-based MRAM, we will describe the manufacturing challenges associated with the volume production of high performance MRAM parts. These include: contamination control, bit patterning, achieving and maintaining uniformity of both very thin magnetic films and the tunnel barrier, formation of cladded programming lines, and processing very thin interlayer dielectrics.

2:40pm **MS-TuA3 Controlling Ultrashallow Junction Formation through Surface Chemistry**, ***E.G. Seebauer***, *K. Dev, C.T.M. Kwok, R.D. Braatz,* University of Illinois at Urbana-Champaign

Forming extremely shallow pn junctions with very low electrical resistance is becoming an insurmountable stumbling block to the continued scaling of microelectronic device performance according to Moore's Law. We have developed a technology based on surface chemistry that holds great promise for simultaneously reducing junction depth and increasing activation for dopants implanted into silicon. The approach uses the surface as a large controllable "sink" that removes Si interstitials selectively over dopant interstitials. We have discovered a new way to employ adsorption at the surface for this task: adjusting the intrinsic loss rate of interstitials to the surface. We control the interstitial loss rate to the surface by saturating dangling bonds using adsorbed nitrogen (introduced as ammonia) before implantation or the subsequent annealing step. To demonstrate such effects, we have measured SIMS profiles of isotopically labeled Si (mass 30) implanted into a Si host lattice depleted in this isotope, The annealed profiles with an atomically clean surface change relatively little from the as-implanted profile, while the profiles with adsorbed N change much more. We have quantified the loss rate of interstitials at the surface by measuring the annihilation probability, which varies from about 0.05 on atomically clean Si(100) to about 0.0008 with only 1% of a monolayer of adsorbed N.

3:00pm **MS-TuA4 Investigation of Boron Penetration through Poly Silicon Films**, ***X.-D. Wang***, *W. Fan, S. Phillips, J. Parker, S. Schauer,* Freescale Semiconductor

Poly-Si is the most commonly used gate material in modern VLSI fabrication. It is also widely used as mask layer for dopant implantation. Such a process has the advantage of reducing lithography steps, however, it requires tight control on film property in order to effectively block undesired implantation through the film to the substrate silicon. In this paper, we investigate an implant issue related to boron penetration through the poly-Si film. Plan view scanning capacitance microscopy (SCM) analysis was performed to examine MOSFET devices which failed due to short channel. SCM images directly revealed undesired boron penetration in CMOS channel region to be the root cause of the failure. It was found that the yield was related to poly-Si deposition conditions. Multiple analytical techniques, including SCM, second ion mass spectroscopy (SIMS) and, transmission electron microscopy (TEM) were used to characterize the severity of boron penetration as function of film deposition conditions, especially the deposition temperature. By correlating to TEM analysis, it was found that the boron penetration is closely related to the crystalline properties of the film and optimal film growth parameters were obtained.

3:20pm **MS-TuA5 Investigation of Low-k Dielectric Etching using Groovy ICP Plasma Source**, *A. Kelly,* ***G.K. Vinogradov***, FOI Corporation, Japan

Plasma etching of low-k dielectric materials, such as porous materials is presenting significant challenges to their introduction in copper dual damascene device production. Plasma damage is implicated in poor retention of low-k properties. We investigated plasma damage using a narrow gap inductive plasma source, Groovy ICP. Specially developed for 300mm low-k dielectric etching, it has three independently controllable highly efficient RF coils immersed in separate grooves machined in a planar roof. Each groove generates its own plasma toroid, both radial plasma density and chemical uniformity can be optimized. We investigated sidewall damage in dual damascene stack structures over a wide pressure range for porous low-k dielectrics. Only under conditions of low pressure, 5-10mTorr and low ion energy can sidewall damage be eliminated. With separate wafer bias control of ion energy, we can distinguish between ion and radical effects on sidewall damage of low k materials. Damage is by radical attack penetrating into the sidewall; therefore low-pressure ion dominant conditions are needed. Also low ion energy is needed as high ion energy conditions can sputter damage sidewalls. Groovy ICP is capable of achieving these conditions in a narrow gap, typical for low residence time oxide etchers. This shows its unique applicability for low-k dielectric etching including oxide layers.

Manufacturing Science and Technology
Room Exhibit Hall C&D - Session MS-TuP

Topics in Advanced Manufacturing Poster Session

MS-TuP1 Dip-Pen Nanolithography-Based Fabrication of ZnO Microarrays, ***I. Takahiro***, *I. Kaoru, S. Nagahiro, T. Osamu,* Nagoya University, Japan

Zinc oxide (ZnO) becomes one of the most important functional materials with unique properties of the near UV emission, optical transparency, electrical conductivity, and surface acoustic wave. Microarrays and micropatterning of functional ceramic materials are expected to provide various applications for microcircuit fabrication. Patterning and arraying techniques are useful for arranging wiring electrode. Conventionally, ZnO micro-patterns and arrays are fabricated by etching with photoresist like the lithography technique for Si. However, it is difficult to find the suitable etching conditions. To overcome the issue, site-selective growth techniques were recently developed. Dip-pen nanolithography (DPN) is a new promising scanning probe-based technique for fabricating sub-100 nm to many micrometer structures on surfaces, since it is a simple method for directly depositing material from an ink-coated atomic force microscope (AFM) tip onto a substrate with a high spatial resolution. In this study, we demonstrate the fabrication of ZnO microarrays on Au through DPN. An oxidized silicon wafer was coated with a Ti adhesion layer via thermal evaporation, which was subsequently coated with Au. DPN was then used to array ZnO microstructures on these substrates with Zn(NO3)2 solution. AFM-probe used in this study was immersed into the solution for a few minutes. The microstructures of ZnO were observed with field emission scanning electron microscope (FE-SEM).

MS-TuP2 The Dependence of Power Trench MOSFET Processes on Wafer Thickness, ***M. Daggubati***, *G. Sim, D. Long, H. Paravi, Q. Wang,* Fairchild Semiconductor

The dependence of trench MOSFET processes on wafer thickness has been studied in detail. In the photolithography process, it was found that the photoresist thickness decreased 30Å when wafer thickness decreased from 675µm to 508µm. This is due to the fact that thinner wafer has less thermal dissipation time i.e. Thinner wafer dissipates heat better and heats up quicker than thicker wafer during baking resulting in more evaporation of the photoresist solvent. Unless compensated for, this change in resist thickness adds to process variation affecting critical dimension (CD) and trench depth control. In the silicidation process, after the rapid thermal processing (RTP), the thinner wafers exhibited a lower resistance and higher silicide stress of 3.23E+10 dynes/cm@super 2@ (compared to thick wafers of 4.60E+09 dynes/cm@super 2@) at the source contact due to the reasons mentioned above. Also, the stress is more uniform across the wafer. The Ti/Si reaction is time and temperature dependent. Higher temperature results in more silicide and the reaction creates a volume reduction that induces stress. The silicide layers on the Si wafers have been analyzed using Z-constrast imaging in transmission electron microscopy (TEM) and energy dispersive x-ray (EDX) profiling techniques. Both Z-contrast imaging and EDX profiling revealed a 50 nm thick TiSi layer on the top of TiSi@sub 2@ layer for the thicker wafers. Whereas, no TiSi layer was found in thinner wafers, but Ti-enrichment in the outer part was sometimes observed. The TiSi layer, especially when it's continuous, can modify the electrical property of the devices. The formation of TiSi layer could be attributed to insufficient Si atoms diffused to the outer layer. Higher temperatures in thinner wafers seem to assist in the removal of this TiSi layer.

MS-TuP5 Optimized Cu Electrochemical Plating considering Pattern Dependency in Dual-Damascene Process, ***H.-Y. Yoo***, Chung-Ang University, Korea*; N.-H. Kim,* Chosun University, Korea*; S.-Y. Kim,* DongbuAnam Semiconductor Inc.*; E.-G. Chang,* Chung-Ang University, Korea

Since damascene technology announced, Cu metallization using electrochemical plating (ECP) has played an important role in back end of line interconnect formation. In damascene process, the problems related with process integration as well as with each unit process are becoming critical issues. Occurrence of step height (SH) and array height (AH) after Cu plating was closely related with pattern dependencies in Cu ECP and influenced in Cu chemical mechanical polishing (CMP) process. So, Cu plating target thickness in Cu ECP process was required to be optimized. In this work, we studied the optimized copper thickness in Cu ECP. In order to select an optimized Cu ECP thickness, we examined Cu ECP bulge (bump, hump or over-plating amount), Cu CMP dishing and electrical properties of via hole and line trench over dual damascene patterned wafers split into different ECP Cu thickness. In the aspect of bump and dishing, the bulge increased according as target plating thickness decreased. Dishing of edge was larger than center of wafer. Also in case of electrical property, metal line resistance distribution became broad gradually according as Cu ECP thickness decreased. In the results, 0.6 @micron@ plating condition that baseline size reduced 40% showed bad property in broad resistance distribution of metal line and dishing after Cu CMP process. In conclusion, at least 20% reduced Cu ECP thickness from current baseline; 0.8 @micron@ and 1.0 @micron@ are suitable to be adopted as newly optimized Cu ECP thickness for local and intermediate layer. Acknowledgement : This work was supported by grant No. R01-2002-000-00375-0 from the Basic Research Program of the Korea Science Engineering Foundation.

MS-TuP7 Fabrication of High Precision Demultiplexer using Embossing Technique with Thermal Curable Polymers, ***C.H. Choi***, *M.W. Lee, B.H. O, S.G. Lee,* Inha University, Korea*; S.G. Park,* Inha University, Korea, Korea, Republic of*; E.H. Lee,* Inha University, Korea

Photonic devices have been fabricated mainly by using the conventional lithography and etch processes. However, the costs of the conventional fabrication were remained expensive, and obviously cannot meet the trend towards fiber-to-the-home (FTTH), which required lower price of the photonic components. Embossing technologies reduce the cost for the fabrication of photonic devices. In this paper, we fabricated a 1310 nm/1550 nm demultiplexer using an embossing technique with the PDMS mold. Resists used as the core and the cladding layers are ZP 51 and ZP 49, respectively, which are the thermal curable polymers. The fabrication process is summarized as: 1) manufacturing the photoresist master by lithography process, 2) forming the PDMS mold from the master, and 3) replicating the device using the mold. For the fabrication of the device, ZP 49 was spin coated onto a glass substrate, and was cured by heating. ZP 51 was applied to the patterned surface of the PDMS mold. This mold filled with the ZP 51 was then placed in contact with the surface of the prepared substrate coated the ZP 49, and the ZP 51 was cured to solid by heating it. After curing, the mold was peeled away carefully, and the upper cladding (ZP 49) was spin coated over the patterned structure. The fabrication of the demultiplexer was completed by curing. Some manufacturing issues, such as the variation of dimension of the replica, the durability of the mold, and optical properties of the device, will be discussed. The embossing technique is applied for low-cost manufacturing photonic devices.

MS-TuP8 Silicon Etch for Nano-photonic Structure using Hydrogen Silsesquioxane (HSQ) as a Direct Etch Mask, ***J.K. Kim***, *J.H. Sung, K.J. Lim, B.H. O,* Inha University, Korea*; S.G. Park,* Inha University, Korea, Korea, Republic of

As a typical etch process for a Si nano-structure of high aspect ratio requires a bilayer mask or a hard mask, we have investigated the use of a hydrogen silsesquioxane(HSQ) layer as a direct etch mask for Si structure. The HSQ is known as a negative tone e-beam resist good for nanosize patterning. It has attracted lots of attention in the semiconductor industry due to its low dielectric constant, easy processability, good planarization for surfaces, as well as excellent gap fill capability in deep submicron features. In our experiment, thin HSQ layer of 90 nm-thickness was tested as a direct Si etch mask for the etch of sub-micron size hole array of 280 nm in depth and 350 nm in hole-diameter. The etch selectivity of around 2.8:1 for Si to HSQ was obtained so far using SF6-based gas chemistry in our ICP system. The systematic variation of etch parameters were studied to improve the etched wall profile and surface roughness, and the optimized results will be discussed.

MS-TuP9 Mixed Oxidizer Effects on CMP (Chemical Mechanical Polishing) Performance of Nickel for MEMS, ***G.-W. Choi***, *N.-H. Kim,* Chosun Univ., Korea*; Y.-J. Seo,* Daebul Univ., Korea*; W.-S. Lee,* Chosun Univ., Korea

Micro electro mechanical system (MEMS) technologies are miniaturized systems which comprise sensor, actuators and electronic functions thereby opening up a whole range of new applications and which would not be possible with purely micro electronic systems. These systems have both electrical and mechanical components. Making small machines which are almost invisible has been one of the dreams of mankind. Nickel and alloys based nickel have been found to have good mechanical properties that can be exploited to realize movable structures in MEMS devices, moreover the magnetic properties of nickel has been widely used in magnetic MEMS. In this study, the effects of oxidants on Nickel with 4 inch diameter and 3 mm thickness chemical mechanical polishing (CMP) process were investigated mixing three different oxidizers such as Fe(NO@sub 3@)@sub 3@,

KIO@sub 3@, and H@sub 2@ O@sub 2@ with MSW 2000A slurry. Moreover, the interaction between the Nickel and the oxidizer was discussed by potentiodynamic polarization test with three different oxidizers, in order to compare the removal rate of nickel-CMP and electrochemical corrosion effects on the nickel as a function of oxidizers. As an experimental result, the removal rate of nickel was calculated by measuring the weight loss of the using Shimadzu AEX-300G balance. Fe(NO@sub 3@)@sub 3@ was higher than the other oxidizers. And as concentration in each of oxidizers increased, removal rate also increased, but over the amount, it decreased. Therefore, we conclude that nickel-CMP performances are strongly dependent on the kinds of oxidizers and the amounts of oxidizer additive. Acknowledgement: This work was supported by a Korea Research Foundation grant (KRF-2004-005-D00007).

Manufacturing Science and Technology
Room 207 - Session MS+MN+NS-WeM

Advanced Manufacturing for Nano-scale Devices & Systems

Moderators: L. Larson, SEMATECH, A. Testoni, Varian Semiconductor Equipment Associates

8:20am **MS+MN+NS-WeM1 Government Directions in Nanomanufacturing*, J.S. Murday,*** Naval Research Laboratory **INVITED**

As the U.S. National Nanotechnology Initiative heads into its second five year, there is increasing attention to the transfer of science discovery into innovative technology. The new NNI Strategic Plan identifies manufacturing of nanoscale materials, structures, devices, and systems as one of seven program areas for emphasis over the next five years. Both the Chemical and Semiconductor Industries have identified critical manufacturing issues at the nanoscale. This presentation will provide an assessment of the present state-of-art, the challenges facing nanomanufacturing, and the government efforts to address those challenges.

9:00am **MS+MN+NS-WeM3 Next Generation Semiconductor Devices based on Carbon Nanotubes*, T. Rueckes,*** Nantero, Inc. **INVITED**

Nantero is developing carbon nanotube-based nonvolatile Random Access Memory (NRAM@super TM@, a high density, high speed, low power universal memory. The target markets in aggregate exceed $100B in revenue per year. To support the development of NRAM@super TM@ Nantero has enabled a unique nanoelectronics platform that for the first time allows the use of carbon nanotubes in DUV production CMOS fabs. Single-walled carbon nanotubes have a combination of properties that make them highly valuable for use in electronics applications, such as higher electrical conductivity than copper, higher thermal conductivity than diamond, higher strength than steel, and molecular-scale size (diameter of 10Å, wall thickness of 1 carbon atom) combined with high chemical and thermal stability. However, there were substantial barriers to using this material in a mass production process: nanotubes could not be positioned reliably on wafers, they were available only with substantial particulates and contaminants and device properties were hard to control. Nantero has developed solutions to all of these problems which now allow carbon nanotubes to be used in production CMOS processes on established tool sets in existing semiconductor fabs. Nantero's carbon nanotube-enabled NRAM@super TM@can be used as an embedded memory within logic products such as microprocessors, ASICs, programmable logic or as a standalone memory that can replace multichip packages in cell phones and enable instant-on computers.

10:20am **MS+MN+NS-WeM7 Assembly Pathway to Nanotechnology: Meso to Micro to Nano*, J.R. Von Ehr,*** Zyvex Corporation **INVITED**

Zyvex is the first molecular nanotechnology company, with a vision of developing adaptable, affordable, molecularly precise manufacturing. This talk will show the progression from macroscopic manipulation, to meso-scale (millimeter), to micro-scale, and ultimately to nano-scale. Zyvex has several years of experience in building and selling nanomanipulation tools, as well as a number of microassembled MEMS products under development, including a miniature mass spectrometer. New work to be discussed is an approach to Atomically Precise Manufacturing, using UHV STM-mediated depassivation of silicon followed by repetitive cycles of Atomic Layer Deposition/Epitaxy to build 3D structures with atomic precision.

Manufacturing Science and Technology
Room 207 - Session MS-WeA

Metrology & Process Control for Advanced Manufacturing

Moderator: S. Shankar, Intel Corporation

2:00pm **MS-WeA1 Optical Interferometric Microscope for Real-Time Monitoring and Control of Focused Ion Beam Processes**, *D.P. Adams, M.B. Sinclair, T.M. Mayer,* ***M.J. Vasile****, W.C. Sweatt,* Sandia National Laboratories

Focused ion beam (FIB) techniques have a wide range of applications including lithographic mask repair, specimen preparation, semiconductor analysis and nanodevice prototyping. Although FIB systems offer excellent in-plane spatial resolution, these do not include instrumentation that actively monitors milled feature depth. In order to enhance the control of FIB systems, we have designed, fabricated and tested a custom optical interferometer microscope suitable for operation during processing. This Michelson interferometer is intended for real-time monitoring and feedback control of focused ion beam processes including sputtering. The apparatus is designed for minimal outgassing / UHV operation, and the optics are retractable (within the vacuum system) providing ample space when removed for other commonly-used diagnostic tools and gasjet assemblies. The optical path and ion beam vector are co-incident at the sample. This is made possible through use of a pinhole mirror that is positioned between the exit aperture of the ion gun and the specimen. Long working distance (39 mm), high numerical aperture (NA = 0.39) objectives have been custom designed and fabricated for the interferometer. Tests with FIB-milled Si samples demonstrate 1.0 micron optical in-plane resolution. Out-of-plane resolution is approximately 1-2 nm.

2:20pm **MS-WeA2 Method for Creating Cross-Sectional TEM Single Crystal Diamond Samples using Focused Ion Beam and In-Situ Lift Out**, ***D.P. Hickey****, E. Kuryliw, K.S. Jones,* University of Florida

A method is described for creating a transmission electron microscope (TEM) cross section of single crystal diamond using a focused ion beam (FIB) and in-situ lift-out. The method results in samples less than 50 nm thick at the tip and approximately 100-300 nm thick across the length, and does not require a large amount of starting material. Few TEM studies of single crystal diamond have been reported, most likely due to the time and difficulty involved in sample preparation. This technique can create a cross-sectional TEM sample in less than five hours. Creating cross-sectional TEM samples for single crystal diamond are slightly different than silicon due to the exceptional hardness and insulating properties of the diamond. The method also allows for additional thinning for use with high-resolution TEM imaging. The method is applied to oddly shaped diamond samples, and does not require a wafer-flat sample to create a TEM sample. This sample preparation technique has been applied to the study of ion implantation damage in single crystal diamond and its evolution upon annealing.

2:40pm **MS-WeA3 Temperature and Film Thickness Sensor for Substrates with Multi-layered Thin Films using Optical Fiber type Low-coherence Interferometry**, ***T. Ohta****,* Wakayama University, Japan*; K. Takeda,* Nagoya University, Japan*; M. Ito,* Wakayama University, Japan*; C. Koshimizu,* Tokyo Electron AT LTD., Japan

The temperature control of substrates is very significant to fabricate much finer and deeper patterns in ultra-fine processing technologies such as plasma processes. So we have developed a temperature sensor for measuring the temperature of each layer of multi-layered substrates, such as Silicon On Insulator (SOI), using a low-coherence interferometer and a Michelson interferometer. This system consisted of Super Luminescent Diodes (SLD:1550nm and 1310nm), a Laser Diode (LD:850nm), a scanning mirror, optical fibers, etc. We measured the temperature of multi-layered substrates of Si/SiO@sub 2@/Si=300µm/500µm/300µm, and as a result, we have found that this system has the resolution of 1 °C. However, this system had difficulty in measuring the temperatures of substrates with thin film layers, which have the optical pass length less than the coherent length of a low-coherent light source. To solve this problem, we have proposed a novel measurement for measuring the thickness of the thin film layer as well as the temperature of substrates. The thickness of the thin film was measured from the ratio of interference intensity of SLDs and the measured value corresponded with theoretical value within 2 micron of thickness. By estimating the film thickness the effect of interference overlapping was reduced, thus improving the error rate of temperature measurement.

3:00pm **MS-WeA4 Endpointing Chamber Clean by Calorimetric Probing of Plasma Effluent**, ***I.S. Chen****, J.W. Neuner, J.J. Welch, P.S.H. Chen, F. DiMeo,* ATMI

The semiconductor industry employs gas-phase cleaning widely to remove materials deposited on the chamber walls during thin film deposition processes. Chamber clean endpointing - i.e., terminating the process when the chamber is clean - is desirable to manage cost-of-ownership and environmental impact. Existing endpointing methods tend to rely on changes of plasma characteristics as the in situ plasma removes the deposit in time. Chamber clean technology is moving towards remote generation of plasma species for cleaning. In this arrangement, the chamber is located downstream from the plasma source. Because the etching reaction occurs ex situ, there are no relevant changes occurring in the plasma characteristics, and the effectiveness of many existing methods decreases. We report the development of a calorimetric probe for chamber clean endpointing. The probe has an all solid-state construction and is engineered to immerse in the plasma effluent during endpointing operation. The probe measures the heat flux carried by the effluent, and the signal has been shown to correlate with chamber condition. By virtue of its downstream location, the probe operation does not depend on the plasma sourcing scheme (in situ vs. remote). We demonstrate successful endpointing for in situ chamber clean of TEOS deposition process on a PECVD tool. The probe results compare favorably with other co-installed endpointing solutions.

3:20pm **MS-WeA5 Sensing and Control Strategies for Spatially Programmable CVD**, ***Y. Cai****, R. Sreenivasan, R. Adomaitis, G.W. Rubloff,* University of Maryland

A multiplexed mass spectrometric gas sampling system was designed and implemented for real-time, in situ measurement of gas species concentrations in a spatially programmable chemical vapor deposition (SP-CVD) reactor, a new paradigm for equipment design based on a segmented gas injection showerhead with exhaust gas recirculation up through the showerhead (U.S. Patent No. 6,821,910). To extend chemical sensing and metrology techniques developed for conventional CVD reactors to this new reactor configuration, we have developed a multiplexed gas sampling system based on a dynamic simulation of the sampling system, and demonstrated it in the SP-CVD reactor. Built on a three-segment SP-CVD prototype reactor, the gas sampling system was used to assess experimentally reactant gas transport mechanisms, focusing on: (1) inter-segment gas diffusion through the gap between showerhead and wafer surface; and (2) gas back diffusion through the common exhaust volume above the showerhead. We quantified the contribution of each transport mechanism to gas phase composition measured in each segment by fixing the sampling tube position and varying the gap dimension between the wafer and the movable showerhead. W CVD experiments using H2 reduction of WF6 were used to establish a model describing the relationship between the time integrated HF reaction product signal from the mass spectrometer and post-process thickness measurements obtained from four-point-probe maps of sheet resistance. Thickness metrology with precision of 3-4% has been obtained, approaching the desired range of thickness control precision. We expect that this sensing methodology not only will enable real-time spatially-distributed end point control, but also will make it possible to guide rapid reprogramming of process recipes intended to achieve simultaneously high material quality and uniformity, or to serve as a valuable asset to potential combinatorial experimental capabilities of the SP-CVD reactor.

3:40pm **MS-WeA6 High Resolution 2D dopant profiling of FinFET Structures and Silicon-based Devices using Scanning Probe Microscopies**, ***A.A. Khajetoorians****,* University of Texas at Austin*; X.-D. Wang,* Freescale Semiconductor Inc.*; J. Li,* University of Texas at Austin*; D. Pham,* International Sematech*; A.C. Diebold,* International Sematech, US*; C.K. Shih,* University of Texas at Austin

The ability to perform dopant/junction profiling with high spatial resolution is critical for development of future generation devices such as FinFET structures. Among various forms of scanning probe microscopy, scanning tunneling microscopy (STM) has demonstrated direct atomic imaging of dopant atoms on GaAs (110) surfaces. More recently, scanning thermoelectric microscopy (SThEM) (H.K. Lyeo et al Science v.303 p816 (2004)) has been applied to profile GaAs p-n junction with unprecedented spatial resolution. The key challenge to successfully apply these techniques to silicon-based devices is to prepare a surface that is both chemically and electronically passivated. Here we present our progress toward this goal. We present STM and SThEM studies on Si p-n junction devices including

FinFET structures. We also present in-depth profiling of fin structures using scanning capacitance (SCM) and conductive atomic force microscopy (C-AFM).

Magnetic Interfaces and Nanostructures
Room 204 - Session MI+MS+NS-ThM

Advanced Magnetic Storage and Manufacturing Processes

Moderator: E.A. Dobisz, Hitachi Global Storage Technologies/San Jose Research Ctr.

8:20am **MI+MS+NS-ThM1 Interface Stability between Amorphous Ferromagnetic Layer and Oxide Barriers in Tunneling Magnetoresistive Films at Elevated Temperatures**, ***X. Peng***, *D. Kvitek, A. Morone, E. Granstrom, S. Xue,* Seagate Technology

Interface stability and microstructure between amorphous ferromagnetic (FM) layers Fe@sub 56@Co@sub 24@B@sub 20@ (atomic percent), and oxide barrier layers (AlO) as deposited by physical vapor deposition, in both as-deposited and annealed states, have been studied using magnetic measurement by looper, elemental depth profiling by X-ray Photoelectron Spectroscopy (XPS), and atomic level microstructure by Transmission Electron Microscopy (TEM) respectively. AlO is amorphous on both amorphous Fe@sub 56@Co@sub 24@B@sub 20@ and crystalline FM layers. Substantial Fe diffusion towards the AlO layer and Al towards FM layer are clearly observed for Fe@sub 56@Co@sub 24@B@sub 20@/AlO system for annealing beyond 360°C, and will likely cause the MTJ devices made from this system to not functioning.

9:00am **MI+MS+NS-ThM3 Nanoimprint Technologies for Magnetic Recording Media**, *T. Ando,* ***C. Haginoya***, *K. Kuwabara, M. Ogino, K. Ohashi, A. Miyauchi,* Hitachi Ltd., Japan **INVITED**

The discrete-track and patterned media have been developed as future magnetic recording media.@footnote 1,2,3@ Nano-scale patterns are formed on the disk surface of these media. The fine patterning technologies are required for producing the patterned disks. The nanoimprint technology is attractive for the fabrication of nano-scale structures in view of cost and mass production. There are two main types of the nanoimprint technologies. One is the thermal nanoimprint technology that fine structures are formed on thermoplastic polymer layer. Another is the photo nanoimprint technology that ultra-fine structures are formed on photo-curable polymer layer. There are several key points for media application such as pattern formation area, resolution, precise control of pattern transfer, lifetime of nano-mold, alignment and so on. The pattern formation area is important for producing patterned disks. We developed a thermal nanoimprint machine that has the auto-parallel system, two step pressure system and so on. The machine enabled us to imprint fine dots on a 300 mm diameter Si wafer using a 300 mm diameter mold. The pattern formation area is large enough to produce the 65 mm diameter patterned disks. The fine resolution is required for high recording density. Austin et al. formed 6 nm half-pitch structure using supperlattice stamper,@footnote 4@ and this resolution seems enough for Tbpsi storage era. D. Wachenschwanz et al.@footnote 1@ and Y. Soeno et al.@footnote 3@ evaluated write/read performance of the discrete-track media that the grooves and servo patterns were formed by using thermal nanoimprint and etching processes. Nanoimprint is promising way for discrete-track and patterned media. @FootnoteText@@footnote 1@ D. Wachenschwanz et al., INTERMAG 2005, no. BB02 @footnote 2@ B.D. Terris et al., INTERMAG 2005, no. BB03 @footnote 3@ Y. Soeno et al., INTERMAG 2005, no. FR04 @footnote 4@ M. D. Austin et al., 3rd Conf. on Nanoimprint Nanoprint Technology 2004, no. III.2

9:40am **MI+MS+NS-ThM5 Ultra Narrow Magnetic Recording Heads: Processing Challenges**, ***M.-C. Cyrille***, HITACHI Global Storage Technologies - San Jose Research Center **INVITED**

As the areal density of magnetic recording increases well beyond 100Gb/in2, the critical dimensions of recording heads continue to shrink at a rate of 30% per year.@footnote 1@ Today, thin film heads with 100nm or less critical dimensions are being routinely fabricated in manufacturing. By the end of 2006, the physical trackwidht of read head sensors is expected to be less than 60nm. The industry is turning to Direct write E-beam and DUV 193nm as the lithography tools of choice to meet those small dimensions. As the material set used to fabricate thin film magnetic heads is unique to this technology, specific challenges arise when trying to pattern such small devices without loss of performances. Damage due to standard patterning techniques can be now be observed on both the reader and the writer as their dimensions become smaller than 100nm and advances in tooling and processes tailored to each kind of magnetic sensor are required to overcome this issue. @FootnoteText@@footnote 1@ Fontana R.E., MacDonald S.A., Santini H, Tsang C., IEEE Trans. Mag 35, 806 (1999)

10:20am **MI+MS+NS-ThM7 Correlated AFM/MFM and Magneto-Optical Studies on Epitaxial L1o FePd Thin Films**, *R.A. Lukaszew, M. Mitra,* ***J. Skuza***, University of Toledo*; A. Cebollada-Navarro, J.M. Garcia-Martin, C. Clavero Perez,* Institute of Microelectronics in Madrid (IMM) - Spain

The latest trend in data storage exploits perpendicular recording. Magnetic binary alloys (e.g. Fe-Pd, Fe-Pt) are of significant interest in magneto-recording because highly ordered L1o structures of these alloys exhibit very large magnetic anisotropy that can withstand the super-paramagnetic limit when reduced in size to accommodate the projected demands for higher areal densities. They can be deposited as films with the anisotropy axis perpendicular to the film plane, making them suitable for perpendicular media. There are practical problems associated with this scheme because usually the experimentally achieved perpendicular anisotropy tends to be too large for writing on this media. Therefore it has been suggested that canted magnetization would be more appropriate. Here we show our correlated XRD, AFM/MFM and magneto-optical studies on two series of epitaxial L1o FePd thin films of varying thickness grown on MgO. We have observed that the choice of capping material has significant effect on the resulting magnetic and magneto-optical properties of the films. We will show correlated structural and magneto-optical data for films grown under identical conditions but capped with either MgO or Pd. Our studies demonstrate that in the first case the films exhibit strong perpendicular anisotropy while in the latter the films have a magnetization component along the plane of the films in addition to the perpendicular component, thus yielding a net canted magnetization. In addition the films capped with Pd exhibit smaller coercivities than the ones capped with MgO thus enhancing their prospect use in heat-assisted magneto-recording.

10:40am **MI+MS+NS-ThM8 Magnetic Properties of Epitaxial FeN Thin Films**, *R.A. Lukaszew,* University of Toledo*; R. Gonzalez-Arrabal,* University Autonoma of Madrid, Spain*;* ***C. Sanchez-Hanke***, Brookhaven National Laboratory*; R. Loloee,* Michigan State University*; D. Boerma,* University Autonoma of Madrid, Spain

Low anisotropy and low magnetostriction iron based FCC films are attractive candidate materials for inductive thin film write heads in magnetic recording. Currently these are made of permalloy and other Fe alloys with polarization ranging from 1.0-1.6 T. Higher polarization is needed to create sufficient stray field to write on the higher-coercivity media that is needed as head and bit dimensions decrease to allow higher areal densities. Fe-N has been proposed as a possible material for the sensing element in read-head. Fe-N exhibits a variety of phases, some of which have enhance magnetic moment. In particular the meta-stable @alpha@"- Fe16N2 is particularly interesting because has the largest saturation magnetization reported of all known materials. We will present a comparative experimental study on epitaxial Fe-N thin films with varying degrees of @alpha@", @alpha@' and @gamma@' phases. The films were obtained using either sputtering or MBE. In the latter case, the films were grown in the presence of a N flow and the growth conditions were optimised in order to obtain a high content of @alpha@"- Fe16N2. A variety of characterization techniques was used to establish the epitaxial character of the films as well as the amount and kind of phase present. The magnetic properties of the samples was characterized by element specific X-ray Magnetic Circular Dichroism (XMCD).

11:00am **MI+MS+NS-ThM9 Processing Technology for Magnetic Random Access Memory**, ***M.C. Gaidis***, *J.P. Hummel, S.L. Brown, S. Kanakasabapathy, E. O'Sullivan, S. Assefa, K. Milkove, D. Abraham, Y. Lu, J.N. Nowak, P. Trouilloud, D. Worledge, W.J. Gallagher,* IBM **INVITED**

Magnetic Random Access Memory (MRAM) offers the potential of a universal memory - it can be simultaneously fast, nonvolatile, dense, and high-endurance. Depending on application, these qualities can make MRAM more attractive than SRAM, DRAM, flash, and hard drive memories, with a market measured in the billions of dollars. Small-scale demonstrations have realized much of the potential of MRAM, but scaling the memory to production on economically-profitable 200 or 300 mm wafer sizes creates unique processing challenges heretofore unseen in a large-scale semiconductor fabrication facility. MRAM read operations rely on electron tunneling through a thin (1 nm) insulating barrier between magnetic films. The exponential dependence of tunnel current on barrier thickness imposes requirements for across-wafer film uniformity on the order of 0.01 nm, made possible only by recent developments in deposition technology. To maximize performance, typical magnetic film stack designs can incorporate more than 10 distinct film layers. Very few of these layers

can be etched by semiconductor-industry-standard RIE processes, and thus have required development of novel patterning techniques specifically tuned to minimize corrosion and to handle the nonvolatile nature of etch byproducts. The elements in these complex film layers tend to interdiffuse at temperatures below that of back-end-of-line (BEOL) semiconductor processing, thus necessitating the development of low-temperature processes for creating the BEOL wiring and packaging. Although daunting, each of the aforementioned challenges has largely been overcome. This presentation provides an overview of the basic MRAM structure and operation, followed by a discussion of the MRAM-specific processing techniques that have been developed to realize this technology in megabit arrays on 200 mm wafers.

Plasma Science and Technology
Room 302 - Session PS+MS-ThM

Process Equipment Modeling

Moderator: D.J. Economou, University of Houston

8:20am **PS+MS-ThM1 Particle Modeling of Plasmas and Gases in Materials Processing*, K. Nanbu,*** *T. Furubayashi,* Tohoku University, Japan **INVITED**

The use of low gas pressure is a recent trend in plasma-assisted materials processing. The low gas pressure means that the collision frequency between two species are insufficient to recover the equilibrium in the velocity distributions. In such a case the particle modeling of plasmas and gases has more sense. First, it is shown that the particle modeling is a solution method of the Boltzmann equation. This gives the theoretical basis of the DSMC (direct simulation Monte Carlo method) for neutral gases and the PIC/MC (particle-in-cell Monte Carlo method) for plasmas. Second, the state-of-the-art modeling is discussed by introducing the problems thus far solved. Last, the results of two newly solved problems are given to show the feasibility of the particle modeling. One is the complicated gas flows in an etching apparatus, consisting of source gases Ar, C@sub 4@F@sub 6@, and O@sub 2@, radicals CF@sub 2@ and C@sub 3@F@sub 4@, and by-products SiF@sub 4@ and CO. The second is the self-sputtering of copper target. The species in the sputtering apparatus are electrons, ions, and sputtered atoms. Here we propose a method to simulate all these species simultaneously even though the velocity difference among species is disparate. This is the first application of the particle modeling to the problem where the slow neutral species are taken into consideration together with charged particles.@footnote 1@ @FootnoteText@ @footnote 1@ K. Nanbu, IEEE Trans. Plasma Science, Vol. 28 (2000), 971-990.

9:00am **PS+MS-ThM3 Coupled Analysis of Inductively-coupled CF@sub 4@ Plasmas and Radicals Flow*, H. Takekida,*** *K. Nanbu,* Tohoku University, Japan

Inductively-coupled CF@sub 4@ plasmas are widely used for the etching of oxide films. In the present work, plasma and flow in an inductively-coupled CF@sub 4@ plasma reactor are simulated simultaneously. The plasma structure and the production rates of CF radicals are examined using the Particle-in-Cell Monte/Carlo (PIC/MC) method. We included low frequency wafer biasing in the plasma simulation. The radicals flow is examined using the direct simulation Monte/Carlo (DSMC) method for which the production rate of CF@sub x@ radicals is the input data from the plasma simulation. The etching reaction on the oxide wafer and the etch products are taken into consideration in the DSMC. After the flow simulation is finished, plasma simulation is improved using the spatial distribution of background CF@sub 4@ gas which is derived from the flow simulation. We repeated a set of these plasma and flow simulation until we obtain a convergence. We compare the results with the ones where the density of background gas CF@sub 4@ is assumed to be uniform. We clarified the effect of gas flow on the CF@sub 4@ plasma structure by the use of coupled analysis. We have found that the radicals flow has a large effect on the spatial distribution of plasma density.

9:20am **PS+MS-ThM4 Effects of an Insulating Focus Ring on a Uniformity of Radical/Ion Distributions in a Wafer Interface in a 2f-CCP Etcher*, T. Yagisawa,*** *T. Makabe,* Keio University, Japan

Technological improvement in efficiency of reactive ion etching of oxide film is still a main issue in plasma etching under the circumstances that the size of the wafer has been continuously increasing from 100 mm in diameter in 1975 to 300 mm in 2003, as well as the miniaturization of ULSI. The etch rate of SiO@sub 2@ in a fluorocarbon plasma is a function of the mixture between the accumulation of radical species on the surface and the impact energy of ions incident on the wafer. Through a series of numerical studies by using VicAddress in addition to the experimental ones, we have demonstrated that a 2f-CCP (two-frequency Capacitively Coupled Plasma) driven by VHF (100 MHz) and LF (1 MHz) sources at each of electrodes has the plasma structure and characteristics appropriate for dielectric etching. That is, in a well designed 2f-CCP, VHF source is prepared to produce a high density plasma and LF source for a high energy ions incident on the wafer. We have confirmed that the radial variation of etch profile is mainly caused by the strong distortion of the surface potential at the wafer edge. In the present study, the influence of the geometry (width and height) and the dielectric constant of the focus ring in SiO@sub 2@ etching has been investigated in CF@sub 4@(5%)/Ar from the viewpoint of the ion velocity (energy and angle) distribution and the radical flux incident on the wafer as a function of radial position. The effective area of the wafer to be processed will be improved by the design of the interfacial physical structure between the surface and the bulk plasma.

9:40am **PS+MS-ThM5 Simulation in Advanced Dielectric Etch Equipment Design and Process Tuning*, K. Bera,*** *D. Hoffman, G.A. Delgadino, J. Carducci, Y. Ye, S. Ma,* Applied Materials, Inc.

Plasma and flow simulations have played vital roles to guide an advanced dielectric etch equipment design and process tuning to achieve desired process performance. Plasma simulation has been performed to study frequency effect on electron density, power deposition and dissociation fraction for a capacitively coupled discharge. Simulation results demonstrated that plasma generation efficiency enhances with increase in frequency while energy of the bombarding ions diminishes. A very high frequency source has been developed to generate high density plasma while RF bias has been used to control ion energy. Charge Species Tuning Unit (CSTU) tunes plasma density and ion flux distributions, and consequently the etch rate uniformity. Using flow simulation we evaluated species residence time that decides the extent of species dissociation in the process chamber. The gap between the showerhead and the wafer was optimized to achieve sufficient dissociation while minimizing the impact of flow convection on the wafer. Flow simulation also guided equipment design for high conductance over a large process window, and for azimuthal flow uniformity using a side pump. Using flow simulation we guided Neutral Species Tuning Unit (NSTU) design that can tune pressure and neutral flow distributions to the wafer, hence, CD bias and profile uniformities. The independent controls of plasma density and ion energy, and distributions of neutrals and ions played crucial roles in process development and tuning that are important for a production-worthy advanced dielectric etch equipment design and process tuning.

10:00am **PS+MS-ThM6 Effect of Reactor Geometry on Ion Energy Distributions for Pulsed Plasma Doping (P@super 2@LAD)@footnote 1@*, A. Agarwal,*** University of Illinois at Urbana-Champaign*; M.J. Kushner,* Iowa State University

Ultra-shallow junctions (USJ) are required for fabrication of sub-0.1 μm transistors in semiconductor integrated circuits. Plasma implantation methods such as pulsed plasma doping (P@super 2@LAD) present simple, low cost alternatives to beam line technologies. P@super 2@LAD is capable of delivering high dose rates at ultra-low energies (0.02-20 keV) using conventional plasma processing technologies.@footnote 2@ In this talk, results from a computational investigation of P@super 2@LAD using different reactor geometries will be discussed. The investigation was performed using a modified version of the Hybrid Plasma Equipment Model to address quasi-dc pulsed biases.@footnote 3@ An inductively coupled plasma is used to generate ions in pressures of 10s mTorr. A quasi-dc pulsed bias is applied to the substrate to accelerate ions. Typical bias pulse lengths range between 5 and 50 μs and bias voltages are up to 20 kV. Results will be presented for Ar/NF@sub 3@ (a surrogate for Ar/BF@sub 3@) gas mixtures. The large bias voltages and long pulse lengths result in there being considerable thickening of the sheath during the pulse. Sufficient charge is extracted during the pulse that some amount of depletion of ions results. Non-uniformities in plasma density as the sheath extends into the plasma or the ability of the plasma to repopulate depleted charge can have a significant effect on the ion energy distributions (IEDs) to the substrate, which influences the doping profiles. For example, at sufficiently high biases (>2 kV), the IEDs can be skewed in the direction of the source of ion production with the result that the ions approach the substrate preferentially from one direction. As the sheath expands into the center of the reactor where the plasma density is higher, the rate of expansion slows. The result can be a laterally dependent sheath thickness which in turn affects the collisionality of ions crossing the sheath. The consequences of varying reactor aspect ratios and positioning of coils on

IEDs will be discussed. @FootnoteText@ @footnote 1@ Work supported by VSEA, Inc. NSF (CTS03-15353) and SRC. @footnote 2@ S. B. Felch, B. -W. Koo, R. B. Liebert, S. R. Walther, and D. Hacker, Surf. Coatings Technol., 156, 229 (2002) @footnote 3@ A. Sankaran and M. J. Kushner, J. Vac. Sci. Technol. A, 22, 1242 (2004)

10:20am **PS+MS-ThM7 Computational Modeling of Process Induced Damage During Back End of Line Wafer Processing***, **S. Rauf**, M. Rasco, A. Haggag, R. Chatterjee, M. Moosa, K. Junker, P. Ventzek,* Freescale Semiconductor, Inc.

A variety of back end of line (BEOL) processes can subject ultra-thin gate dielectrics in transistors to extremely large electric fields or currents. These processes include plasma etching, plasma enhanced deposition and electron beam treatment of low-@kappa@ dielectrics. A computational modeling infrastructure is described in this presentation that is being used to address process induced damage issues for BEOL microelectronics manufacturing processes. The model couples simulations of plasma etching and electron beam processes to an electrostatic model for charging of gate dielectric. The 2-dimensional models for capacitively and inductively coupled etching plasmas are fluid-based and take account of the detailed plasma chemistry of etching plasmas. The electron beam process is simulated using a 1-dimensional Monte Carlo model. The 2/3 dimensional electrostatic model solves the coupled set of Poisson equation and current continuity equation. Dielectric and semi-conducting properties of materials are taken into account in the electrostatic model using nonlinear electric-field dependant conductivity. Computational results show that, if the gate dielectric is exposed to current from the processing equipment, it charges up rapidly leading to dielectric breakdown. The structure of the transistor, materials surrounding the transistors (e.g., insulation layers) and area of charge collection antennas determine how much current flows through the gate dielectric and the consequent damage that occurs to it. Examples are used to illustrate how this modeling infrastructure is being used to help design BEOL processes and integrations.

10:40am **PS+MS-ThM8 Computational Model for Ion Beam Extraction from a Pulsed Plasma Through a Grid***, **S.-K. Nam**, V.M. Donnelly, D.J. Economou,* University of Houston

A computational model was developed to study the energy and directionality of an ion beam extracted from a pulsed plasma through a grid. First, a fluid model was used to obtain the space and time resolved profiles (at the periodic steady state) of the active glow (power ON) of the 13.56 MHz plasma. Then, the plasma evolution in the afterglow (power OFF) was followed with the fluid model. A positive DC bias voltage (acceleration voltage) was applied at a specific time in the afterglow to raise the plasma potential and expel positive ions out of the plasma and through the grounded extraction grid. The electric potential profiles found by the fluid model were in turn used as a boundary condition in a Particle-in Cell (PIC) simulation of ion flow through the holes of the grid. The output of the PIC simulation was the energy and angular distributions of the extracted ion beam. Fractional beam neutralization by ion contact with the metal grid was also determined. Beam directionality improved by extracting ions in the afterglow as the electron temperature dropped precipitously. A smaller diameter of the grid holes and a greater DC acceleration voltage also improved beam directionality. The energy distribution of the beam was very sharp (assuming ideal step accelerating voltage) except at higher pressures when ion-neutral collisions played a role. Work supported by NSF-NIRT and the Texas Advanced Technology Program.

11:00am **PS+MS-ThM9 CKnudsen - a Chemkin-based Collisionless Transport and Surface Reaction Simulator***, **A.H. Labun**,* University of British Columbia - Okanagan, Canada

Reactive gas transport through a channel differs in the molecular flow (collisionless) regime from the flow in a fluid (collisional) regime. Chemical systems composed of gas and surface species and elementary reactions on the surface are simulated in the collisionless transport regime by CKnudsen, a new Chemkin code. Angular distributions for incident flux from all sources for each gas species are assembled at each point of the surface which encloses the volume. The system of simultaneous reaction rate equations is solved deterministically at each surface point. The reaction rates at each surface point together with the input angular flux distribution for each gas determine the angular distribution of reemitted flux for each gas. The use of the same Chemkin reaction formalism and subroutine libraries used by fluid codes facilitates multi-scale simulation and the validation of proposed reaction mechanisms in different regimes. As an example, Arora and Pollard's W CVD mechanism with 16 elementary surface reactions@footnote 1@ is converted into Chemkin format and evaluated at the equipment scale and then at the feature scale in submicron trenches and compared to experimental results. @FootnoteText@ @footnote 1@ R. Arora and R. Pollard, J. Electrochem. Soc. vol. 138, 1523-1537 (1991).

11:20am **PS+MS-ThM10 Simplified Model for the DC Planar Magnetron Discharge***, **G. Buyle**, D. Depla, R. De Gryse,* Ghent University, Belgium

In order to investigate the DC planar magnetron discharge, we developed a simplified 2D model.@footnote 1@ This model differentiates itself from numerical models by analytically calculating the ionization caused by the high energy electrons, i.e. the electrons with energy above the ionization threshold. The model also takes into account that secondary electrons, which are emitted from the target due to ion bombardment, can be recaptured by the target.@footnote 2@ Here, the simplified model is extended such that the discharge current can be calculated. To achieve this extension, the Child-Langmuir law is applied and adapted to account for the specific magnetron discharge conditions. This way, a self-consistent model for the magnetron discharge is obtained. The extended simplified model allows investigating the influence of different external parameters on the magnetron discharge. The parameters considered are the magnetic field strength, the gas pressure, the secondary electron yield and the electron reflection coefficient. The latter two parameters are mainly determined by the target material. Special attention is given to the influence of these parameters on the current-voltage characteristic. Especially the considered target material properties seem to have a strong influence: increasing the secondary electron yield shifts the current-voltage characteristic to lower discharge voltages and increases its slope. Increasing the electron reflection coefficient leads to the same changes but their magnitude is larger. @FootnoteText@ @footnote 1@ G. Buyle et al., Vacuum 74 (3-4), 353-358, 2003.@footnote 2@ G. Buyle et al., J. Phys. D: Appl. Phys. 37, 1639-1647, 2004.

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