Monday Afternoon, October 31, 2005

Plasma Science and Technology
Room 304 - Session PS2-MoA

Silicon Etching

Moderator: D. Leonhardt, US Naval Research Laboratory

2:00pm **PS2-MoA1 Advanced Gate Stack Etch Modeling for 65 nm Node***, **P.J. Stout**, M. Shroff, T. Stephens, J.E. Vasek, O.O. Adetutu, S. Rauf, P. Ventzek,* Freescale Semiconductor, Inc.

A reactor/feature modeling approach has been applied to etching an advanced gate stack. The reactor model is HPEM (developed at the University of Illinois) and the feature model is Papaya (developed at Freescale). Papaya is a 2D/3D Monte Carlo based feature scale model. The reactor model supplies Papaya with the identity, flux rate, angular distribution, and energy distribution of specie incident on the feature surface. Papaya has also been coupled to lithography models to obtain the initial resist profile used as a mask during the etch process. The gate stack consists of polysilicon, an anti-reflective coating, and a hard mask. Discussed will be the 3D feature modeling of the plasma etch steps required to etch through the gate stack. The cummulative effect of the gate etch steps is studied. The influence each etch step has on subsequent steps will be explored. The photoresist profile and feature proximity effects on the final polysilicon profile will also be discussed.

2:20pm **PS2-MoA2 Investigation of Gate Oxide Behavior during Highly Selective Poly-Si Gate Etching for Triple Gate Transistors***, **D. Kim**, H.S. Lee, S.J. Park, Y.J. Jee, K.K. Chi, C.J. Kang, H.K. Cho, J.T. Moon,* Samsung Electronics, South Korea

Triple gate transistor, or FinFET, is one of the most promising candidates for the next CMOS technology. FinFETs have better capability for higher transistor current and better controllability for the short channel effect, especially for sub 50nm ULSI devices. However, focusing on the fabrication aspects, the structure of FinFET has difficulties to overcome, which are inherently originated from using the fin-shaped active structure: (1) The thin gate oxide should be able to stand for the large amount of gate poly-Si etching not to leave any residues on the sidewalls and the bottom area of the 3-dimensional fin structure. (2) We should also overcome the undercut or tapering of the gate profile on the top and sidewall of the active area, which also originate from the 3-dimensional fin structure. These directly affect transistor characteristics such as threshold voltage distribution. In this work, we report detailed analyses on highly selective poly-Si gate etching for a FinFET. Since poly-Si etching should be carried out to the bottom area of the fin with G-ox exposed to the etch environment, high etch selectivity to G-ox is required. From this point of view, we tried to fully figure out how initial G-ox is affected by polymer deposition on G-ox, etching of G-ox itself, and plasma oxidation of silicon beneath the G-ox, which compete with one another during the gate etching. Transmission Electron Microscope (TEM) analysis, G-ox wet etch rate measurement, and measurement of electrical characteristics such as density of interface trap, charge density, leakage current were implemented. Based on the above investigations, plasma oxidation is considered to play an important role in gate etching with thin G-ox. It is also shown that the silicon-containing byproduct during gate etching is indispensable for polymer generation.

2:40pm **PS2-MoA3 Silicon Etching Beyond the 90nm Technology Node: the Need for Total Parameter Flexibility***, **A.M. Paterson**, T. Panagopoulos, T.J. Kropewnicki, V. Todorow, A. Matyushkin, B. Hatcher, S. Pamarthy, N. Gani, A. Khan, S. Deshmukh, M. Shen, T. Lill, J.P. Holland,* Applied Materials **INVITED**

As CMOS technology node sizes push further into the nano-scale domain (sub 100nm) it has initiated new challenges for the silicon etching of logic and DRAM structures. In order to keep abreast of Moore's Law, new gate materials, geometries and architectures are currently being explored by IC manufactures with the intent of driving the node size to 32 nm by the end of this decade. Such device scaling brings new demands to wafer etch suppliers, with even more stringent etch requirements expected. At present, 90 nm technology is the smallest node in volume production, with the gate lengths being approximately 65 nm and CD bias requirements of 4 nm 3s over the entire 300 mm wafer, 3 mm edge exclusion. CD bias control is of paramount importance as it directly correlates to processor speed and cost. For smaller nodes the combination of resist trimming and curing (to prevent Line Edge Roughness (LER)) and process parameter flexibility become even more crucial in controlling the gate CD bias. This presentation will focus on the research and development work undertaken at Applied Materials to produce novel silicon etch equipment that will enable IC manufactures to obtain their goals for continued node size reduction. Experimental and theoretical work will be discussed showing the many novel features of an advanced 300 mm Applied Centura® DPS® process chamber for sub-65 nm gate, Shallow Trench Isolation (STI) and capacitor etches. This chamber has been designed to produce precise resist trimming / curing with total process step parameter flexibility allowing CD bias control of less than 3 nm 3s, 2 mm edge exclusion, for sub-65 nm technologies.

3:20pm **PS2-MoA5 Silicon Gate Etching using Amorphous Carbon Hard Mask***, **F. Lazzarino**,* CNRS/LTM, France*; P. Gouraud,* STMicroelectronics, France*; T. Chevolleau, B. Pelissier, G. Cunge, L. Vallier, O. Joubert,* CNRS/LTM, France*; T. Lill,* Applied Materials

Nowadays, the development of new integrated circuit generations requires the introduction of new materials. Among them, the amorphous carbon (a-C) is a promising candidate as a hard mask for gate etching processes due to its high selectivity to silicon (6:1). Moreover, since the conventional photolithography is not able to achieve resist linewidth lower than 80 nm, the trimming of a-C can be used as a new strategy to obtain sub-30 nm gate length. In this paper, an etch integration scheme using a-C hard mask is evaluated on 300 mm wafers and fully characterized for undoped, n-doped and p-doped wafers. The gate stack is composed of 1.2 nm SiON gate oxide, 100 nm polysilicon film, 100 nm PECVD amorphous carbon, 20 nm dielectric anti-reflective coating (DARC). The wafers are patterned with a 193 nm lithography and etched in an industrial inductively coupled plasma reactor. The resist trimming combined with the a-C trimming is investigated using different types of halogen chemistries containing oxygen (HBr/O@sub 2@, Cl@sub 2@/O@sub 2@,...) which allow to obtain sub-30 nm gate structures. The polysilicon gate is etched in conventional HBr/Cl@sub 2@/O@sub 2@ chemistries and the impact of the plasma parameters on the etch rates and both undoped and doped (n and p) gate profile is evaluated. Futhermore, chemical topography analyses by quasi in-situ X-ray Photoelectron Spectroscopy (XPS) are performed in order to correlate the etch profiles with the chemical composition of the passivation layers deposited on the sidewalls of the polysilicon gate.

3:40pm **PS2-MoA6 Atomic Scale Etching of Poly-Si in Inductively Coupled Ar and He Plasmas***, J.-H. Min,* Seoul National University, Korea*; S.H. Moon,* Seoul National University, Korea, South Korea*; Y.W. Kim,* FOI Korea Corporation, Korea*; C.B. Shin, **C.-K. Kim**,* Ajou University, Korea

For fabrication of novel Si-based devices, device structures with a high aspect ratio are increasingly required. The reactive ion etching is widely used for defining fine features, but energetic ions generated in a plasma are known to cause serious radiation damages. In a low-energy ion system, isotropic chemical reactions caused by neutrals become predominant and the deterioration of the pattern definition will occur. Therefore, a new concept of directional etching with minimum reaction energy is needed. In this work, atomic scale etching of poly-Si was performed by using a cyclic process of etchant adsorption and ion beam irradiation. This process is the same as the so-called atomic layer etching of single crystalline Si. Cl@sub 2@ was used as an etchant gas, and Ar or He ions generated in an inductively coupled plasma was used as an ion beam. The self-limiting characteristic of the etch rate with respect to the duration of ion irradiation for poly-Si etching was significantly different from that for single crystalline Si etching. That is, as the duration of the ion irradiation increased, the poly-Si etch rate was initially increased and converged to about 0.6Å/cycle and then rapidly increased, eventually showing a characteristic S curve. When He ions were used as an ion beam, the bias voltage region where the etch rates were smaller than the sputtering rates was observed, which was in contrast to the case where Ar ions were used as an ion beam. It is believed that this is because the size and mass of He ions are much smaller than those of chlorine atoms adsorbed on the poly-Si surface and therefore the chlorine atoms effectively prevent the poly-Si layer from being sputtered by the He ions.

4:00pm **PS2-MoA7 Spectroscopic and Real-Time Study of Ar@sup +@ and XeF@sub 2@ Etching of Si(100) by Second Harmonic Generation***, **A.A.E. Stevens**[1], P.M. Gevers, J.J.H. Gielis, M.C.M. Van De Sanden,* Eindhoven University of Technology, The Netherlands*; W.M.M. Kessels,* Eindhoven University of Technology, The Netherlands, Netherlands*; H.C.W. Beijerinck,* Eindhoven University of Technology, The Netherlands

To gain new insights into the fundamental processes occurring at surfaces during plasma etching, Second Harmonic Generation (SHG) has been

[1] **PSTD Coburn-Winters Student Award Finalist**

employed to study the etching of Si(100) in an Ar@sup +@/XeF@sub 2@ beam etching experiment. SHG by a medium is only allowed when inversion symmetry of the medium is broken and is therefore possibly extremely sensitive to surfaces and interfaces. Using a Ti:Sapphire laser in the 710 to 920 nm wavelength range the strain-induced resonance of Si-Si bonds (2.70-3.44 eV) has been probed before, during and after etching by Ar@sup +@ ions and XeF@sub 2@. Low-energy (20-2000 eV) ions impinging onto the Si(100) create a damaged, amorphized Si layer, which leads to an enormous increase in the SH signal within less than 1 ML Ar@sup +@ dose, and broadening of the resonance, indicative for an amorphous medium. XeF@sub 2@ passivation of the surface after the ions are switched off reveals that the signal originates not only from the surface but also from a buried interface between the damaged and crystalline silicon. At the switch-on of the XeF@sub 2@ after the ion bombardment an immediate increase of the SH signal (at 3.42 eV) can be observed showing an instant reaction of F with the highly reactive amorphous silicon surface. For XeF@sub 2@ etching of Si(100) two separate spectral features in the SH signal can be distinguished. After the XeF@sub 2@ is switched off, the spectral features change, indicating a reconstruction of the reaction layer. Furthermore, dosing a hydrogen terminated surface with XeF@sub 2@ shows an increase in the SH signal over the full spectral range before the actual etching begins as a result of the initial binding of F to Si. These and other observations will be discussed, which have led to some surprising new insights in the etch mechanism of Ar@sup +@ and XeF@sub 2@ of Si(100), showing that SHG is a promising, powerful diagnostic tool for surface sensitive studies of etch mechanisms.

4:20pm **PS2-MoA8 Optimization of Cryogenic Processes with Plasma Diagnostics***, **T. Tillocher**, R. Dussart, X. Mellhaoui, P. Lefaucheux, N. Mekkakia Maaza,* GREMI - Université d'Orléans, France*; M. Boufnichel,* ST Microelectronics*; L.J. Overzet,* University of Texas at Dallas*; P. Ranson,* GREMI - Université d'Orléans, France

The so-called cryogenic process is a good alternative to the Bosch process for the etching of high aspect ratio structures. Indeed, etching and passivation occur simultaneously and anisotropic profiles result from a balance between these two mechanisms. Consequently, high etch rates can be reached with relatively smooth profiles. This equilibrium is put into evidence with mass spectrometry and optical spectroscopy on maskless silicon wafers : an oxidation threshold appears from one oxygen percentage in the SF@sub 6@/O@sub 2@ plasma where the etch rate drops. In such a case an overpassivation regime is reached, which strongly reduces the etching. We have shown that this threshold depends on the substrate temperature, the source power and the chuck self-bias : a lower temperature involves a higher sticking coefficient of oxygen on silicon and a higher energy transmitted to the wafer by the ions can prevent the formation of the layer. We think that these results, which can be characterized with a simple model, can also be correlated to the etching of high aspect ratio patterns. Indeed, the interaction between the surface and the radicals is quite similar on a bulk silicon wafer and on the sidewalls of the patterns. This appears to be a way to find the optimum oxygen flow. Plasma diagnostics, such as mass spectrometry, optical emission spectroscopy and Langmuir probe can also be used to optimize the other plasma parameters, especially the SF@sub 6@ flow and the source power. Finally, we will present performances which can be reached with optimized processes in the case of holes etching for the drilling of 400 µm thick silicon wafers.

4:40pm **PS2-MoA9 The Role of the Reaction Products in the Silicon Etching Cryogenic Process***, **R. Dussart**, X. Mellhaoui,* GREMI - Universit@aa e@ d'Orleans, France*; T. Tillocher,* GREMI, France*; P. Lefaucheux, N. Mekkakia Maaza,* GREMI - Universit@aa e@ d'Orleans, France*; M. Boufnichel,* ST Microelectronics, France*; L.J. Overzet,* Univ. of Texas at Dallas*; P. Ranson,* GREMI - Universit@aa e@ d'Orleans, France

The cryogenic process of silicon deep etching can be used in MEMS and power microelectronic component fabrication. In this process, a SF6/O2 plasma is used to etch high aspect ratio silicon microstructures. The bottom of the structure, which is submitted to ion bombardment, is etched while lateral etching is inhibited by the formation of a SiOxFy passivation layer. This layer, which only appears at low temperature and with oxygen, is continuously deposited on the microstructure sidewalls during the etching process. The formation of this passivation layer is not well characterized. It mostly desorbs when the wafer is warmed up to ambient temperature. In particular, the role of SiF4 (the main etching product) is not well understood. Experiments with SiF4/O2 and SF6/O2 plasmas were carried out to investigate the formation of the passivation layer. Mass spectrometry, profile characterization by SEM and ellipsometry measurements were carried out to better understand the role of SiF4 in the passivation layer formation in the cryogenic process.

5:00pm **PS2-MoA10 The Characterization of Silicon Trench Etching in a High Density Reactor Using Self-Excited Electron Resonance Spectroscopy (SEERS)***, **F.C. Session**,* Fairchid Semiconductor, US

The development and characterization of a medium depth Si trench process for power IC applications, was performed utilizing Self-Excited Electron Resonance Spectroscopy (SEERS). SEERS provides volume averaged plasma parameters such as electron collision frequency, electron density and sheath width by monitoring the non-linearity of the space charge sheath at the electrode. Several etch chemistries were investigated including SF@sub 6@/ O@sub 2@, Cl@sub 2@/ O@sub 2@, HBr/ O@sub 2@, HBr/SF@sub 6@/O@sub 2@ and Cl@sub 2@/SF@sub 6@/O@sub 2@ and their effect on etch rate and sidewall profile. Pressure appears to be the overwhelming parameter in terms of profile and has a large effect on the electron collision rate and electron heating mechanisms. The study of pressure effects on electron temperatures and electron collision rates have been performed@footnote 1@ but these parameters have yet to be correlated to the actual etch performance and trench morphology. This study looks at these relationships and their effects on the optimized trench process.

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