Wednesday Morning, November 2, 2005

Plasma Science and Technology
Room 304 - Session PS-WeM
Advanced Gate Stack Fabrication

Moderator: S. Vitale, Texas Instruments

8:40am **PS-WeM2 Ta Based Metal Gate Etch for Dual Metal Gate CMOS Applications***, **C.H. Huffman**, Z. Zhang,* Texas Instruments Assignee to SEMATECH*; S.C. Song,* SEMATECH

Although the ITRS states that low power applications may require high-k materials first, the high performance devices trend will soon require both high-k dielectrics and metal gate electrodes to remove polysilicon depletion effects. The selection of the metal gate material will be driven by the workfunction of the metal in order to control the threshold voltage of the transistors. Candidate metals should have a workfunction within 0.1v of the conduction band and the valance band edges for NMOS and PMOS respectively. The potential NMOS candidate metals are more reactive while the PMOS candidates are more noble like and this creates an etch challenge for dual metal CMOS integration. This paper will discuss the formation of dual metal gate CMOS structures using Ta based metal electrodes (TaN, TaSiN, TaCN). Affects of plasma parameters on the various metals will be discussed with respect to successful construction of dual metal gate CMOS. Differences in recipes for the various metals will be compared and contrasted with respect to successful construction of advanced metal gate electrodes. Included in the discussion will be potential process solutions for some of the common multiple material gate etch issues that occur. Optical endpoint control will be included for selected materials and process steps.

9:00am **PS-WeM3 Challenges in Plasma Processing for Advanced Gate Stack Fabrication***, **B.-W. Chan**,* Taiwan Semiconductor Manufacturing Corp., Taiwan*; Y.-H. Chiu,* Taiwan Semiconductor Manufacturing Corp.*; E. Luckowski, B. Goolsby, S. Rauf, P.J. Stout, B. White, P. Tobin,* Freescale Semiconductor*; H.-J. Tao, S.-M. Jang, M.-S. Liang,* Taiwan Semiconductor Manufacturing Corp. **INVITED**

High gate leakage current limits gate oxide thickness shrinkage in traditional SiO2 dielectrics. New gate stacks with novel material combinations are being investigated to reduce gate leakage while enhancing transistor performance. The combination of high K dielectrics and metal gates is a leading candidate for advanced CMOS gate materials but at the cost of increased complexity and greater challenge for the plasma processes that would be used to etch them. In this presentation, we will point out critical issues related to high K and metal gate etch and in particular dual metal gate fabrication. Examples of how simulation is being used to aid advanced gate etch development will also be presented. A specific focus of the talk will be gate trim process and resultant accurate critical dimension (CD) control and meeting CD control metrics required for beyond 65nm transistor fabrication.

9:40am **PS-WeM5 Challenges in Plasma Etching of Metal Gate Stacks***, **A. Le Gouil**,* STMICROELECTRONICS*; E. Richard, T. Chevolleau, G. Cunge, O. Joubert, L. Vallier,* LTM (CNRS), France

The rapid downscaling of metal-oxide-semiconductor transistors imposes the introduction of metal gates electrodes and high k gate dielectrics. Hence the patterning of a typical gate stack (Si/metal/high-k) requires the development of new etching processes. In this work the metal gate etching process is developed with both poly-Si/TiN and poly-Si/TaN stack for the gate electrode and HfO@sub2@ or HfSiO (3.5 nm thick) as the gate dielectric. First, the silicon part of the gate is etched using a standard HBr/Cl@sub2@ silicon gate etching process, which is followed by the metal etching step. By comparison with classical silicon etch processes two main issues are identified during the etching of the metal gate stack. First, when silicon etching stops on a metal instead of a SiO@sub2@ layer, a slope is observed at the bottom of the silicon etch profile. This difference is attributed to charging effect: charge accumulation on the insulator gate oxide deviate the ions towards the bottom of the gate (thus eliminating the gate foot), while this does not occur on a conductive metallic layer. Second, in the HBr-rich chemistry that is needed to etch the metal layer selectively towards the gate dielectric, a strong slope is systematically observed in the metal etch profile. This slope is attributed to the continuous increase of the mask dimension during the etching process due to the redeposition of precursors on the mask and feature sidewalls. We will show that these precursors originates from the SiOCl coating formed on the reactor walls during the silicon etching process, and which is subsequently sputtered during the metal etching step. This is a serious issue for critical dimension control in metal gate etching processes, and potential strategies to minimize it will be investigated.

10:00am **PS-WeM6 Investigation of Fluorocarbon Polymer Formation in Polysilicon Etching on Metal Gate***, **E. Luckowski**,* Freescale Semiconductor, Inc.*; B.W. Chan,* TSMC*; S. Rauf, A. Martinez,* Freescale Semiconductor, Inc.

It is well known that control of critical dimension and profile for ULSI devices with conventional polysilicon gates below the 90-nm technology node requires a detailed understanding of chemical etching and by-product deposition mechanisms in a plasma system. Carbon-containing feedstock gases such as CF4 are typically used in mixtures of Cl2, HBr, and/or SF6 to achieve a balance between deposition and etching required for profile control that also meet selectivity requirements for thin dielectric layers in MOSFET devices. Impact of chamber walls and contribution of species from masking materials can play an important role in the overall balance, as well as other additives such as O2 and N2. For advanced gate stacks, as conventional polysilicon gates are being replaced by metal gates to overcome polysilicon depletion effects, the impact of these various mechanisms on metal gate patterning must also be considered. In this work, we investigated the impact of polymer formation in polysilicon etch processes on the profile of polysilicon/transition metal gate stacks on high-K dielectrics. For fluorocarbon etching in particular, the C/F ratio has been found to strongly impact the final profile of polysilicon/metal gate stacks. OES and in-situ reflectometry were used to characterize composition and changes in the plasma conditions, while polymer formation and etch rate were characterized by SEM/TEM. Plasma modeling was also done using a 2D integrated equipment-feature scale model to improve understanding of the interaction between polysilicon and metal gate etch processes.

10:20am **PS-WeM7 Ion-Enhanced Plasma Etching of Metal Oxides in Chlorine Based Plasma***, **R.M. Martin**,* University of California, Los Angeles*; H.O. Blom,* Uppsala University, Sweden*; M. Sawkar, J.P. Chang,* University of California, Los Angeles

The development of plasma etching chemistries is necessary to pattern new gate dielectric materials, such as hafnium based oxides, for sub-65nm complementary metal oxide semiconductor (CMOS) devices. An electron cyclotron resonance high density plasma reactor is used in this work to study the etching of metal oxides and their corresponding metals in chlorine based chemistries. The plasma density, electron temperature, and gas phase species are characterized by a Langmuir probe, an optical emission spectrometer, and a quadrupole mass spectrometer. The etching of Al@sub 2@O@sub 3@, SiO@sub 2@, and HfO@sub 2@ was first studied in Cl@sub 2@ and BCl@sub 3@ plasmas, to allow for studies of the etching of hafnium aluminate, HfAl@sub x@O@sub y@, and hafnium silicate, HfSi@sub x@O@sub y@, with well controlled and varying compositions of Al and Si in HfO@sub 2@. The dominant etch products of Al and Hf metals in Cl@sub 2@ and BCl@sub 3@ plasmas were metal chlorides and metal boron-oxy-chlorides, respectively. These results enabled the assessment of the effect of metal-oxygen bond strength on the surface etching reactions, as well as the oxygen removal mechanism in the etching of metal oxides. The etch rates of hafnium aluminates were found to increase with the square root of ion energy, and the surface chlorination was enhanced with increasing ion energy, demonstrating that the etching reaction is limited by the momentum transfer from the ions to the film surface. The etching selectivity of HfAl@sub x@O@sub y@ and HfSi@sub x@O@sub y@ to Si in Cl@sub 2@ and BCl@sub 3@ plasmas will be presented, with a focus on the effect of increasing concentrations of Al and Si, and how the etch rates compare to the etching of Al@sub 2@O@sub 3@, SiO@sub 2@, and HfO@sub 2@ individually. Finally, the application of a generalized model, developed for the etching of ZrO@sub 2@ and HfO@sub 2@, to the etching of Hf aluminates and silicates in chlorine based plasmas will be discussed.

10:40am **PS-WeM8 ICP Etching of p-type Conducting Materials with High Work Function for CMOS Application***, W.S. Hwang, Y.Q. Wang,* National University of Singapore*; **W.J. Yoo**,* National University of Singapore, singapore*; V.N. Bliznetsov,* Institute of Microelectronics, Singapore

As metal electrode / high-k dielectric gate stacks are expected to be integrated for future complementary metal oxide semiconductor (CMOS) device process, extensive research on new conducting electrodes as a replacement for poly-Si is currently underway. Many candidate materials have already been identified as potential n-type conducting materials in the work function range of 4.0-4.5 eV. However, only a few conducting materials have high work functions above 5.0 eV to replace p-type poly-Si, and thus IrO@sub 2@, Ir, Ni, and Pt which meet this requirement are

receiving significant attention as candidates of p-type conducting materials. Plasma etching of these materials is one of the most challenging issues in the integration of advanced CMOS gate stacks because of their chemically inert property. In this work, the etching properties of the p-type conductors / high-k gate stacks are investigated in SF@sub 6@ / Cl@sub 2@ / O@sub 2@ using inductively coupled plasma (ICP). Gas composition and plasma parameters of pressure, source power and bias power were changed to understand the etching mechanisms. The linear dependence of etch rates on the square root of bias voltages obtained from most of the above p-type conducting films indicated the dominance of ion induced etch mechanism in both SF@sub 6@ and Cl@sub 2@ etching. The effect of byproducts generated during etching on surface properties showed two different trends, depending on which type of by-product formation is predominant: volatile or nonvolatile. This phenomenon was well explained by evaporation temperature and Gibbs free energy of formation of byproducts in SF@sub 6@ and Cl@sub 2@. X-ray photoelectron spectroscopy (XPS) also revealed that more residues remain after the Cl@sub 2@ etching than the SF@sub 6@ etching. Using the optical emission of fluorines and other halogenated compounds, we were able to control the etch endpoints from the gate stack using p-type conducting materials.

11:00am **PS-WeM9 Damage-free MOS Gate Electrode Patterning on Thin HfSiON Film Using a Neutral Beam Etching***, **S. Noda**, T. Ozaki, S. Samukawa,* Tohoku University, Japan

We have already reported that our newly developed neutral beam could realize highly anisotropic gate electrode patterning on thin SiO@sub 2@ film with reasonable etching rate and etching selectivity.@footnote 1@ In this paper, radiation damages during the gate electrode patterning on thin HfSiON gate dielectric films (2nm) were investigated in our system. By changing the beam acceleration method (DC or RF voltages) in the neutral beam source, the beam flux and its composition (ratio between neutral and charged particles) could be controlled on the surface. Then, the leakage current of gate dielectric film was measured with antenna MOS capacitors. Although the gate leakage currents of the MOS capacitors measured just after the etching of poly-Si electrodes slightly increased in any conditions, its values were sufficiently lower (less than 1/10) than that in a conventional plasma etching. Since the leakage current increased according to over etching time, it was understood that a little degradation was caused by small stress current through the thin gate dielectric films due to the residual charges even during the neutral beam etching process. However, the residual charge current was extremely low and degradation of the gate dielectrics was negligibly small even if annealing was not performed in the neutral beam process. @FootnoteText@ @footnote 1@S. Noda et al., JVST A22,1506 (2004).

11:20am **PS-WeM10 Evaluation of Several Plasma Etching and Boron Cleaning Processes for Hafnium Oxide Thin Films on Silicon***, **C. Wang**, V.M. Donnelly,* University of Houston

At present, BCl@sub 3@-containing plasmas are commonly used to etch high dielectric constant ("high-k") materials such as HfO@sub 2@ and aluminum oxide. However, a boron residue is left on underlying surfaces during the overetch period. Boron is a p-type dopant; its presence is undesirable in subsequent processing. Previously, we reported that pure H@sub 2@ plasmas were effective in removing B from Si surfaces after HfO@sub 2@/Si and Al-oxide/Si samples were overetched in high density BCl@sub 3@ plasmas for 60 s. The underlying Si substrate, however, was etched about 15 nm. Here we report that dilute H@sub 2@/Ar plasmas (1 to 5% of H@sub 2@) are also effective in removal B, but in a more controlled fashion, such that the etching of the Si substrate can be minimized. After 60 s overetch in BCl@sub 3@ plasmas, HfO@sub 2@ samples were transferred under vacuum to an ultrahigh vacuum (UHV) for X-ray photoelectron spectroscopy surface analysis. B deposited during BCl@sub 3@ plasma etching was removed from the reactor walls in a pure H@sub 2@ plasma, and the samples were then returned to the plasma chamber and exposed to a dilute H@sub 2@/Ar cleaning plasma, and then re-examined by XPS. Under the best conditions (1% H@sub 2@/Ar plasma), > 90% of B was removed from Si in 20 s, while etching away

11:40am **PS-WeM11 Damage-free Ultrathin Oxynitride Films Formed Using Pulse-Time-Modulated Nitrogen Plasma***, **S. Fukuda**, C. Taguchi, Y. Kato, Y. Ishikawa, S. Noda, S. Samukawa,* Tohoku University, Japan

Ultra thin Si oxynitride (SiO@sub x@N@sub y@) films have been identified as leading candidates to replace conventional SiO@sub 2@ gate dielectrics for present and future ultra large-scale integrated circuits. Remote plasma processes for top surface nitridation of thermally grown oxides have been developed and applied in complementary MOS device applications. However, it is much difficult to control the concentration and position of nitrogen in ultrathin Si oxynitride film by using plasma processing and there are many serious problems, such as plasma radiation damage and increases in interface state density due to N penetrating the SiO@sub 2@-Si interface. To overcome these problems, we have already proposed pulse-time-modulated (TM) plasma nitridation.@footnote 1@ The pulsed nitrogen plasma makes it possible to restrain injection of higher energy particles from plasma into the silicon dioxide film. Then, the concentration and position of nitrogen in ultrathin Si oxynitride film could be controlled by changing the pulse-on time in the TM N@sub 2@ plasma. Additionally, the TM plasma could drastically reduce the UV and VUV photon radiation damages to Si oxynitride film, because of low electron energy during pulse-off time in the TM plasma. As a result, by using the TM plasma nitridation, NBTI characteristics were about 200 % improved at the maximum. TM plasma is very promising candidate as the damage-free nitridation method for SiO@sub 2@ and high-k films. @FootnoteText@ @footnote 1@ S. Samukawa, Y. Minemura, and S. Fukuda, Jpn. J. Appl. Phys. Vol. 42 (2003) pp. L795-L797.

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