Plasma Science and Technology
Room Exhibit Hall C&D - Session PS-MoP
Plasma Science and Technology Poster Session

PS-MoP1 Minimum Area Required for Poly Etch Endpoint Detection*, **R.L. Hill**,* National Semiconductor

There have been somewhat arbitrary design rules implemented over the years dealing with how much open (non-resist covered) area is required on a product layout at a given layer to ensure robust endpoint detection. Design rules have been used at the typical layers that employ endpoint detection, e.g. poly, isolation, metal, capacitor. A systematic study of the poly layer endpoint detection is discussed in this report. A photolithographic method is introduced to measure the open area required for endpoint detection. Two etchers are studied: Lam 4400 poly etcher and a higher plasma density Lam TCP 9400SE. The endpoint signal versus percent open area and etch rate versus percent open area are presented. The minimum reticle open area required for the Lam 4400 endpoint detection was determined to be 25% and for the Lam 9400 it was 30%. Neither etcher showed an etch rate dependence on the percent open area.

PS-MoP2 Optical Second Harmonic Generation during Ar@sup +@ Etching of Silicon*, **P.M. Gevers**, A.A.E. Stevens, J.J.H. Gielis, H.C.W. Beijerinck, M.C.M. Van De Sanden,* Eindhoven University of Technology, The Netherlands*; W.M.M. Kessels,* Eindhoven University of Technology, The Netherlands, Netherlands

Plasma etching of crystalline silicon can create a damaged layer in the top region of the silicon due to ion bombardment. Defects like strained and dangling silicon bonds are expected to be abundant in this region. The surface and interface sensitive nonlinear optical technique of second harmonic generation (SHG) is known to probe these defects in crystalline silicon and is therefore applied to study the plasma etching process. To circumvent the complexity of the plasma, the experiments are performed in a UHV multiple-beam setup, containing an ion source producing Ar@sup +@ ions with energies ranging from 20 eV to 2.5 keV. The data presented here will discuss the SH-signal in the photon energy range of 2.70-3.44 eV probing the strain-induced resonance. The silicon SH-signal exhibits an enormous increase when subjected to Ar@sup +@ ions. Careful analysis has localized the origin of the signal to both the surface of the silicon and the interface between the damaged and crystalline silicon. Future application of this diagnostic in the ion induced etching process promises to aid in the understanding of the etching process and might supply the possibility of monitoring the defects induced during processing.

PS-MoP3 The Study of Atomic Layer Etching Mechanism for Si with Various Substrate Orientations*, **S.D. Park**, C.K. Oh, M.S. Kim, G.Y. Yeom,* Sungkyunkwan University, Korea

Atomic layer etching (ALET) can be an indispensable method in the fabrication of future devices such as nano-scale devices, quantum devices etc., because current etch technology utilizing reactive ion etching dose not have precise etch rate controllability and tends to damage the surface of the devices physically and electrically due to the use of energetic reactive ions to achieve vertical etch profiles. Generally, ALET of Si is composed of a cyclic process consisted of 4 steps; (1) adsorption of Cl@sub2@ on the Si surface, (2) evacuation, (3) Ar@super+@ ion beam irradiation to the substrate surface for desorption, (4) evacuation of the etch products. But, if Ar@super+@ ion beam is used for the desorption, the etched substrate can be charge damaged due to the charged particles such as positive ions and photons generated in the plasma. In this study, the ALET of Si was carried out for the first time using an Ar neutral beam instead of the Ar@super+@ ion beam to avoid charge-related damage during the desorption of halide and its ALET characteristics of Si by Cl@sub2@ were investigated. Especially, the ALET of Si having different orientations were investigated to understand the silicon etch rate per cycle.

PS-MoP4 The Effect of Oxide Thickness on Photoemission and Photoconduction Currents during VUV Irradiation*, **J.L. Lauer**, J.L. Shohet, G.S. Upadhyaya,* University of Wisconsin-Madison

Vacuum ultraviolet (VUV) radiation with photons in the energy range of 5 to 20 eV produced by high-density plasmas in plasma-processing systems can cause degradation to devices by changing the optical, mechanical, chemical and electrical properties of dielectrics. This is particularly important for thin films used in intermetal dielectric layers, because VUV is absorbed by the dielectric layer. Radiation charging of Si wafers coated with SiO@sub 2@ of different thicknesses in the range of 3000Å to 200Å was made by exposing them to synchrotron VUV radiation with photon fluxes in the range of 10@super 10@ -10@super 11@ photons/sec cm@super -2@ and photon energies of 7, 10, and 13 eV. The photoemission current and the current drawn by the substrate were monitored during each exposure. The tunneling and/or photoconduction current drawn through the oxide layer can be found by subtracting the photoemission current from the current drawn by the substrate. The total charge induced on the dielectric during VUV exposure consists of charge due to photoemission and electron-hole-pair creation, the net amount of which can be measured with a Kelvin Probe. The tunneling current (electrons injected from the silicon substrate into the oxide layer) causes a decrease in the charge produced by photoemission and electron-hole-pair creation. For most dielectrics, the threshold photon energy for photoemission is higher than that for electron-hole-pair production. The photoemission current can be minimized while the tunneling/photoconduction current increases, if the photon energies are below the threshold energy for photoemission but larger then the bandgap energy. VUV-exposed SiO@sub 2@ of various thicknesses shows the photon penetration depth as a function of energy and allows a quantitative description of the mechanisms that are involved in the photoconduction/tunneling processes taking place. @FootnoteText@ Work supported by NSF under Grants DMR-0306582.and DMR-0084402. .

PS-MoP5 Reduction of Gate Oxide Plasma Induced Damage via Silicon Nitride Backside Film*, **H. McCulloh**, C. Bossie, P. Allard, J. Garmon, C. Printy,* National Semiconductor

Plasma charging damage continues to be an issue in advanced semiconductor processing. In this work, the effect of residual films on the backside of the wafer on plasma damage induced at interconnect layers is investigated. Our experimental results show that intermetal dielectrics formed using fluorinated high density plasma (FHDP) are particularly prone to causing plasma induced damage (PID). The current work shows that residual material on the backside of the wafer has a strong impact on this damage. It is proposed that the presence of a conductive or semi-conductive backside film contributes to PID via electrical coupling through the electrostatic chuck (ESC) during the FHDP deposition process. Our results show that the presence of a uniform silicon nitride film on the back of the wafer dramatically reduces gate oxide damage caused by PID. Different backside film integration schemes were studied. PID was evaluated using metal antenna style test structures, with FHDP being deposited directly on the antenna.

PS-MoP7 Study of the Plasma-Induced Damage by Inductively Coupled Plasma in Pb(Zr,Ti)O@sub 3@ for FeRAM(Ferroelectric Random Acess Memory) Devices*, **H.Y. Ko**, K.R. Byun, Y.J. Jung, D.H. Im, D.C. Yoo, S.H. Joo, J.H. Ham, S.H. Park, H.S. Kim, K.K. Chi, C.J. Kang, H.K. Cho, U.I. Jung, J.T. Moon,* Samsung Electronics, South Korea

FeRAM is a non-volatile memory device based on the remnant polarization of ferroelectric film such as Pb(Zr,Ti)O@sub 3@ (PZT). The electrical properties of PZT films have proven to be excellent enough to apply to high-density FeRAM with 1T1C cell structure, in terms of the high remnant polarization and low crystallization temperature. However, it is known that high-density integration gives rise to several problems such as plasma-induced damage of PZT surface and surface composition change, which degrade FeRAM capacitor performances during the patterning of capacitor module. In this article, we carried out the investigations of the plasma-induced etching damage for the PZT thin films etched with the various gases chemistries (O2, Ar, BCl@sub 3@, Cl@sub 2@, CF@sub 4@, and mixture gases) on the microstructural and electrical properties. We analyzed the effect of individual and mixture gases on the near surface chemistry of the PZT thin films by XPS(X-ray Photoelectron Spectroscopy). We also used TEM(Transmission Electron Microscopy) and AFM(Atomic Force Microscope) for the structural and compositional change and roughness in the film through patterning of the real FeRAM devices. Finally, we evaluated the electrical properties (2Pr, fatigue, leakage current, retention) of the plasma-exposed PZT films through patterning of the real FeRAM devices.

PS-MoP8 Effective Stripping of Heavily Implanted Photoresist by Insitu-Bake Process*, S.-K. Yang,* Inha University, Korea*; J. Yang,* PSK Inc.*; **S.G. Park**,* Inha University, Korea, Korea, Republic of

Popping of heavily implanted photoresist during plasma stripping, which is the main source of particulate contamination, occurs during the conventional stripping process using oxygen radicals at the temperature

range of 250°C or higher. We introduce in-situ bake process (ISBP) prior to oxygen plasma stripping which does not suffer from low ashing rate or substrate damage. It is found that baking wafers at 250°C in the atmospheric pressure before evacuating the process chamber accelerates outgassing from bulk of photoresist without popping. Since heat transfer from heating wafer stage to wafer is better in air than that in vacuum, the stripping rate is also increased 50% because time to reach the process temperature is reduced. In this paper, we show the evidence of no-popping during bake-in-air step and the surface modification by bake-in-air by XPS analysis of carbon bonding. XPS data shows that baking in vacuum enhances more amorphous carbons in the photoresist surface than baking in air.

PS-MoP9 Plasma Etching of High-k and Metal Gate Materials in High-Density Chlorine-Containing Plasmas*, **K. Nakamura**, T. Kitagawa, K. Osari, K. Takahashi, K. Ono,* Kyoto University, Japan

As ultra large scale integrated circuit dimensions continue to be scaled down, high dielectric constant (high-k) materials such as HfO@sub 2@, ZrO@sub 2@, Al@sub 2@O@sub 3@, etc. are being required as gate dielectric to maintain the gate capacitance in smaller size. Moreover, for a gate stack with high-k dielectrics, gate electrodes of conventional polycrystalline silicon (poly-Si) tend to cause some problems of the depletion layer present in doped poly-Si gate materials, thus being replaced by metal electrodes such as Pt, Ru, TaN, TiN etc. For the fabrication of high-k gate stacks, an understanding the etching characteristics and mechanisms is indispensable for high-k dielectrics as well as metal electrodes. However, only a few studies have recently been concerned with their etching for the application to high-k gate stacks. In this study, we have investigated the etching of high-k materials of HfO@sub 2@ and metal electrode materials of Pt and TaN using high-density chlorine-containing plasmas excited by electron cyclotron resonance. The etching of HfO@sub 2@ etching was performed in BCl@sub 3@ plasmas at around 10 mTorr without rf biasing, giving a high etch selectivity (>>1) over Si and SiO@sub 2@ was obtained. At lower pressures, some deposition was found to occur on all material surfaces. The etching of Pt was performed in Ar/O@sub 2@ plasmas with high rf biasing, where highly selective Pt etching was achieved over HfO@sub 2@, Si, and SiO@sub 2@ by adding O@sub 2@ to Ar. Moreover, the etching of TaN was performed in Ar/Cl@sub 2@ plasmas, where high etch rates and high etch selectivity of TaN over HfO@sub 2@, Si and SiO@sub 2@ were obtained with low rf biasing. The etched profiles of Pt and TaN were also investigated; the etched profile of Pt was positive tapered, while the profile of TaN was found to be almost anisotropic. This work was supported by NEDO/MIRAI project and by Taiyo Nippon Sanso Corp.

PS-MoP10 Effects of Non-Volatility of Etch Products on Surface Roughness during Etching of Advanced Gate Stack Materials*, **W.S. Hwang**,* National University of Singapore*; W.J. Yoo,* National University of Singapore, singapore

As device dimensions continue to shrink, it becomes very crucial to understand evolution of surface roughness of device structures during etching. Until now, the mechanism on roughness evolution of Si surface from which volatile etch products are generated has been studied by various researchers. However, surface properties of new conducting materials such as TaN, TiN, HfN, and IrO@sub 2@ have rarely reported, although several reports on etching properties of advanced gate electrodes have been reported. In this work, we investigate the effects of the plasma parameters of ion energy (E), ion current density (J@sub i@) and ratio of ion flux over neutral flux (J@super +@ / J@sub n@) on the evolution of surface properties of these materials during etching. Etch rates of all samples are seen to obey the following empirical relation of ER(t)=C@sub 1@ E J@sub i@ (J@super +@/J@sub n@) (t) where ER is etch rate. The same approach was made to understand the evolution of surface roughness. It was found that surface roughness and etch rate are inversely related each other when volatile byproducts are formed, as shown in the following relation of @sigma@(t)=C@sub 2@ 1/E 1/J@sub i@ (J@sub n@ / J@super +@) t where @sigma@ is roughness value, in that surface roughness is proportional to pressure but inversely proportional to bias voltage. This relation implies that anisotropic profile can be attained without sacrificing the surface roughness. On the other hand, it is found that surface roughness and etch rate are proportional each other when non-volatile byproducts are formed, as expressed in the relation of @sigma@(t)=C@sub 3@ E J@sub i@ (J@super +@ / J@sub n@) t. That is, the formation of nonvolatile residues promotes surface roughening during ion induced chemical etching. In addition, results show that the average lateral distance between peak to peak increases with increasing surface roughness due to the redeposition and agglomeration of nonvolatile byproducts.

PS-MoP11 Highly Selective W/WN/Poly-Si Etching by using RLSA Microwave Plasma Source*, **T. Nishizuka**, K. Song Yun, K. Ishibashi, T. Nozawa,* Tokyo Electron, LTD., Japan*; T. Goto, T. Ohmi,* Tohoku Univ., Japan

W/WN/Poly-Si stack is used as a gate material of DRAM. For the etching of W/WN layer, high density plasma sources, such as ECR, ICP, etc., are usually applied with Cl@sub2@+O@sub 2@ gases.@footnote 1@ An important requirement of this etching is selectivity to Poly-Si. The selectivity can be improved by increasing oxygen fraction. However, actual selectivity used to be 1 or so because oversupply of oxygen causes deposition which is attributed to oxidized etching by-products, WO@sub 3@. In this study, we developed a RLSA (Radial Line Slot Antenna) microwave plasma source, and evaluated it on the W etching process. It can generate uniform surface-wave plasma with low electron temperature without magnets,@footnote 2,3@ and therefore it has compact chamber which reduces gas residence time. As for gas chemistry, N@sub 2@ addition was evaluated along with Cl@sub 2@+O@sub 2@ gases condition. As a result, we obtained high selectivity>5, W etch rate>100nm/min and straight W profile under the condition of fairly low stage temperature=60°C. We also found N@sub 2@ gas addition in high flow rate was effective to achieve both high selectivity and good profile. The role of nitrogen appeared to contribute to variety of radicals in the plasma rather than nitridation of Poly-Si and W surface. It probably controls the amount of reactive Cl and O radicals then reduces oxidization of by-products and Poly-Si etching rate. Furthermore, no charge-up damage has been observed on antenna MOS structure under any conditions. We believe that the high density plasma with low electron temperature and short residence time of gases lead to those performances. @FootnoteText@ @footnote 1@ T. Umezawa et.al., 1998 Dry Process Symposium, p49.@footnote 2@ H. Kokura et.al., 1999 Dry Process Symposium, p209.@footnote 3@ T. Ohmi, Semiconductor Manufacturing, Nov.2003, p110.

PS-MoP12 Extremely Thin Silicon Oxide Formation Using Pulse-Time-Modulated Oxygen Neutral Beam*, **C. Taguchi**, S. Fukuda, S. Noda, S. Samukawa,* Tohoku University, Japan

For next generation ULSI devices, high-k gate dielectric film is promising candidate since it provides both low gate-leakage and minimal electrical thickness in inversion. It is also important to form ultra-thin SiO@sub 2@ film between high-k film and Si substrate to avoid forming silicate. To minimize EOT of gate dielectric films, sub-1 nm fine thin SiO@sub 2@ film formation is indispensable. However, it is much difficult for conventional thermal-oxidation-processes to realize the requirement. To break through the problem, we proposed pulse-time-modulated neutral beam oxidation. In this new method, low energy (less than 10 eV) O@sub 2@ neutral beam radiation was modulated to the silicon substrate at the time constant of a few tens of μ seconds. That is, the oxidation process was modulated on the silicon surface. We first found that the SiO@sub 2@ thickness could be precisely controlled by changing the beam-on time in the pulse-time-modulated O@sub 2@ neutral beams without any radiation damages. It is speculated that the injected O@sub 2@ was diffused at a time constant of a few tens of μ seconds in the silicon. As a result, extremely thin SiO@sub 2@ film of less than 1 nm (minimum thickness:0.5 nm) could be formed on the silicon substrate by using the pulsed O@sub 2@ neutral beams. Our newly developed method is promising candidate to replace the thermal-oxidation-processes.

PS-MoP14 A Comparative Study on Dry Etching of TaN/HfO@sub 2@ Gate Stack Structure in Inductively Coupled Plasmas using Cl@sub 2@, BCl@sub 3@, and HBr Chemistries*, **M.H. Shin**, M.S. Park, N.-E. Lee,* Sungkyunkwan University, Korea*; J.Y. Kim,* Kookmin University, Korea, Rep. of Korea

Development of advanced high-k gate dielectrics and its integration into advanced nano-scale CMOS devices below 50-nm technology node has gained considerable attention recently because of the need for the replacement of ultrathin SiO@sub 2@ or nitrided SiO@sub 2@ gate dielectrics. For the integration of the high-k gate dielectric materials in the nano-scale CMOS devices, metal gate electrodes are expected to be used in the future. Currently, the metal gate electrode materials including TaN, TiN, HfN, WN, TaSiN and metal silicides are being widely studied for next generation devices with high-k gate dielectrics. Among many integration issues, selective etching of metal gate electrodes and the high-k gate dielectrics over the Si substrate is expected to be one of critical steps in the process integration of the front-end of the line (FEOL). In this work, as a

model system for studying the etching characteristics of the metal gate electrode/high-k dielectric stack structures and etch rate selectivity of the metal gate electrode over the high-k dielectric layer, TaN/HfO@sub 2@ gate structure, was chosen. ICP etching characteristics of TaN(150nm)/HfO@sub 2@(80nm) gate stack structures on Si substrate were investigated by varying the process parameters such as etch gas mixing ratios (Cl@sub 2@/Ar/O@sub 2@, BCl@sub 3@/Ar/O@sub 2@, and HBr/Ar/O@sub 2@), the top electrode power, the DC self-bias voltage (V@sub dc@), and working pressure in an ICP etcher. To understand the role of etch gas chemistry in ICP etching, the relative change in the densities of ion radical and chemical binding states of etched TaN and HfO@sub 2@ surfaces were measured by optical spectroscopy (OES) and X-ray photoelectron spectroscopy (XPS), respectively. The results of the etch rate and etch selectivity of SiO@sub 2@ to HfO@sub 2@ measured as a function of the various process parameters will be discussed in detail in conjunction with the OES and XPS analysis data.

PS-MoP15 Etching of Titanium Nitride*, **D. Wu,** B. Ji, E.J. Karwacki,* Air Products and Chemicals, Inc.

Titanium nitride (TiN) has many emerging new applications within semiconductor industry. It is being employed as a diffusion barrier in contacts, vias, trenches, and interconnect stacks, as well as an electrode material. The film is typically deposited by way of a batch CVD technique within a quartz tube furnace at a temperature lower than 150ºC. A cleaning method that removes TiN deposits from the inner surfaces of the deposition chamber, but does not damage the furnace is urgently needed by the industry. In this paper we report on our efforts to develop an effective process for TiN deposition chamber cleaning. Using our lab reactor as a screening tool, a variety of reactive gases and process conditions has been screened. For example, we have tested a thermal process using NF3, Cl2, and 5%F2. In each case, a temperature of higher than 200ºC is needed to start the etching reaction. To reduce the required temperature, remote plasma is used together with the thermal process. The process using remote NF3 plasma etches TiN at a rate of 1000 nm/min with a TiN/SiO2 selectivity of 8 at 140ºC. Surface analysis is also conducted to understand the etching mechanism.

PS-MoP16 Etching of Narrow Porous SiOCH Trenches using a TiN Metallic Hard Mask*, **M. Darnon,*** CNRS LTM - France, France*; N. Posseme,* ST Microelectronics - France*; D. Eon,* UJF - France*; T. David,* CEA LETI - France*; T. Chevolleau,* CNRS LTM - France, France*; L. Vallier,* CNRS LTM - France*; O. Joubert,* CNRS LTM - France, France

In CMOS technology, most of the interlayer dielectric materials achieve low k values by introducing porosity in order to reduce the total resistance capacitance (RC) delay in the interconnect levels. Trench or via patterns are transferred into porous SiOCH (p-SiOCH) using a dual hard mask strategy. This approach minimizes the porous low k degradation induced during ash plasma exposure. Different hard masks (metallic such as TiN or TaN and inorganic such as SiO@sub 2@ or SiC) are currently under investigation to pattern 65 nm trenches targeted for the 45 nm node. This work is dedicated to the analysis of the impact of a metallic hard mask used to pattern narrow porous SiOCH trenches etched in fluorocarbon based plasmas. The stack investigated is composed of 600 nm p-SiOCH, 40 nm SiO@sub 2@, 45 nm TiN and 100 nm photoresist (PR). The 200 mm wafers are patterned using direct ebeam lithography to achieve aggressive trenches dimensions down to 50 nm. After TiN opening and resist removal, the SiO@sub 2@ and p-SiOCH layers are etched in two different industrial etching chambers: either an inductive (ICP) or a capacitive (MERIE) plasma source. Chemical topography analyses by X Ray Photoelectron Spectroscopy (XPS) and ion mass spectroscopy show that the condensation of low volatile Ti based etch by-products on the trench sidewalls can generate severe profile distortions. The profile distortion is strongly minimized and even suppressed by increasing the wafer temperature from 20°C up to 60°C. The TiN hard mask consumption during the dielectric etch process can be reduced by using highly polymerizing chemistries which contributes to the formation of a fluorocarbon overlayer on top of the mask. The patterning of very narrow trenches reveals that one of the main issues is the faceting of TiN hard mask, leading to unacceptable profile distortions. The impact of the plasma parameters on the profile distortion of narrow trenches will be presented and discussed.

PS-MoP17 A Stacked Mask Process (S-MAP) for Precise CD Control using 100 MHz CCP RIE*, **H. Hayashi,** J. Abe, A. Kojima, I. Sakai, T. Ohiwa,* Toshiba Corporation, Japan

The stacked mask process (S-MAP)@footnote 1@ has been developed to provide improved critical dimension (CD) control in deep UV lithography, where it is necessary to use thin photo resist (P.R.) susceptible to etch erosion. In S-MAP, the P.R. pattern is first transferred to a spin-on-glass (SOG) layer, then to spun-on carbon film. An oxygen-based chemistry has been widely used for organic film etching. However, it tends to cause a bowed profile due to excess oxygen radicals. Therefore, a nitrogen-based chemistry is often used, where a straight profile can be obtained because of the sidewall protection effect by nitrogen. But, when the nitrogen-based chemistry was applied to the etching of stacked film structure such as S-MAP, the SOG film peeled at the interface of SOG and carbon films during etching under some conditions. The mechanism of SOG peeling in nitrogen-based chemistry was examined by analyses of the SOG/carbon stacked film after etching, and it was found that nitrogen gas was trapped in the stacked film. On the other hand, the SOG surface exposed to the plasma was densified by ion irradiation. It is assumed that, as etching progressed, nitrogen molecules gradually accumulated in the stacked film until the nitrogen gas pressure in the film became high enough to cause SOG peeling. By using the 100 MHz capacitive coupled plasma (CCP) which can realize low pressure and low ion energy simultaneously, carbon film etching using nitrogen-less gas chemistry without bowing was realized, by suppression of oxygen radical density at low pressure. Furthermore, selectivity to SOG improved because of the low ion energy, and CD loss due to SOG erosion was reduced. In conclusion, S-MAP for the 55 nm pattern size with precise CD control was realized by using 100 MHz CCP RIE using nitrogen-less gas chemistry. @FootnoteText@ @footnote 1@J. Abe et al., Symp. Dry Process, (2001) 187.

PS-MoP18 Characterization Methodologies for Unsaturated 1,3-C4F6 Plasma used to Investigate Aspect Ratio Dependent Etch and Etch Characteristics with Comparison to Saturated C-C4F8*, **T.L. Anglinmatumona,*** San Jose State University*; C.T. Gabriel,* Advanced Micro Devices*; E. Allen,* San Jose State University

The scaling of device features below 65 nm may encounter severe challenges such as the mass transport of CF2 and CF polymer precursors to the bottom of the feature due the generation of large molecular-weight radicals in saturated chemistries. As aspect ratios continue to increase due to the shrinking of the via hole diameter, saturated chemistries such as octafluorocyclobutane (c-C@sub 4@F@sub 8@) will no longer provide the etch performance required for ULSI. Hexafluorobutadiene (1,3-C@sub 4@F@sub 6@) is being proposed as an alternative gas to c-C@sub 4@F@sub 8@ for via etching in an inductively coupled plasma system. Profile slope, etch selectivity, CD bias and etch rates were investigated as a function of cathode temperature, rf bias power and chamber pressure. Optimum process conditions were identified based on a statistical design of experiment. Hexafluorobutadiene at optimized process conditions improved the etch parameters overall by 2X in comparison to c-C@sub 4@F@sub 8@. Aspect ratio dependent etching (ARDE) was reduced due to 1,3-C@sub 4@F@sub 6@ unsaturated bond configuration and improved process conditions.

PS-MoP20 Effects of N@sub 2@ Additive Gas on Etching Characteristics of Silicon Oxide Layers in F@sub 2@/N@sub 2@/Ar Remote Plasmas*, **J.Y. Hwang,** D.J. Kim,* Sungkyunkwan University, South Korea*; N.-E. Lee,* Sungkyunkwan University, South Korea, Korea*; C.Y. Jang, G.H. Bae,* ATTO, Korea

In this study, remote plasma etching characteristics of silicon oxide layers were investigated in F@sub 2@/Ar and F@sub 2@/N@sub 2@/Ar plasmas. A toroidal-type remote plasma source was used for the generation of remote plasmas. The effect of additive N@sub 2@ gas on the etch rates of various silicon oxide layers, including PE-oxide (deposited by PECVD using SiH@sub 4@ and N@sub 2@O), O@sub 3@-TEOS oxide (deposited by thermal CVD using ozone and TEOS precursor) and BPSG (borophosphosilicate glass), was investigated by varying the various process parameters, such as the additive gas N@sub 2@ flow rate and the substrate temperature. The species emitted during cleaning were monitored by Fourier transformed infrared spectroscopy (FT-IR) and residual gas analysis (RGA). The etching rate of the silicon oxide layers is increased 20~25% by adding N@sub 2@ gases to the optimized F@sub 2@/Ar chemistry. Under the current experimental conditions, the largest increase in the etch rate of the silicon oxide layers was observed at the flow condition of F@sub 2@:N@sub 2@=2:1. The etch rates of the silicon oxide layers were increased by the factors of 8.7, 8.3, and 35.7 for PE-oxide, O@sub 3@-TEOS oxide, and BPSG, respectively, at the conditions of F@sub 2@(1500 sccm)/N@sub 2@(750 sccm)/Ar (500 sccm) as the substrate temperature increases from 25 to 350°C. The additive N@sub 2@ flow rate and the substrate temperature were found to be the most critical parameters in determining the etch rate of the silicon oxide layers.

PS-MoP21 Comparison of C@sub 4@F@sub 6@ with C@sub 4@F@sub 8@ Chemistry for Deformation of ArF Photoresist and Silicon Dioxide Etching using Dual Frequency Superimposed (DFS) Capacitive Coupled Plasmas*, **C.H. Lee**, C.H. Park, N.-E. Lee,* Sungkyunkwan University, Korea

As the critical dimension (CD) of advanced CMOS devices is scaled down below 100 nm, 193 nm ArF photoresist (PR) needs to be used as a mask for various etching processes including silicon nitride (SiN) hard-mask opening. Recently, dielectric etch process using ArF photoresist mask by dual frequency superimposed (DFS) capacitive coupled plasma (CCP) has attracted a lot of attention. High frequency (HF) power is used to enhance plasma density and low frequency (LF) power is used to control ion bombardment to the wafer. During dielectrics etch process using DFS-CCP, understanding of ArF photoresist deformation is very important. It has been found that the most serious problems of the hard-mask open process with ArF PR are striation, wiggling, and agglomeration of the PR. In this study, we investigated deformation of ArF photoresists and silicon dioxide etching by varying the process parameters such as HF(13.56, 27.12, and 60 MHz)/LF(2 MHz) power ratio, O@sub 2@ flow, CH@sub 2@F@sub 2@ flow rate and etch chemistry (C@sub 4@F@sub 8@ or C@sub 4@F@sub 6@/ CH@sub 2@F@sub 2@/ O@sub 2@/ Ar). Characterization of surface chemical change was performed by X-ray photoelectron spectroscopy (XPS). Surface morphological changes also investigated by field emission scanning electron microscopy (FE-SEM) and atomic force microscopy (AFM). Also, morphological changes of surface and line edges in ArF PR, SiO@sub 2@ etch rate, selectivity over PR during etching of ArF PR/BARC/SiO@sub 2@ structures were investigated. Effects of process parameters on the etch results will be discussed in detail.

PS-MoP22 Influence of the Positive Ion Composition on the Ion-Assisted Chemical Etch Rate of SrTiO@sub 3@ Thin Films in Ar/SF@sub 6@ Plasmas*, O. Langlois, L. Stafford, **J. Margot**,* Universite de Montreal, Canada*; M. Gaidi, M. Chaker,* INRS-Energie, Materiaux et Telecommunications, Canada

The control of the etch rate is one of the critical issues related to the patterning of functional thin films relevant for applications in electronic, opto-electronic and optical integrated devices. This etch rate is known to be strongly influenced by the reactive neutral and total positive ion density, by the positive ion energy, and by the surface temperature. For plasmas sustained in molecular gases such as BCl@sub 3@, CF@sub 4@, C@sub 4@F@sub 8@, and SF@sub 6@, more than one positive ion species can be present simultaneously in the plasma. It is therefore likely that in addition to the previous parameters, the relative concentration of each positive ion species somewhat impacts the etch rate. In this work, we investigate the influence of the positive ion composition on the ion-assisted chemical etch rate of strontium-titanate-oxide (SrTiO@sub 3@) thin films in Ar/SF@sub 6@ plasmas, using a parametric approach. In this context, we characterize the influence of the operating parameters (e.g. gas pressure and absorbed power) on the positive ion density of each charged species by using plasma sampling mass spectrometry and Langmuir probes. It is found that as either the gas pressure increases or the absorbed power decreases, the relative concentration of molecular positive ion species such as SF@sub 3@@super +@ and SF@sub 5@@super +@ strongly increase. Based on these results, it is possible to define an effective positive ion mass M that describes the overall positive ion composition of the plasma. The SrTiO@sub 3@ etch yield Y (i.e. the number of atoms desorbed from the surface per incident ion) is shown to be a decreasing function of the effective ion mass M, in excellent agreement with the predictions of a simple ion-assisted chemical etching model.

PS-MoP23 In Situ Etching of (Pb,Sr)TiO@sub 3@ Thin Films by using Inductively Coupled Plasma*, **G.H. Kim**, K.T. Kim, C.I. Kim,* Chungang University, Korea

To overcome the limitations of conventional capacitor structure, high-k material, for example, (Ba,Sr)TiO@sub 3@ (BST) and (Pb,Sr)TiO@sub 3@ (PST), have been intensively studied for a number of integrated devices such as dynamic random access memories (DRAM) because high dielectric constant, lower crystallization temperature and low leakage current. However, BST thin film possesses a satisfactorily characteristics, it was known that a post heat treatment at a high temperature was essential to obtain good electrical property. The heat treatment at high temperature can cause deleterious effects on an electrode, barrier metal, and contact plug. On the other hand, PST thin film can be a promising material due to its high dielectric constant, paraelectricity at normal operating temperature and good electrical properties. In this study, inductively coupled plasma etching system was used for PST thin film etching. The chlorine base plasmas were characterized by optical emission spectroscopy (OES), Langmuir probe and quadrupole mass spectrometer (QMS) analysis. OES and QMS were used for the analysis of byproduct.

PS-MoP24 Surface Etching Mechanism of Bi@sub 4-x@La@sub x@Ti@sub 3@O@sub 12@ Thin Films using Quadrupole Mass Spectroscopy and X-ray Photoelectron Spectroscopy*, **J.G. Kim**, G.H. Kim, K.T. Kim, C.I. Kim,* Chungang University, Korea

Ferroelectric thin films are employed for ferroelectric random access memories (FeRAMs). FeRAMs offer non-volatility, a lower voltage operation and larger write cycle numbers. (Bi@sub 4-x@La@sub x@)Ti@sub 3@O@sub 12@ (BLT) thin films was proposed as a promising ferroelectric material that does not exhibit the polarization fatigue, does have bigger remanent polarization value than that of SrBi@sub 2@Ta@sub 2@O@sub 9@. Accordingly, for high density FeRAMs, the etching mechanism of BLT thin films must be understood by investigation of both chemical and physical reactions between plasma species and BLT thin films. In this paper, the etching properties of BLT thin films in inductively coupled Ar/Cl@sub 2@ plasma was investigated with various gas mixing ratio. For investigation of chemical reaction with ions and radicals, in-situ monitoring using quadrupole mass spectroscopy (QMS) with 250µm orifice was performed. After etching process, etched BLT thin film surface was analyzed with X-ray photoelectron spectroscopy (XPS), since etching byproducts of BLT thin films has non-volatile species and re-deposited its surface. One could explain how to react the ions and radicals on the surface of BLT thin films to combine the QMS scanning data and the analyzed data of XPS spectrum.

PS-MoP25 The Etching Characteristics of LaNiO@sub 3@ Thin Films in CF@sub 4@/Cl@sub 2@/Ar and BCl@sub 3@/Cl@sub 2@/Ar Gas Chemistry*, G.H. Kim, K.T. Kim, **C.I. Kim**,* Chungang University, Korea*; D.P. Kim,* KDG Engineering Co., Ltd., Korea*; C.I. Lee,* Ansan College of Technology, Korea*; T.H. Kim,* Yeojoo Technical College, Korea

During the last decade, ferroelectric thin films have been attracting much attention for nonvolatile memory application. Among ferroelectric material, zirconate titanate (Pb(Zr,Ti)O@sub 3@ : PZT) thin films have been studied extensively because PZT has high dielectric constant and bistable polarization. Platinum (Pt) film usually employed as an electrode for metal-ferroelectric-metal (MFM) capacitor for 1 transistor-1 capacitor structure (1T/1C). However, Pt/PZT/Pt capacitors suffer from poor resistance on fatigue property due to generation oxygen vacancies in interface of Pt/PZT during exposing to a hydrogen environment. Therefore, metal-oxides (IrO@sub 2@ and RuO@sub 2@) have been studied for top electrode. However, IrO@sub 2@ and RuO@sub 2@ have the problems that metal-oxides are easily transferred to metallic Ir and Ru under vacuum and high temperature conditions, resulting in degradation of ferroelectric properties by H@sub 2@ diffusion. Recently, LaNiO@sub 3@ (LNO) electrodes are challenged as top and bottom electrodes. Because LNO has a pseudo cubic perovskite structure, the close lattice constant (3.84 Å) to PZT (4.04 Å) and a good metallic property. In order to realize highly integrated FRAMs, the etching process must be developed. In this case, the task of primary importance is to understand etching mechanism to open the ways for the optimization of etching process. Unfortunately, there is only one report for etching LNO thin film. Therefore, the etching mechanism of LNO films should be understood in terms of etching system and gas mixture. In this work, we investigated etching characteristics and mechanisms of LNO thin films using CF@sub 4@/Cl@sub 2@/Ar and BCl@sub 3@/Cl@sub 2@/Ar mixtures in inductive coupled plasma (ICP) system. Plasma diagnostic was represented by quadrupole mass spectrometer and Langmuir probes measurements.

PS-MoP26 Low Damage Etching of III-V Semiconductors using a Low Angle Forward Reflected Neutral Beam*, **B.J. Park**, K.S. Min, H.C. Lee, J.W. Bae, G.Y. Yeom,* Sungkyunkwan University, Korea

Plasma etching is essential in the fabrication of compound semiconductor devices due to the requirements of anisotropic profiles and submicron features for optoelectronic integrated circuits, microwave devices, lasers, etc. Any process-related damage such as electrical damage and surface modification remaining during the processing may cause serious problems due to the size limitation of the devices. Therefore, etch processes without or negligible damages are required. In this study, fluorine based directional neutral beams were formed by low angle reflection of the energetic directional fluorine-based reactive ion beams generated by a fluorine-based inductively coupled plasma (ICP) gun. GaAs and GaN were etched and their etch characteristics such as etch rates and etch damage due to the etching were investigated. As a comparison, GaAs and GaN were etched by a conventional ICP and their damage characteristics were

compared. When dry etch damage of the etched GaAs and GaN were investigated using PL and PRS, no damage could be observed when the neutral beam etching was used while the GaAs and GaN etched by the ICP showed significant surface damage. No damage by the energetic neutral beam etching appears to be related to the insignificant reaction of the neutrals with the electrically active surface states during the etching.

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