## Manufacturing Science and Technology
## Room Exhibit Hall C&D - Session MS-TuP

### Topics in Advanced Manufacturing Poster Session

**MS-TuP1 Dip-Pen Nanolithography-Based Fabrication of ZnO Microarrays**, ***I. Takahiro***, *I. Kaoru, S. Nagahiro, T. Osamu,* Nagoya University, Japan

Zinc oxide (ZnO) becomes one of the most important functional materials with unique properties of the near UV emission, optical transparency, electrical conductivity, and surface acoustic wave. Microarrays and micropatterning of functional ceramic materials are expected to provide various applications for microcircuit fabrication. Patterning and arraying techniques are useful for arranging wiring electrode. Conventionally, ZnO micro-patterns and arrays are fabricated by etching with photoresist like the lithography technique for Si. However, it is difficult to find the suitable etching conditions. To overcome the issue, site-selective growth techniques were recently developed. Dip-pen nanolithography (DPN) is a new promising scanning probe-based technique for fabricating sub-100 nm to many micrometer structures on surfaces, since it is a simple method for directly depositing material from an ink-coated atomic force microscope (AFM) tip onto a substrate with a high spatial resolution. In this study, we demonstrate the fabrication of ZnO microarrays on Au through DPN. An oxidized silicon wafer was coated with a Ti adhesion layer via thermal evaporation, which was subsequently coated with Au. DPN was then used to array ZnO microstructures on these substrates with Zn(NO3)2 solution. AFM-probe used in this study was immersed into the solution for a few minutes. The microstructures of ZnO were observed with field emission scanning electron microscope (FE-SEM).

**MS-TuP2 The Dependence of Power Trench MOSFET Processes on Wafer Thickness**, ***M. Daggubati***, *G. Sim, D. Long, H. Paravi, Q. Wang,* Fairchild Semiconductor

The dependence of trench MOSFET processes on wafer thickness has been studied in detail. In the photolithography process, it was found that the photoresist thickness decreased 30Å when wafer thickness decreased from 675µm to 508µm. This is due to the fact that thinner wafer has less thermal dissipation time i.e. Thinner wafer dissipates heat better and heats up quicker than thicker wafer during baking resulting in more evaporation of the photoresist solvent. Unless compensated for, this change in resist thickness adds to process variation affecting critical dimension (CD) and trench depth control. In the silicidation process, after the rapid thermal processing (RTP), the thinner wafers exhibited a lower resistance and higher silicide stress of 3.23E+10 dynes/cm@super 2@ (compared to thick wafers of 4.60E+09 dynes/cm@super 2@) at the source contact due to the reasons mentioned above. Also, the stress is more uniform across the wafer. The Ti/Si reaction is time and temperature dependent. Higher temperature results in more silicide and the reaction creates a volume reduction that induces stress. The silicide layers on the Si wafers have been analyzed using Z-constrast imaging in transmission electron microscopy (TEM) and energy dispersive x-ray (EDX) profiling techniques. Both Z-contrast imaging and EDX profiling revealed a 50 nm thick TiSi layer on the top of TiSi@sub 2@ layer for the thicker wafers. Whereas, no TiSi layer was found in thinner wafers, but Ti-enrichment in the outer part was sometimes observed. The TiSi layer, especially when it's continuous, can modify the electrical property of the devices. The formation of TiSi layer could be attributed to insufficient Si atoms diffused to the outer layer. Higher temperatures in thinner wafers seem to assist in the removal of this TiSi layer.

**MS-TuP5 Optimized Cu Electrochemical Plating considering Pattern Dependency in Dual-Damascene Process**, ***H.-Y. Yoo***, Chung-Ang University, Korea*; N.-H. Kim,* Chosun University, Korea*; S.-Y. Kim,* DongbuAnam Semiconductor Inc.*; E.-G. Chang,* Chung-Ang University, Korea

Since damascene technology announced, Cu metallization using electrochemical plating (ECP) has played an important role in back end of line interconnect formation. In damascene process, the problems related with process integration as well as with each unit process are becoming critical issues. Occurrence of step height (SH) and array height (AH) after Cu plating was closely related with pattern dependencies in Cu ECP and influenced in Cu chemical mechanical polishing (CMP) process. So, Cu plating target thickness in Cu ECP process was required to be optimized. In this work, we studied the optimized copper thickness in Cu ECP. In order to select an optimized Cu ECP thickness, we examined Cu ECP bulge (bump, hump or over-plating amount), Cu CMP dishing and electrical properties of via hole and line trench over dual damascene patterned wafers split into different ECP Cu thickness. In the aspect of bump and dishing, the bulge increased according as target plating thickness decreased. Dishing of edge was larger than center of wafer. Also in case of electrical property, metal line resistance distribution became broad gradually according as Cu ECP thickness decreased. In the results, 0.6 @micron@ plating condition that baseline size reduced 40% showed bad property in broad resistance distribution of metal line and dishing after Cu CMP process. In conclusion, at least 20% reduced Cu ECP thickness from current baseline; 0.8 @micron@ and 1.0 @micron@ are suitable to be adopted as newly optimized Cu ECP thickness for local and intermediate layer. Acknowledgement : This work was supported by grant No. R01-2002-000-00375-0 from the Basic Research Program of the Korea Science Engineering Foundation.

**MS-TuP7 Fabrication of High Precision Demultiplexer using Embossing Technique with Thermal Curable Polymers**, ***C.H. Choi***, *M.W. Lee, B.H. O, S.G. Lee,* Inha University, Korea*; S.G. Park,* Inha University, Korea, Korea, Republic of*; E.H. Lee,* Inha University, Korea

Photonic devices have been fabricated mainly by using the conventional lithography and etch processes. However, the costs of the conventional fabrication were remained expensive, and obviously cannot meet the trend towards fiber-to-the-home (FTTH), which required lower price of the photonic components. Embossing technologies reduce the cost for the fabrication of photonic devices. In this paper, we fabricated a 1310 nm/1550 nm demultiplexer using an embossing technique with the PDMS mold. Resists used as the core and the cladding layers are ZP 51 and ZP 49, respectively, which are the thermal curable polymers. The fabrication process is summarized as: 1) manufacturing the photoresist master by lithography process, 2) forming the PDMS mold from the master, and 3) replicating the device using the mold. For the fabrication of the device, ZP 49 was spin coated onto a glass substrate, and was cured by heating. ZP 51 was applied to the patterned surface of the PDMS mold. This mold filled with the ZP 51 was then placed in contact with the surface of the prepared substrate coated the ZP 49, and the ZP 51 was cured to solid by heating it. After curing, the mold was peeled away carefully, and the upper cladding (ZP 49) was spin coated over the patterned structure. The fabrication of the demultiplexer was completed by curing. Some manufacturing issues, such as the variation of dimension of the replica, the durability of the mold, and optical properties of the device, will be discussed. The embossing technique is applied for low-cost manufacturing photonic devices.

**MS-TuP8 Silicon Etch for Nano-photonic Structure using Hydrogen Silsesquioxane (HSQ) as a Direct Etch Mask**, ***J.K. Kim***, *J.H. Sung, K.J. Lim, B.H. O,* Inha University, Korea*; S.G. Park,* Inha University, Korea, Korea, Republic of

As a typical etch process for a Si nano-structure of high aspect ratio requires a bilayer mask or a hard mask, we have investigated the use of a hydrogen silsesquioxane(HSQ) layer as a direct etch mask for Si structure. The HSQ is known as a negative tone e-beam resist good for nanosize patterning. It has attracted lots of attention in the semiconductor industry due to its low dielectric constant, easy processability, good planarization for surfaces, as well as excellent gap fill capability in deep submicron features. In our experiment, thin HSQ layer of 90 nm-thickness was tested as a direct Si etch mask for the etch of sub-micron size hole array of 280 nm in depth and 350 nm in hole-diameter. The etch selectivity of around 2.8:1 for Si to HSQ was obtained so far using SF6-based gas chemistry in our ICP system. The systematic variation of etch parameters were studied to improve the etched wall profile and surface roughness, and the optimized results will be discussed.

**MS-TuP9 Mixed Oxidizer Effects on CMP (Chemical Mechanical Polishing) Performance of Nickel for MEMS**, ***G.-W. Choi***, *N.-H. Kim,* Chosun Univ., Korea*; Y.-J. Seo,* Daebul Univ., Korea*; W.-S. Lee,* Chosun Univ., Korea

Micro electro mechanical system (MEMS) technologies are miniaturized systems which comprise sensor, actuators and electronic functions thereby opening up a whole range of new applications and which would not be possible with purely micro electronic systems. These systems have both electrical and mechanical components. Making small machines which are almost invisible has been one of the dreams of mankind. Nickel and alloys based nickel have been found to have good mechanical properties that can be exploited to realize movable structures in MEMS devices, moreover the magnetic properties of nickel has been widely used in magnetic MEMS. In this study, the effects of oxidants on Nickel with 4 inch diameter and 3 mm thickness chemical mechanical polishing (CMP) process were investigated mixing three different oxidizers such as Fe(NO@sub 3@)@sub 3@,

KIO@sub 3@, and H@sub 2@ O@sub 2@ with MSW 2000A slurry. Moreover, the interaction between the Nickel and the oxidizer was discussed by potentiodynamic polarization test with three different oxidizers, in order to compare the removal rate of nickel-CMP and electrochemical corrosion effects on the nickel as a function of oxidizers. As an experimental result, the removal rate of nickel was calculated by measuring the weight loss of the using Shimadzu AEX-300G balance. Fe(NO@sub 3@)@sub 3@ was higher than the other oxidizers. And as concentration in each of oxidizers increased, removal rate also increased, but over the amount, it decreased. Therefore, we conclude that nickel-CMP performances are strongly dependent on the kinds of oxidizers and the amounts of oxidizer additive. Acknowledgement: This work was supported by a Korea Research Foundation grant (KRF-2004-005-D00007).

# Author Index

## Bold page numbers indicate presenter