Manufacturing Science and Technology
Room 207 - Session MS-TuA

Advanced Manufacturing Processes for Silicon Devices
Moderator: A.C. Diebold, SEMATECH

2:00pm **MS-TuA1 Magnetoresistive Random Access Memory - Manufacturing Challenges**, ***G.W. Grynkewich***, *B. Butcher, J. Chan, W. Feil, G. Kerszykowski, K. Kyler, J. Martin, J. Molla, K. Nagel, J. Ren, K. Smith, J.-J. Sun, R. Williams,* Freescale Semiconductor, Inc. **INVITED**

Magnetoresistive random access memory (MRAM) combines a magnetic tunnel junction (MTJ) with standard silicon-based CMOS to provide a unique combination of high speed read and write, non-volatility, and unlimited read and write endurance. We have produced the world's first commercially viable MRAM circuits. After a brief description of the fundamentals of an MTJ-based MRAM, we will describe the manufacturing challenges associated with the volume production of high performance MRAM parts. These include: contamination control, bit patterning, achieving and maintaining uniformity of both very thin magnetic films and the tunnel barrier, formation of cladded programming lines, and processing very thin interlayer dielectrics.

2:40pm **MS-TuA3 Controlling Ultrashallow Junction Formation through Surface Chemistry**, ***E.G. Seebauer***, *K. Dev, C.T.M. Kwok, R.D. Braatz,* University of Illinois at Urbana-Champaign

Forming extremely shallow pn junctions with very low electrical resistance is becoming an insurmountable stumbling block to the continued scaling of microelectronic device performance according to Moore's Law. We have developed a technology based on surface chemistry that holds great promise for simultaneously reducing junction depth and increasing activation for dopants implanted into silicon. The approach uses the surface as a large controllable "sink" that removes Si interstitials selectively over dopant interstitials. We have discovered a new way to employ adsorption at the surface for this task: adjusting the intrinsic loss rate of interstitials to the surface. We control the interstitial loss rate to the surface by saturating dangling bonds using adsorbed nitrogen (introduced as ammonia) before implantation or the subsequent annealing step. To demonstrate such effects, we have measured SIMS profiles of isotopically labeled Si (mass 30) implanted into a Si host lattice depleted in this isotope, The annealed profiles with an atomically clean surface change relatively little from the as-implanted profile, while the profiles with adsorbed N change much more. We have quantified the loss rate of interstitials at the surface by measuring the annihilation probability, which varies from about 0.05 on atomically clean Si(100) to about 0.0008 with only 1% of a monolayer of adsorbed N.

3:00pm **MS-TuA4 Investigation of Boron Penetration through Poly Silicon Films**, ***X.-D. Wang***, *W. Fan, S. Phillips, J. Parker, S. Schauer,* Freescale Semiconductor

Poly-Si is the most commonly used gate material in modern VLSI fabrication. It is also widely used as mask layer for dopant implantation. Such a process has the advantage of reducing lithography steps, however, it requires tight control on film property in order to effectively block undesired implantation through the film to the substrate silicon. In this paper, we investigate an implant issue related to boron penetration through the poly-Si film. Plan view scanning capacitance microscopy (SCM) analysis was performed to examine MOSFET devices which failed due to short channel. SCM images directly revealed undesired boron penetration in CMOS channel region to be the root cause of the failure. It was found that the yield was related to poly-Si deposition conditions. Multiple analytical techniques, including SCM, second ion mass spectroscopy (SIMS) and, transmission electron microscopy (TEM) were used to characterize the severity of boron penetration as function of film deposition conditions, especially the deposition temperature. By correlating to TEM analysis, it was found that the boron penetration is closely related to the crystalline properties of the film and optimal film growth parameters were obtained.

3:20pm **MS-TuA5 Investigation of Low-k Dielectric Etching using Groovy ICP Plasma Source**, *A. Kelly,* ***G.K. Vinogradov***, FOI Corporation, Japan

Plasma etching of low-k dielectric materials, such as porous materials is presenting significant challenges to their introduction in copper dual damascene device production. Plasma damage is implicated in poor retention of low-k properties. We investigated plasma damage using a narrow gap inductive plasma source, Groovy ICP. Specially developed for 300mm low-k dielectric etching, it has three independently controllable highly efficient RF coils immersed in separate grooves machined in a planar roof. Each groove generates its own plasma toroid, both radial plasma density and chemical uniformity can be optimized. We investigated sidewall damage in dual damascene stack structures over a wide pressure range for porous low-k dielectrics. Only under conditions of low pressure, 5-10mTorr and low ion energy can sidewall damage be eliminated. With separate wafer bias control of ion energy, we can distinguish between ion and radical effects on sidewall damage of low k materials. Damage is by radical attack penetrating into the sidewall; therefore low-pressure ion dominant conditions are needed. Also low ion energy is needed as high ion energy conditions can sputter damage sidewalls. Groovy ICP is capable of achieving these conditions in a narrow gap, typical for low residence time oxide etchers. This shows its unique applicability for low-k dielectric etching including oxide layers.

Author Index

Bold page numbers indicate presenter