MEMS and NEMS
Room 207 - Session MN-TuM

Micro and Nano Fabrication Techniques for MEMS & NEMS
Moderator: A.V. Sumant, University of Wisconsin

8:20am **MN-TuM1 Nanomanufacturing Using Nanotemplates for Directed Assembly of Nanoelements**, ***A. Busnaina***, Northeastern University; *J. Mead,* University of Massachusetts Lowell; *G. Miller,* University of New Hampshire; *C. Barry,* University of Massachusetts Lowell **INVITED**

The electronics industry is looking for new nanoscale technologies that will be energy efficient with high performance, scalable with gain and operational reliability at room temperature that are preferably compatible with CMOS process and architecture. Proposed nanoelectronic devices using technologies beyond currently-deployed are many; mechanical or molecular switches, spin logic, phase logic, molecular devices, cross-bar devices, cross-net devices, etc. Manufacturing of these involves very diverse fabrication and assembly techniques that may involve top-down, bottom or both. There is a need to develop heterogeneous process integration such as combination of hierarchical directed assembly techniques with other processing techniques. High-throughput hierarchical directed assembly and nanoscale components and interconnect reliability will also be essential in going beyond silicon. Another important nanomanufacturing issue is nanoscale defect mitigation and removal and defect tolerant materials, structures and processes in addition to nanoscale metrology tools, such as in-line or in-situ monitoring and feedback. Fundamental understanding and novel technology in high rate, high volume integration and assembly of robust tools and processes are addressed. Nanotemplates and tools are used to accelerate the creation of highly anticipated commercial products and will enable the creation of an entirely new generation of applications. This requires understanding what is essential for a rapid multi-step, high volume/high rate processes, as well as for accelerated-life testing of nanoelements and defect-tolerance.

9:00am **MN-TuM3 Ion Trapping in Microfabricated Ion Trap Arrays**, ***D. Cruz***, UCLA and Sandia National Laboratories; *M. Fico, A.J. Guymon, R.G. Cooks,* Purdue University; *J.P. Chang,* University of California, Los Angeles; *M.G. Blain,* Sandia National Laboratories

In this work we describe the microfabrication and testing of cylindrical ion trap arrays. The ion trap has become an essential tool in several areas of physical science, including mass spectrometry, atomic frequency standards, studies of fundamental quantum dynamics, and quantum information science. Many of these applications benefit from miniaturized ion traps at dimensions several orders of magnitude below the current centimeter and millimeter scale. Our design of the individual trap array element consists of two endcap electrodes, one ring electrode, and a detector/collector plate, fabricated in seven tungsten metal layers by molding tungsten around SiO@sub 2@ features (0.5 µm minimum dimension) using standard lithography and plasma etching techniques. Each layer of tungsten is then polished back in damascene fashion. The SiO@sub 2@ is removed using a standard MEMS release processes to realize a free-hung ion trap element. Common anchor points of adjacent elements allow for the entire array of traps to be operated in parallel. Four different sized traps were fabricated with inner radius of 1, 2, 5 and 10 µm and heights ranged from 3-24 µm. We focused our testing on the 5-µm sized ion trap array to trap toluene (C@sub 7@H@sub 8@), mass 92 amu. We discerned the electrical characteristics of the packaged ion trap arrays through vector network analyzer measurements. We ejected the ions by turning off the rf and noted a current signal. We were not able to fully determine that our signal was all due to trapped ions. However, we attained favorable trapping conditions such as a significant pseudopotential well and an ionization rate twice the ion loss rate determined by simulation. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

9:20am **MN-TuM4 Monolithic In-Plane Tunable Optical Filter**, ***J. McGee***, *N. Siwak, R. Ghodssi,* University of Maryland, College Park

The development and commercialization of future communication systems and biological diagnostic equipment will benefit greatly from dense integration of optical and electrical components through the use of in-plane, guided optics. Tunable optical filters are a necessary component for wavelength multiplexing and spectroscopy. However, in-plane devices have been challenging to produce as the very advantages of guided optics, small size and dense integration, lead to loss mechanisms that degrade the filter well below the performance of out-of-plane devices. Indium phosphide is our chosen material as its direct bandgap provides the possibility of integrated emitters and lasers while operating in the standard telecommunications bands of 1500-1600 nanometers at low loss. We recently demonstrated a functional in-plane tunable filter in indium phosphide and we have now improved its performance by utilizing a ribbed waveguide structure. The use of ribbed waveguides offers the advantage of a large beam less susceptible to divergence while providing single mode operation. In our device, an electrostatically-actuated doubly-clamped beam deflects a ribbed Bragg reflector relative to a stationary ribbed waveguide attached to a second Bragg reflector, forming a variable-length Fabry-Perot cavity. A simulation model we developed predicts a Q-factor of 90 compared to a Q-factor of 44 measured in the original device. The detailed fabrication, characterization, and measurement results will be presented.

9:40am **MN-TuM5 Cooper-Pair Molasses - Cooling a Nanomechanical Resonator with the Quantum Noise of a Single Electron Transistor**, ***K.C. Schwab***, National Security Agency **INVITED**

We are performing ultra-low temperature experiments with a radio-frequency, nanomechanical resonator coupled to a superconducting single electron transistor, a system which has demonstrated the closest approach to the uncertainty principle for continuous position detection, and the closest approach to the quantum ground state of a mechanical system.@footnote 1@ Recently, we have used the resonator to detect the asymmetric, quantum noise of the SET, which produces the back-action required by the uncertainty principle. In addition, have discovered an unexpected cooling mechanism, analogous to optical molasses, which is a result of resonant Josephson effects in the transistor: we have observed cooling of a 10 MHz, Q=230,000 mode from 500 mK to 100 mK. Using these techniques and devices, we are anticipating the observation of squeezed, superposition, and entangled states of a mechanical device. @FootnoteText@ @footnote 1@LaHaye, Buu, Camarota, Schwab, "Approaching the Quantum Limit of a Nanomechanical Resonator," Science 304, 74 (2004).

10:20am **MN-TuM7 Granular Adsorbent Loading and Wafer Bonding for Si Microcavity Preconcentrator**, ***H.K. Chan***, University of Michigan; *M. Takei,* Fuji Electric Systems; *S.W. Pang,* University of Michigan

A new technique for loading 180 to 212 µm diameter granular adsorbents and Au-Si eutectic bonding at 400 °C has been developed for filling and hermetically sealing 450 µm deep Si cavity microheaters for thermal regeneration of graphitized carbon adsorbents. This development has enabled the first wafer-level integrated, microfabricated preconcentrator for trapping parts-per-billion concentrations of volatile organic compounds (VOCs). Previous Si microheaters for preconcentrators have included anodically bonded glass and Si and Al solder bonded Si-Si using rapid thermal annealing at 850 °C, all of which were assembled at the die level due to the difficulty in loading carbon granules using dry filling methods. The newly developed adsorbent-solvent method uses the principle of solvent surface tension to confine the granules into the cavities. This method is demonstrated across a 100 mm wafer for cavities accommodating 0.8 to 1.5 mg of carbon granules. The remaining solvent in the porous carbons has to be removed to avoid outgassing during the wafer-level hermetic sealing step using Au-Si eutectic bonding. Solvent removal under vacuum and elevated temperature have been investigated for the new adsorbent-loaded cavity microheaters. The resulting bonded wafers after loading of carbons and removal of the solvent have bonding strengths of >3 MPa under a tensile load for Au-Si eutectic bonding at 400 °C. The result of the new adsorbent-solvent loading, solvent removal, and Au-Si eutectic bonding is the first wafer-level integrated microscale carbon granule preconcentrator which traps VOCs at room temperature and heats to 300 °C to thermally regenerate the carbons and desorb the VOCs for analysis with a microscale gas chromatograph.

10:40am **MN-TuM8 Copper Electroplating to Fill Blind Vias for 3D Integration**, ***S. Spiesshoefer***, *S. Polamreddy, R. Figueroa, J. Patel, T. Lam, L. Cai, S. Burkett, L. Schaper,* University of Arkansas

The continued demand for lower cost electronic products with decreased size, higher performance and increased functionality require improvements in the system level integration of logic, memory, and other functional integrated circuits. The formation of vertical interconnects in silicon may be one approach to provide this integration. This method involves stacking of individual die to form a highly interconnected 3D structure. One way to create an efficient 3D stack is to place electrically conductive vias through

the body of the silicon to bring the connections from top to bottom. Copper is the metal used to fill the through silicon via (TSV) structure because of the high conductivity and the common use in multilevel wiring. A process will be described in this paper to electroplate copper into small diameter (5-10 µm) vias of aspect ratio > 3. The objective of this project is to develop an electroplating process to obtain a void-free copper filled blind via. Prior to plating, vias are formed by both reactive ion etch (RIE) and deep RIE processes. The resulting via profile varies depending on the etch process chosen. Vias are lined with insulation, barrier, and seed films. The insulation, SiO@sub2@, is deposited by plasma enhanced chemical vapor deposition (PECVD) while the barrier (TaN) and Cu seed layers are deposited by sputtering. A complete and conformal copper seed layer is essential for the electroplating process. A combination of three electroplating techniques is used in this study. They consist of optimized bath composition (additive control), fountain plating, and reverse pulse plating. The goal during electroplating is to achieve a bottom-up fill, also referred to as a super fill. The process will be described that results in void-free electroplating to fill an array of blind vias as well as the related processing issues.

11:00am **MN-TuM9 A Fully Integrated Micro Plasma Electron Source in Silicon***, **E. Wapelhorst**, J.P. Hauschild, J. Müller,* Hamburg University of Technology, Germany

This paper presents the concept and the fabrication of a novel, fully integrated electron and UV light source using a micro plasma. The electron source is primarily developed for use in a micro mass spectrometer. This novel system is fabricated using standard processes in silicon e.g. DRIE based on the working principle of a micro plasma ion source as shown in.@footnote 1@ Furthermore, the RF-efficiency is increased by direct RF coupling through vias. An application of this type of electron source for ionization purposes in a micro mass spectrometer has been presented in,@footnote 2@ which uses the concept of.@footnote 1@ The electron source consists of three units: The filament, the plasma chamber, and the electron accelerator. The pressure in the plasma chamber is set to 100 Pa. To ignite a stable RF plasma in the chamber, a current pulse is driven through the filament to free electrons while the RF signal is directly applied to the RF coupler. After ignition the filament is switched off. By applying a voltage between the extraction grid and the acceleration grid electrons can be extracted from the plasma and accelerated to a defined kinetic energy. Due to its shape, the acceleration area has a focusing effect on the electron beam. The pressure in the acceleration area is less than 1 Pa. The two described pressure regimes are installed by the extraction grid which acts as pressure aperture. The system emits an electron beam with adjustable and defined energy, e.g. a 100ÂµA beam and an electron energy of 70eV. Benefits of the system are the high electron current, small dimensions (diameter of the plasma chamber is less than 1mm), the low gas and power consumption, uncritical vacuum requirements because of the small size, and the adjustable electron energy. @FootnoteText@ @footnote 1@ Plasmagestuezte Ionenquelle in Mikrosystemtechnik fuer den Einsatz in einem MMS, P.Siebert, TUHH, 2001@footnote 2@ A Micro Mass Spectrometer, G.Petzold et al. MicroTAS, 2001.

11:20am **MN-TuM10 Deep Reactive Ion Etching of Membrane-Based Devices Using a Low-Frequency Bias***, **R.J. Shul**, J. Stevens, R.P. Manginell, M.G. Blain, S.G. Rich, S.A. Zmuda, L.J. Sanchez,* Sandia National Laboratories*; M. DeVre, J. Shin, S.L. Lai,* Unaxis USA Inc.

Deep reactive ion etching (DRIE) of Si or the Bosch process is essential in the fabrication of many membrane-based devices, especially chemical and biological sensors. The process relies on the ability of the DRIE process to essentially stop on the membrane film, typically a dielectric film such as SiO@sub2@ or SiN. The ability to stop on this film is due to the high etch selectivity of Si to the membrane film. Since the SiO@sub2@ or SiN membrane is an insulator, positive charge can build up on this film upon exposure to the plasma and notching at the foot of the feature can result. The positive charge causes ions accelerated from the plasma to assume a divergent path at the Si-insulator interface and causes preferential, lateral etching of the Si at the interface, allowing a notch to form. The notch can be several microns in both the lateral and vertical dimensions and can destroy the device. Notching can be minimized and often eliminated when a low-frequency or pulsed-bias is used. In this study, we will report on the results of deep Si etching of membrane devices using a low-frequency 100 kHz bias. We will compare the results for specific device applications where both high-frequency and low-frequency biasing has been incorporated and demonstrate the relative advantages of low-frequency techniques. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

11:40am **MN-TuM11 Aspect Ratio Dependent Etching Lag Reduction in Deep Silicon Etch Processes***, **S.L. Lai**, D. Johnson, R.J. Westerman,* Unaxis USA, Inc.

MEMS device fabrications often involve 3-D structures with high aspect ratios. Moreover, MEMS designs require structures with different dimensions and ARs to co-exist on a single microchip. There is a well-documented aspect ratio dependent etching (ARDE) effect in deep silicon etching (DSE) processes. The ARDE effect can be manifested in two ways: firstly, the etch rate decreases as the aspect ratio increases for a specific feature; secondly, for features with different dimensions etched simultaneously, bigger features are etched at faster rates. For example, when a 2.5 µm-wide trench is etched simultaneously with a 100 µm-wide trench in a conventional DSE process, the resultant trench depth of the latter can be more than double that of the 2.5 µm-wide trench. Indeed, the ARDE effect causes many undesired complications to MEMS device fabrication. One of the approaches to cope with ARDE is to employ etch stop layers, such as oxide, to compensate the lag. However, disadvantages, such as notching at the silicon/oxide interface, emerges sometimes when an etch stop layer is used. At Unaxis, we have developed a proprietary technique to eliminate the ARDE effect encountered in DSE processes. Our novel technique is based on a new physical model for ARDE lag reduction. This paper presents the theoretical model and the experimental results on ARDE reduction. With controls over the passivation and etch steps employed in a TDM etch process, we have demonstrated that normal ARDE can be changed to inverse ARDE, while maintaining good etch profile in all features. DSE processes can be optimized such that ARDE is completely eliminated. In the experiments, the ARDE lag was reduced to below 3% for trenches with widths ranging from 2.5 to 100 µm; for trenches with widths ranging from 4 to 30 µm, the ARDE lag was below 2%. Such results were achieved at etch rate exceeding 2 µm/min.

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