Dielectrics
Room Exhibit Hall B - Session DI-MoP
Poster Session

DI-MoP1 Surface Preparation for Atomic Layer Deposition of High-K Oxides on Silicon Studied by XPS and SPM*, J.M. Sturm*, *A.I. Zinine, H. Wormeester, R.G. Bankras, J. Holleman, J. Schmitz, B. Poelsema,* University of Twente, The Netherlands

Atomic Layer Deposition (ALD) is regarded as a suitable deposition technique for high-K metal oxides. In order to obtain a good interface quality with the silicon substrate, preparation of the starting surface is of major importance. The initial stage of Al@sub 2@O@sub 3@ deposition from trimethylaluminium and water and growth of thin films (~ 5 nm) were studied by XPS and SPM techniques. XPS was used to determine the growth rate and chemical state of the interface and deposited film as a function of wet-chemical pre-treatment of the starting surface and the pulse time of precursor and purge pulses. Ambient AFM showed that the deposited films are microscopically rough, with a correlation length of typically 20 nm and without correlation on larger length scales. UHV STM was used to investigate the stability of a hydrogen terminated Si surface in vacuum at typical growth temperatures of 250-300 °C used in ALD growth. Starting surfaces with a high RMS roughness of about 0.6 nm resulting from a concentrated HF dip did not change significantly by annealing at pressures below 5x10@super -10@ mbar. However, annealing in a higher background pressure of 3x10@super -8@ mbar (mainly H@sub 2@O) as typically present in a deposition set-up was found to result in a decrease of the surface roughness. These results indicate the importance of in-situ preparation of the starting surface and characterization of its chemical stability.

DI-MoP2 Orientation Selective Epitaxy of CeO@sub 2@ Thin Films on Si(100) Substrates by Magnetron Reactive Sputtering Enhanced by Oxygen Radical Beams with Substrate Bias*, T. Inoue*, *M.O. Ohashi, N. Sakamoto, S. Shida,* Iwaki Meisei University, Japan*; T.W. Chiu, K. Yamabe,* University of Tsukuba, Japan

It is found that the epitaxial CeO@sub 2@(100) and CeO@sub 2@(110) layers are able to be selectively grown using reactive dc magnetron sputtering enhanced with an inductively coupled rf plasma (helicon sputtering) by controlling substrate bias and plasma power.@footnote 2@ Although many reports have been made on the growth of CeO@sub2@(110)/Si(100), recently CeO@sub 2@(100) layers have been reported to grow on atomically cleaned Si(100) surfaces with a 2x1 reconstructed structure in an ultra-high vacuum. Our method has superiority in the requirement of only practical H-terminated surfaces obtained by the usual wet cleaning process. Adopting two step growth method; ultrathin metallic Ce layer deposition at room temperature using Ce metal target followed by silicidation process at several hundreds degree C, and subsequent reactive sputtering in an Ar/O@sub 2@ mixture environment at elevated temperature, the CeO@sub 2@(100) layer epitaxy is attained applying adequate substrate bias whereas CeO@sub 2@(110) layers are grown without substrate bias. Helicon sputtering is performed at rf power of 50 W for helicon chathode coil, 120 W for helicon chathode dc plasma power and substrate bias ranging between -20 and +50 V. Growth rate is controlled in between 0.2 and 0.4 nm/s varying Ar gas flow between 4 and 15 sccm. Oxygen gas flow for reactive sputtering is 1 sccm. The orientation selection is found to be also dependent on plasma power, in other words the growth rate: upper limit in growth rate exists for (100) layer growth, beyond which (110) layer grow. Precise mapping of growth paramters, in terms of substrate bias and growth rate, for the growth of CeO@sub 2@(100) films are attained from a lot of growth experiments. In order to improve crystalline quality and to lower the epitaxial temperature, we have started to develop a novel reactive sputtering method employing oxygen free radical beams. The oxygen radical source is operated typically under the conditions; applied rf power of 50 W and O@sub 2@ gas flow of 1 sccm, whereas the intensity of free radical beams is varied controlling rf power and oxygen gas flow. We demonstrate the experimentsl results indicating its effectiveness; successful epitaxial temperature lowering and crystalline quality improvements. Chracterization of the epitaxial films are carried out using RHEED, 4-circle XRD, XTEM and AFM, including C/V and I/V measurements for getting fundamental electrical properties. This orientation selective epitaxial growth technology will be useful for device applications. @FootnoteText@ @footnote 1@ Present address: ULVAC-PHI Corp., 370 Enzou, Chigasaki 253-0084, Japan@footnote 2@ T. Inoue et al., J. Vac. Sci. Tehcnol. A 22(1), 46 (2004).

DI-MoP3 Characteristics of Mo@sub x@Si@sub y@ Gate Electrodes for Advanced CMOS Applications*, P. Sivasubramani*, *P. Zhao, I.S. Jeon,* University of Texas at Dallas*; J. Lee, J. Kim,* Kookmin University, Korea*; M. Kim, B.E. Gnade, R.M. Wallace,* University of Texas at Dallas

Metal gates have been investigated to overcome several challenging issues such as poly-depletion and B penetration for conventional poly-Si gates. Recently, the dual metal gate approach has attracted attention to improve CMOS performance, as opposed to mid-gap metals, such as TiN and TaN. For CMOS integration, tunable metals may be suitable for metal gate applications. Alloying and implantation are being considered as possible techniques to tune the metal gate workfunction. In particular, silicidation is an acceptable process for Si IC fabrication. In this study, we investigated the characteristics of the Mo-Si alloy system for dual metal gate applications. Mo has been demonstrated as a possible P-MOS gate metal because of its high work function and good thermal stability. In this presentation we focus on the tunability of work function, thermal stability and electrical characteristics of Mo silicide as a function of Si concentration. Mo silicide has three different stable silicide phases, Mo@sub 3@Si, Mo@sub 5@Si@sub 3@ and MoSi@sub 2@. Mo silicide samples were prepared on SiO@sub 2@ on Si wafers. The samples were annealed by RTA for 15sec. up to 1000°C. We observed metal work function tuning of at least 0.5V by changing the composition. We also found a possible thermal instability issue of MoSi@sub 2@, even at room temperature. The dependence of characteristics on composition will be discussed based on XPS, XRD, RBS, TEM, CV and IV results. This work is partially supported by the TATP (Texas Advanced Technology Program) and COSAR (Collaborate Project for Excellence in Basic System IC Technology-Korea).

DI-MoP4 TiN/Ta@sub 2@O@sub 5@/PE-SiN/TiN MIM Capacitor for RF and Mixed Signal IC Applications*, Y.S. Chung*, *K.S. Kim, Y.S. Ryu, S.B. Hwang, C.-S. Shin,* Hynix Semiconductor Inc., Korea*; S.-G. Park,* Hynix Semiconductor Inc., Korea, Korea, Republic of*; J.K. Lee,* Hynix Semiconductor Inc., Korea, S. Korea

Ta@sub 2@O@sub 5@ / PE-SiN MIM capacitors with high capacitance density of 4.7 fF/µm @super 2@ for mixed-signal / RF applications were originally integrated by adopting 120Å-thick-PE-SiN as a barrier layer between bottom electrode and 80-Å-thick MOCVD Ta@sub 2@O@sub 5@ layer. Inserting PE-SiN layer resulted in dramatic reduction of leakage current at -3.3 V from 8.0E-5 A/cm@super 2@ with only Ta@sub 2@O@sub 5@ film to 9.3E-8 A/cm@super 2@ with Ta@sub 2@O@sub 5@/PE-SiN layers. We attribute the huge reduction in leakage current for the laminated structure that the PE-SiN layer provides high barrier height as well as a physical diffusion barrier against oxygen into the bottom electrode. These laminated MIM capacitors also showed good linearities of capacitance with 302 ppm/V@super 2@, 125 ppm/V, and 30.7 ppm/°C as well as an excellent matching property with 0.79 % µm. Breakdown voltage of capacitor was about 6 MV/cm and the life time (time-to-breakdown) of Ta@sub 2@O@sub 5@/PE-SiN MIM capacitor at 3.7 V and 25°C was 198000 years. Quality factor of 55 and capacitance density of 5.08 fF/µm @super 2@ at 2.4GHz were obtained for 10X10 µm @super 2@ MIM capacitor.

DI-MoP5 The Physical and Electrical Characteristics of p@super+@-Polycrystalline-Si and Si@sub1-x@Ge@subx@(x=0.27)/High-k Gate Dielectric (AlN and Al@sub2@O@sub3@) Films*, C. Lee*, *J.Y. Park, C.H. Hwang, H.J. Kim,* Seoul National University, Korea

The polycrystalline (poly) Si@sub1-x@Ge@subx@(x=0.27) gate has been also investigated as a substitute of poly-Si gate, which seems not to be suitable for new high-k dielectrics and gives rise to troubles due to poly-depletion effect (PDE) and boron penetration. We investigated the compatibility between the poly-Si@sub0.73@Ge@sub0.27@ gate and high-k gate dielectrics in terms of the boron and germanium diffusion behaviors and electrical characteristics of stack structures, which were prepared with or without a capping or bottom AlN layer on high-k Al@sub2@O@sub3@ of MOS capacitors. The metal-oxide-semiconductor (MOS) capacitors characterized in this experiment include various high-k gate dielectric stacks such as p@super+@-poly-Si gate/ Al@sub2@O@sub3@/n-type Si, p@super+@-poly-Si@sub0.73@Ge@sub0.27@ gate/Al@sub2@O@sub3@, AlN-Al@sub2@O@sub3@, or AlN-Al@sub2@O@sub3@-AlN/n-type Si. High-k dielectrics like Al@sub2@O@sub3@ and AlN films were deposited on n-type Si (100) wafers with a resistivity of 4~8 @ohm@cm by atomic layer deposition (ALD) technique using Al(CH@sub3@)@sub3@, O@sub3@, and NH@sub3@ at 400°C after RCA SC1 and diluted HF cleaning. The physical thickness of the AlN films was controlled very thin (~ 0.5 nm). Post deposition annealing (PDA) of the samples was performed with rapid thermal annealing (RTA) at 800°C in N@sub2@ for 30 seconds. Post-metallization annealing (PMA) was performed at 400°C for 30 min under a 5% H@sub2@ + 95% N@sub2@ atmosphere. Capacitance equivalent thickness (CET) decreased by approximately 30 % for the p@super+@-poly-Si@sub0.73@Ge@sub0.27@ gate compared to the p@super+@-poly-Si gate with the Al@sub2@O@sub3@ films at the same physical thickness, which resulted from the improved PDE. Leakage current density of MOS capacitors with AlN barrier layers shows a lower value compared to that of the single Al@sub2@O@sub3@ film due to the enhanced boron blocking properties.

DI-MoP6 Structure Properties and Thermal Stability of Plasma Oxynitrided Hf and Zr Thin Films*, **Yi-Sheng Lai**, L.-M. Chen, C.-H. Lu, J.S. Chen,* National Cheng Kung University, Taiwan

Thermal stability is a critical issue in replacing conventional SiO@sub 2@ gate dielectrics with high-@kappa@ materials. The interlayer (IL) growth as well as the interface reaction is of particularly concern in this respect. Growth of the low-dielectric-constant IL usually increases equivalent oxide thickness (EOT) of the high-@kappa@/IL structure, leading to the applicability in the downscaling of the electronic devices. Accordingly, engineering of the interface becomes a challenging issue in fabricating high-@kappa@ gate dielectrics. In this work, we study the characteristics of plasma oxynitrided Hf and Zr thin films. A 50-Å thick Zr or Hf metal film is first deposited on the Si surface and followed by plasma oxynitridation on these metal films in a mixture of N@sub 2@O+NH@sub 3@ ambient. Incorporation of O and N leads to the formation of ZrO@sub x@N@sub y@ and HfO@sub x@N@sub y@ films. The increased nitrogen content is found to increase the onset of the crystallization temperature in both ZrO@sub x@N@sub y@ and HfO@sub x@N@sub y@ films. Growth of the IL examined from the X-ray photoelectron spectroscopy is also dependent on the incorporated nitrogen content. The thermal stability related to the difference of nitrogen content between ZrO@sub x@N@sub y@ and HfO@sub x@N@sub y@ films is also addressed.

DI-MoP7 Valence Band Offsets and Interface Structure of Hf@sub X@si@sub 1-X@o@sub 2@ Films on Si(111) from Photoemission Spectroscopy*, **L. Fleming**,* North Carolina State University*; M.D. Ulrich,* Army Research Office*; C. Hinkle, J.G. Hong,* North Carolina State University*; J.E. Rowe,* University of North Carolina*; G. Lucovsky,* North Carolina State University*; A.S.-Y. Chan, T.E. Madey,* Rutgers University

We have used synchrotron radiation to perform high resolution soft x-ray photoemission spectroscopy measurements on device-quality Si(111)/Hf@sub x@Si@sub 1-x@O@sub 2@ films. Our samples included both thick (~ 75 Å) and thin (~ 10 Å) silicate films. In addition, we grew SiO@sub 2@/HfO@sub 2@/SiO@sub 2@ layered films for interface studies. All samples were grown by remote plasma enhanced chemical vapor deposition at a temperature of 300 °C using hafnium tert-butoxide and silane in a helium carrier gas. After growth, thin film silicate samples were heated by rapid thermal annealing at 500 °C for 30 s, while the thick film silicates and layered structures were annealed at temperatures between 500 and 900 °C. Si 2p and Hf 4f core levels were studied along with valence band spectra using photon energies of 70, 100, 130, 150 and 170 eV. Core-level binding energies exhibit a linear dependence with alloy composition in the thick silicate films, and are expected to provide some information about the interfacial structure and relaxation behavior of the layered oxide films. We have used several photoemission methods for obtaining the band offset parameter as a function of the Hf/Si composition including edge extrapolation and core-level shift data. The linear edge approximation yields a valence band offset of ~ 2.9 ± 0.1 eV for an ultrathin film of HfSiO4. This value agrees with estimates of 3.0 - 3.1 eV based on unpublished tunneling data. Valence band offsets for other compositions will be presented based on data from thick oxide films.

DI-MoP8 Dry Etching of HfO@sub 2@ Films by Inductively Coupled Plasma*, **S.-K. Yang**, H.-Y. Song, S.-G. Lee, B.-H. O, I.-H. Lee, C.-W. Kim,* Inha University, South Korea*; S.-G. Park,* Inha University, South Korea, Korea, Republic of

Not only deposition of high quality high-k dielectric layer but its dry etching is very important for fabrication of complete gate stack structure. In this study, 2000Å thick HfO@sub 2@ films are deposited on Si wafers for etching experiments by reactive sputtering and annealed in oxygen. Dry etching of HfO@sub 2@ is investigated in Cl@sub 2@, SF@sub 6@, HCl or Ar based ICP plasma. Etching characteristics are investigated in terms of RF powers, chamber pressures and gas compositions. It is found that physical sputtering effect enhances the formation of volatile hafnium halides. Single etching recipe is successfully used to pattern multiple layers of Pt/HfO@sub 2@/Si structure.

DI-MoP9 Structural and Optical Properties of Erbium-doped Ba@sub 0.7@Sr@sub 0.3@TiO@sub 3@ Thin Films*, **S.Y. Kuo**,* National Science Council, Taiwan, R.O.C.*; W.F. Hsieh,* National Chiao Tung University, Taiwan

The Er-doped Ba@sub 0.7@Sr@sub 0.3@TiO@sub 3@ (BST:Er) thin films prepared by sol-gel technique have been investigated by means of x-ray diffraction (XRD), Raman, C-V, and photoluminescence (PL) measurements. While the sintering temperature is increased from 600°C to 700°C, the peaks of the XRD patterns become sharper and more intense, indicating better crystallinity and larger grain size. On the other hand, the crystallinity becomes worse as a result of phase separation and charge compensation mechanism when sintering temperature is above 700°C. We have shown that the addition of Er-dopant does not reduce the dielectric property of BST thin films in C-V measurement. Excitation-dependent PL studies indicate that these emission peaks do not shift with the change in excitation power, whele the integrated intensity increases exponentially with the increase in excitation power. Additionally, green emission intensities of the BST:Er films increase as the Er doping concentration increases from 1 to 3 mol%, and then quench due to the presence of clusters as doping concentration exceed 3 mol%. Besides, the improvement of the crystallinity of BST:Er films will result in the luminescence enhancement as well. These experimental results indicated that the BST:Er thin films might be a potential candidate for optoelectronics devices.

DI-MoP10 Comparison of Forming Gas Effects on the Ferroelectric Properties Between More-oriented and Less-oriented Pb(Zr@sub 0.53@Ti@sub 0.47@)O@sub 3@ Thin Films*, **E.S. Lee**, H.W. Chung, S.H. Lim,* Yonsei University, Korea

More-oriented and less-oriented Pb(Zr@sub 0.53@Ti@sub 0.47@)O@sub 3@(PZT) thin films were deposited by pulsed laser deposition method on (Pb@sub 0.72@La@sub 0.28@)Ti@sub 0.93@O@sub 3@ buffer and Pt/Ti/SiO@sub 2@/Si substrate, respectively, which were observed by XRD patterns. These films were annealed in H@sub 2@-contained ambient for 30 minutes at the substrate temperature of 400 °C to evaluate the forming gas annealing effects. The comparative studies on the ferroelectric properties of these two films were carried out, which are shown that the degradation rate of the more-oriented film is lower than that of less-oriented film. These results have proven that well oriented structures can prohibit the diffusion of the hydrogen into the film.

DI-MoP11 Effect of Pb(Zr@sub 0.52@Ti@sub 0.48@)O@sub 3@ Buffer Layers on the Fatigue Resistance of Pb(Zr,Ti)O@sub 3@-Pb(Mn,W,Sb,Nb)O@sub 3@ Thin Films*, S.Y. Lee, **S.H. Lim**, E.S. Lee, H.W. Chung,* Yonsei University, Korea

The effect of a Pb(Zr@sub 0.52@Ti@sub 0.48@)O@sub 3@ (PZT) buffer layer on a perovskite Pb(Zr,Ti)O@sub 3@-Pb(Mn,W,Sb,Nb)O@sub 3@ (PMWSN) thin film deposited on a Pt/Ti/SiO@sub 2@/Si substrate was examined. The film having stoichiometric PMWSN composition was deposited directly on the Pt/Ti/SiO@sub 2@/Si substrate by pulsed laser deposition. While as-grown PZT-PMWSN thin films have poor fatigue resistance, PZT-PMWSN thin films with PZT buffer exhibit good fatigue resistance. The insertion of PZT buffer layer contributes to enhance the crystallinity of PZT-PMWSN and it can protect to diffuse the accumulated charges at the interfaces between electrodes and the films.

DI-MoP12 Comparison of Ferroelectric Properties Between PZT (Pb(Zr,Ti)O@sub 3@) -PMWSN (Pb(Mn,W,Sb,Nb)O@sub 3@) Thin Film and PZT Thin Film*, **C.S. Jeon**, E.S. Lee, H.W. Chung, S.Y. Lee,* Yonsei University, Korea

Pb(Zr,Ti)OPb(Zr,Ti)O@sub 3@-Pb(Mn,W,Sb,Nb)O@sub 3@ (PZT-PMWSN) targets were fabricated using typical bulk ceramic processes. Thin films were deposited on Pt/Ti/SiO@sub 2@/Si substrate by pulsed laser deposition. Structural characteristics were measured by XRD (X-ray diffraction). Ferroelectric properties of thin films were investigated by P-E and C-V measurements to define hysteresis loops and dielectric constants. Results of PZT-PMWSN thin films were compared with those of PZT thin films. Leakage current of PZT-PMWSN thin film was higher than that of PZT film and crystallization was less oriented than that of PZT film. But P@sub r@ (remanant polarization) and dielectric constant showed higher values than those of PZT film.

Dielectrics
Room 304B - Session DI+PS-ThA
Oxides on Semiconductors

Moderator: S.A. Chambers, Pacific Northwest National Laboratory

3:40pm **DI+PS-ThA6 Crystalline Oxides on Semiconductors, from Interface Structure to Electrical Properties***, **F.J. Walker**,* University of Tennessee*; C.A. Billman,* Penn State University*; M. Buongiorno-Nardelli,* North Carolina State University*; R.A. McKee,* Oak Ridge National Laboratory **INVITED**

From the point of view of synthesis using molecular beam epitaxy (MBE) and understanding using tools developed from first principle theory like density functional theory (DFT), a metal oxide semiconductor (MOS) device can be described as an epitaxial superlattice where each atomic layer is well-defined. This view is becoming increasingly germane to device physics as dimensions are scaled down to the atomic level. In this paper we discuss the fundamental interplay of the physical structure, as determined by reflection high energy electron diffraction (RHEED), and the electrical properties, as determined by frequency-dependent electrical impedance measurements and x-ray photoelectron spectroscopy (XPS), for the crystalline oxide on semiconductor system. We show that an interface phase is particularly important to structure and electrical properties for alkaline earth oxides grown on silicon and germanium. The interface phase begins as a surface phase of strontium silicide and transforms to an interface phase through a structural transition. The final structure and composition of the interface phase determines the band offset, interface state density and serves as a template for the epitaxial growth of the alkaline earth oxides. Office of Basic Energy Sciences, U.S. Department of Energy at Oak Ridge National Laboratory under contract DE-AC05-00OR22725 with UT-Battelle, LLC and at the University of Tennesssee under contract DE-FG02-01ER45937.

4:20pm **DI+PS-ThA8 Ultra Thin Oxides and Nitrides on Si: Growth and Properties***, **P. Morgen**, U. Robenhagen, A. Bahari,* SDU Odense, Denmark*; M.G. Rao,* IISc, India*; K. Pedersen,* Aalborg University, Denmark

Various conditions for slow growth of ultra thin silicon oxides on Si have been studied, at relatively low temperatures and pressures, in an ultra high vacuum environment. In this way a hitherto unknown regime in pressure-temperature space has been discovered including a fast (ballistic) stage terminating with a self-limiting oxidation. This precedes and deviates radically from the high temperature-high pressure Deal-Grove mechanism. Several different schemes are invented leading to oxide thicknesses from about 0.4 to 0.7 nm, with high quality of the interface and uniformity of coverage. Our present and previous studies connect the initial steps of oxygen adsorption and reaction at room temperature with the first steps (and barriers) to form three dimensional oxides on two Si surfaces (111) and (100). The structural information is obtained by following these oxidation reactions with photoemission spectroscopy, including high resolution, surface sensitive core-level photoemission; STM; LEED; optical second harmonic generation spectroscopy, and Auger electron spectroscopy. Similar procedures are followed to create ultra thin nitrides using microwave dissociated nitrogen. This process is already known to be self limiting, but at a somewhat higher film thickness than for the growth of oxides. The prospect of doping these oxides with nitrogen, and these nitrides with oxygen, is also successfully explored.

4:40pm **DI+PS-ThA9 Preparation and Properties of Clean Si@sub 3@N@sub 4@ Surfaces***, **V.M. Bermudez**, F.K. Perkins,* Naval Research Laboratory

Si@sub 3@N@sub 4@ is an important material for use in electronic devices. Thin films of Si@sub 3@N@sub 4@ are used as passivation layers and diffusion barriers in IC's and as protective coatings in disk drives. However, the basic surface science of Si@sub 3@N@sub 4@ films has been impeded by the difficulty in obtaining a clean and undamaged surface. In this work, in-situ chemical methods for preparing atomically clean surfaces of Si@sub 3@N@sub 4@ thin films in UHV have been studied using XPS, UPS, ELS and AES. Prior to UHV studies, the thin films (grown ex situ on Si(100) by LPCVD) were characterized by IR reflection-absorption spectroscopy which showed them to be stoichiometric with a low H content. A two-step process consisting of annealing in a flux of NH@sub 3@ vapor to remove C and vapor deposition of Si (followed by thermal desorption) to remove O is found to be an effective cleaning procedure. Other potential cleaning methods, such as annealing in UHV without in- situ chemical treatment or annealing in a flux of H atoms, were considered and found to be only partly effective. The clean surfaces are disordered, as seen in LEED, but show no evidence of Si-Si bonding (which would indicate N vacancies) in the Si LVV AES or in surface-sensitive Si 2p XPS. Evidence for surface- related features is seen in the N 1s XPS and in ELS data in the region of valence excitations; however, no indication of occupied surface states near the valence band maximum is seen in UPS. Preliminary results for O@sub 2@ chemisorption show adsorbate- induced features in the band gap and also evidence for a reduction in the negative surface potential due to electron traps present on the clean surface.

5:00pm **DI+PS-ThA10 STM, STS, and DFT Studies of SiO Deposition on the Ge(100) Surface***, **T.J. Grassman**, J.Z. Sexton, A.C. Kummel,* University of California, San Diego

To further the development of a germanium-based metal-oxide-semiconductor field effect transistor (MOSFET) a suitable gate-oxide material must be found which yields a high-quality, electrically-unpinned interface. For this, the semiconductor/oxide interface needs to be free of charge traps and other such interfacial defects that can cause Fermi-level pinning. High defect densities reduce the capacitance of the MOS structure and prevent the modulation of the semiconductor valence and conduction bands via the application of a gate bias. Germanium's intrinsic oxide has been shown to be inadequate for the task of providing a clean interface, therefore an alternative material must be used which can be deposited and grown on the Ge surface. To this end, we are investigating the bonding and electronic structure of the interface between SiO and the Ge(100)-p(2x1) surface using scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), and density functional theory (DFT) computational modeling. SiO can act as a precursor to SiO@sub 2@ or as a buffer layer for high-k dielectric growth. We will present atomically resolved images of both the clean Ge(100) and SiO-deposited surfaces at various coverages, along with DFT modeling results of the observed bonding structures. We find that SiO always bonds Si-end down, mostly inserting in between the Ge dimer rows and sometimes into the Ge dimers themselves. Even at modest coverages (> 5%) SiO bilayers are formed via pyramidal (SiO)@sub 3@ molecular structures with Si-O-Si-O bonding configuration. DFT-based STM simulations will be presented to aid in the interpretation of experimental STM images. We will also present STS dI/dV spectra of the associated surface electronic structure (density of states) which show that the SiO/Ge interface yields an unpinned Fermi level.

Plasma Science and Technology
Room 213A - Session PS1+DI-FrM
High K and Difficult Materials Etch

Moderator: A. Miller, LAM Research

8:20am **PS1+DI-FrM1 Inductively Coupled Plasma Etching of Poly-SiC in SF6 Chemistries**, ***S.H. Kuah***, *P.C. Wood,* SAMCO International Inc.

A study was made to find a low cost and robust etching solution for silicon carbide (SiC) using a commercially available inductively coupled plasma etching tool. Sulfur hexafluoride (SF6) was selected because of its high degree of F dissociation and non-hazardous nature. A parametric study of the etching characteristics of poly-SiC in inductively coupled plasma (ICP) SF6 chemistries was performed. Etch chemistry was found to greatly affect etch rate, selectivity, final surface cleanliness and smoothness. Etch rates as high as 5884 Å/min were achieved with high SiC/Cr selectivity (36) and clean, but relatively rough etched surfaces (134 Å RA) using a SF6/CF4/He gas mixture. It was found that He addition apparently increases the ionization of SF6 in the plasma and thus increases the SiC etch rate due to increases in the SF3+ and F radical concentrations@footnote 1,2@. The formation of pillar-like structures and side wall deposition was observed on the etched SiC surfaces under some conditions. These unwanted etch by-products exhibited a high concentration of Cr and Fluorine. However, an Ar plasma pre-clean of the the substrate, or high ICP and/or bias powers, and CF4 addition can reduce the pillars formation significantly. @FootnoteText@ @footnote 1@ J.D.Scofield, B.N.Ganguly, and P.Bletzinger, J.Vac.Sci.Technol. A 18, 2175 (2000).@footnote 2@ Z.A.Talib and M.Saporoschenko, Int. J. Mass Spectrom. Ion Processes 116, 1(1992).

8:40am **PS1+DI-FrM2 A Study of Inductively Coupled Plasma Etch of GaN/InGaN Based Light Emitting Diodes**, ***H.D. Chiang***, *K.C. Leou,* National Tsing Hua University, Taiwan, ROC*; C.H. Shen, S. Gwo,* National Tsing Hua University, Taiwan*; M.H. Wu,* Uni Light Technology Inc., Taiwan*; C.H. Tsai,* National Tsing Hua University, Taiwan

Group III-Nitride semiconductors are of considerable interest because of their potential for optoelectronic applications such as light-emitting diodes (LEDs) and laser diodes (LDs) in the visible light regions. The dry etching process is one of the critical steps in the fabrication of nitride-based LEDs. A study based on Taguchi experimental design was carried out to investigate the etch characteristics of GaN/InGaN quantum well light emitting diodes using a high density inductively coupled plasma of BCl@sub3@/Cl@sub2@-based chemistry. The process parameters studied include inductive power, bias power, BCl@sub3@/Cl@sub2@ gas ratio and chamber pressure. The etch characteristics measured were etch rate, surface roughness, side-wall angle and etch selectivity to SiO@sub2@ mask. It was found that the variations in the bias power had maximum effect on the etch rate whereas the pressure affected etch rate the least. Anisotropic profiles were generally achieved over a wide range of parameters with low substrate bias. Certain interesting phenomena such as grass and sidewall striations were observed. Nearly smooth etched surface were observed for most etch conditions. The etch mechanisms of different etch conditions on both GaN grown by MBE and MOCVD and the differences of surface roughness before and after etching will also be discussed.

9:00am **PS1+DI-FrM3 High-k Materials Etching**, ***D. Wu***, *B. Ji, S.A. Motika, E.J. Karwacki, M.J. Plishka,* Air Products and Chemicals, Inc.

As integrated circuit (IC) device geometry shrinks, high-k materials are needed to maintain adequate breakdown voltage. Due to their high chemical inertness and extremely low volatility, removal of the high-k materials has been technically challenging. In this paper, we will present an effective plasma etching process where a mixture of BCl3 and NF3 is identified as the reactive gas. Compared to pure BCl3, the etch rate for HfO2 was doubled after adding 25% NF3 to BCl3, and the etch rate for HfSixOy was also doubled after adding 15% NF3 to BCl3. Pure BCl3 did not etch ZrO2 at a condition of 0.55 W/cm2 power density and 500 mTorr chamber pressure. But an etch rate of 6 nm/min was achieved when using a mixture of 20% NF3 in BCl3. Detailed experimental setup and data analysis will be reviewed in this paper.

9:20am **PS1+DI-FrM4 Ion-Enhanced Plasma Etching of Metal Oxides in Chlorine Based Plasmas**, ***D. Ramirez***, *Y. Ta, J.P. Chang,* University of California, Los Angeles

The development of plasma etching chemistries is necessary to pattern new gate dielectric materials, such as hafnium based oxides, for sub-90nm complementary metal oxide semiconductor (CMOS) devices. An electron cyclotron resonance high density plasma reactor is used in this work to study the etching of metal oxides and their corresponding metals in chlorine based chemistries. The plasma density, electron temperature and gas phase species are characterized by a Langmuir probe, an optical emission spectrometer, and a quadrupole mass spectrometer. The etching of Al@sub 2@O@sub 3@ and HfO@sub 2@ was first studied in Cl@sub 2@ and BCl@sub 3@ plasmas, to allow for studies of the etching of hafnium aluminate, Hf@sub 1-x@Al@sub x@O@sub y@. The dominant etch products of Al and Hf metals in Cl@sub 2@ and BCl@sub 3@ plasmas were metal chlorides. However, the dominant etch products of Al@sub 2@O@sub 3@ and HfO@sub 2@ in Cl@sub 2@ and BCl@sub 3@ plasmas were metal chlorides and metal boron-oxy-chlorides, respectively. These results allowed us to assess the effect of metal-oxygen bond strength on the surface etching reactions, as well as the oxygen removal mechanism in the etching of metal oxides. Enhanced surface chlorination of the metal oxide surfaces was observed with increasing ion energy, which demonstrates that the etching reaction is limited by the momentum transfer from the ions to the film surface. The etch rates of Al@sub 2@O@sub 3@ and HfO@sub 2@ and their selectivities to Si were found to increase in BCl@sub 3@ plasmas due to the increased oxygen removal rate. Etching of Hf@sub 1-x@Al@sub x@O@sub y@ will also be presented, with a focus on predicting its etch rate based on the etching of Al@sub 2@O@sub 3@ and HfO@sub 2@ individually. Finally, the application of a generalized model, developed for the etching of ZrO@sub 2@ and HfO@sub 2@, to the etching of Al@sub 2@O@sub 3@ and Hf@sub 1-x@Al@sub x@O@sub y@ in chlorine based plasmas will be discussed.

9:40am **PS1+DI-FrM5 Investigation of Etching Properties of HfSiO and HfSiON as Gate Dielectrics**, ***J.H. Chen***, *W.S. Hwang,* National University of Singapore*; W.J. Yoo,* National University of Singapore, Singapore*; S.H.D. Chan,* National University of Singapore

Hf based high-K dielectrics have been studied as the alternative gate dielectric. For the high performance logic device application, HfSiON is receiving significant attention as the most promising dielectric material because of its good thermal stability, immunity to boron penetration and high carrier mobility in the channel under the gate. In advanced HfSiON films, N profile is optimized: the top HfSiON is highly nitrided to block boron penetration, but the bottom near Si substrate remains as HfSiO to maintain high carrier mobility in the channel. We investigated the etching properties of Hf@sub x@Si@sub 1-x@O@sub 2@ (x=0, 0.3, 0.5, 0.7 and 1) and their nitrided films in ICP of Cl@sub 2@/HBr/O@sub 2@. Results show that etch rates of HfSiO and HfSiON increase rapidly with increasing ion energy, ion density and ratio of Cl@sub 2@. Linear dependency of etch rates on the @sr@E@sub ion@, which obeys the universal energy dependency model of ion enhanced chemical etching yields, was observed with the etch threshold energies of 30-36 eV for HfSiO with different Si% in Cl@sub 2@/HBr. Etch rates of HfSiO and HfSiON are strongly dependent on the open area of the wafer because the oxygen released from these films can suppress the etching process. The addition of the small amount of O@sub 2@ to Cl@sub 2@/HBr plasma or increasing pressure can suppress the etching of HfSiO and HfSiON effectively. The 6nm thick HfSiO or HfSiON can be removed by a wet chemical of 1% HF (DHF) in 30s before anneal; after 700@super o@C anneal, etch rates drop slightly but the densified HfSiO interfacial layer (IL) of ~1nm cannot be removed in DHF. By incorporating N by the plasma nitridation, this IL can be removed by DHF in 10s, and very little Si substrate recess and clean surface can be achieved. This combined approach of the plasma etching and the wet removal proved that HfSiON can be integrated into advanced CMOS processes successfully.

10:00am **PS1+DI-FrM6 Etching of HfO@sub 2@ and HfSiO@sub x@ at Elevated Temperatures**, ***M. Hélot***, CNRS, France*; G. Borvon, T. Chevolleau, L. Vallier, O. Joubert,* LTM-CNRS, France*; P. Mangiagalli, J. Jin, Y.D. Du, M. Shen,* Applied Materials

In CMOS technology, the traditional SiO@sub 2@ used as gate dielectric is being replaced by a material presenting a higher dielectric constant (so called high-K materials) for the 65 or more likely the 45 nm nodes. In the integration of such materials, the etch process is one of key issues since the volatility of etch by-products is low and the high-K/Si selectivity seems extremely difficult to achieve. This work is dedicated to the etching of

HfO@sub 2@ and HfSiO@sub x@, two of the most promising candidates, using an industrial inductively coupled plasma source (ICP) with a hot cathode (the temperature range of the wafer can be adjusted from 200 to 350°C). Vertical high-K profile without footing or silicon recessing have been achieved. AFM measurements of silicon surface show an acceptable substrate roughness after etch. The etch process has to be adjusted with respect to the deposition technique (CVD vs. ALD) as well the thickness of the silicon oxide buffer layer between the silicon substrate and the high-K layer. XPS analyses reveal that the selectivity is obtained thanks to the formation of a thick C and Cl overlayer on SiO@sub 2@ and not on HfO@sub 2@. Even for these very thin layers, the endpoint techniques such as emission spectroscopy and spectroscopic ellipsometry have to used. Finally we found that the etch process (etch rate and uniformity) depends on the walls reactor seasoning.

10:20am **PS1+DI-FrM7 Ion-enhanced Etching of HfO@sub2@ with Cl@super+@, BCl@subx@@super+@(X = 1, 2) and SiCl @subx@@super+@(X = 1, 2,3) Ion***, K. Karahashi,* MIRAI-ASET, JAPAN*; N. Mise,* MIRAI-ASET, Japan*; T. Horikawa,* MIRAI-ASRC/AIST, Japan*; A. Toriumi,* MIRAI-ASRC/AIST, Univ. of Tokyo, Japan

As advanced high-k gate dielectrics are being developed to replace SiO@sub2@ in the near future generation of microelectronics devices, understanding their plasma etch characteristics becomes vital for introducing new materials into the manufacturing process. We report on the interactions of HfO@sub2@ with ionic species contained in plasma etching environments. To clarify the ion induced reactions of Cl@super+@, BCl@subx@@super+@(X = 1, 2) and SiCl@subx@@super+@ (X = 1, 2,3), we employed the mass-analyzed ion beam apparatus that can irradiate a single ionic species to the sample surface under an ultra-high vacuum condition. Etching yield of SiCl@sub3@@super+@ ion is about 2 times larger than that of Cl@super+@ ion, and etching products are hafnium chlorides and oxygen atom. This result suggests that chlorine atoms play a key role in etching reaction, and that the chemical etching yield increases with increasing number of chlorine atoms contained in the incident ions. The kinetic energy of etching products, which were estimated by the time delay of etching products with respects to the incident ion pulses, was larger than 0.1 eV. Therefore, products are different from thermally desorbed molecules. This indicates that desorption is caused by the momentum transfer to hafnium chloride. This work was supported by NEDO.

10:40am **PS1+DI-FrM8 Evaluation of the Effectiveness of H@sub 2@ Plasmas in Removing Boron from Si After Etching of HfO@sub 2@ Films in BCl@sub 3@ Plasmas***, **C. Wang**, V.M. Donnelly,* University of Houston

Etching of high dielectric constant ("high-K") materials in BCl@sub 3@-containing plasmas is challenging due in part to boron residue that deposits on the underlying Si or SiO@sub 2@ surface during the over-etching period. Boron is a p-type dopant and therefore it is best if it is removed prior to subsequent processing. We have investigated the effectiveness of H@sub 2@ plasmas in removing this boron-containing layer. Following etching of HfO@sub 2@ or Al@sub 2@O@sub 3@ thin films in a high-density BCl@sub 3@ plasma, including a 60s overetch period, samples were transferred under vacuum to a UHV chamber equipped with x-ray photoelectron spectroscopy (XPS). After observing B-coverages of ~1 x 10@super 15@ (equivalent of ~ 1 monolayer), the samples were transferred back to the plasma reactor for exposure to the H@sub 2@ cleaning plasma, and then re-examined by XPS. Optical emission spectroscopy was used to monitor B deposition on and removal from the plasma chamber walls. B deposition on the reactor walls during BCl@sub 3@ plasma exposure reached saturated coverage in ~2 min. Following this, the H@sub 2@ plasma removed half of this B layer in 90s, and 90 % in 320 s. B was rapidly removed (< 5s) from the BCl@sub 3@-over-etched Si surfaces provided that the walls were first cleaned in the H@sub 2@ plasma, with the Si sample held in the UHV chamber during the chamber cleaning process. Conversely, it took much longer (~170s) to remove all detectable B on the sample surface if the sample and the reactor chamber walls were cleaned in the H@sub 2@ plasma at the same time. Etching rates of SiO@sub 2@ and Si in the H@sub 2@ cleaning plasma will be reported. Mechanisms of B deposition on and removal from chamber walls and Si and SiO@sub 2@ surfaces will be discussed. A less effective sequential O@sub 2@/H@sub 2@ plasma cleaning process will also be presented. Supported by SRC and AMD Inc.

11:00am **PS1+DI-FrM9 Selective Etching of HfO@sub 2@ High-k Dielectric over Si in C@sub 4@F@sub 8@/Ar/H@sub 2@ Inductively Coupled Plasmas***, **K. Takahashi**, K. Ono, Y. Setsuhara,* Kyoto University, Japan

As integrated circuit device dimensions continue to be scaled down, increasingly strict requirements are being imposed on plasma etching technology. Regarding gate dielectrics, the technological challenge continues for growing ultrathin SiO@sub 2@ films of high quality; however, the ultimate solution relies on high dielectric constant (k) materials. In integrating high-k materials into device fabrication, an understanding of the etching characteristics of the materials is required for their removal and for contact etching. This paper presents the etch rates and possible etch mechanisms for HfO@sub 2@ thin films on Si substrate in inductively coupled plasmas containing mixtures of CF@sub 4@/Ar/H@sub 2@ and C@sub 4@F@sub 8@/Ar/H@sub 2@, as a function of gas composition and rf bias power. In the experiments, the discharge was established at a gas pressure of 20 mTorr and an rf source power of 280 W. The gas flow rates of fluorocarbon and Ar were 2.5 and 247.5 sccm (the ratio of fluorocarbon to total was 1 %). The rate of H@sub 2@ was varied between 0 and 16 sccm. As the dc selfbias voltage was maintained at the constant value of -90 V, HfO@sub 2@ and Si were etched in the CF@sub 4@/Ar/H@sub 2@ plasma with no relation to H@sub 2@ flow rate. In the C@sub 4@F@sub 8@/Ar/H@sub 2@ plasma, however, the conditions could be found where HfO@sub 2@ was etched at the rate more than 10 nm/min, and the fluorocarbon polymer deposited on Si. In this regime, it can be possible to selectively etch HfO@sub 2@ over Si. The chemical composition of the polymer was carbon-rich, and the carbon content on HfO@sub 2@ was not so much as on the polymer. It can be said that carbonized products may correspond to etch products for HfO@sub 2@. @FootnoteText@ This work was supported by NEDO/MIRAI Project.

11:20am **PS1+DI-FrM10 Characterization of the Sputtering Process in an rf Plasma for the Patterning of Nonvolatile Materials***, **T.J. Kropewnicki**, A.M. Paterson, T. Panagopoulos, J.P. Holland,* Applied Materials, Inc.

With the integration of nonvolatile materials into microelectronic devices, such as NiFe in magnetic random access memory, perovskites in ferroelectric random access memory, and HfO@sub 2@ as a transistor gate dielectric, it has become necessary to develop methods of characterizing the patterning of these materials. Removal of these nonvolatile materials by sputtering with heavy ions is probably a key component of the etching mechanism. Sputtering of materials by ion bombardment has typically been characterized using high energy ion beam systems, leading to sputtering yield probabilities as a function of ion energy. Since typical commercial plasma etch reactors use rf power to energize the ion bombardment, the usefulness of these sputtering probabilities in understanding the reaction mechanism is limited by the much lower energy levels being produced by the rf sheath, and by the spread of ion bombardment energies typically produced by an rf plasma sheath. Ion energies less than 1000 eV are common in many plasma etch systems. To create a more realistic picture of the etching process, direct measurements of the actual rf waveforms occurring on the wafer are transformed using a simple plasma sheath model into ion energy distribution functions which are then used in combination with the reported sputtering yield data to predict more accurate sputter yields for these conditions. Langmuir probe measurements of ion fluxes are then used to determine the etch rates. Comparison of these predicted rates and actual measured rates will be presented as well as possible reasons for discrepancies between the two rates.

Author Index

Bold page numbers indicate presenter