Wednesday Morning, November 17, 2004

Manufacturing Science and Technology
Room 303B - Session MS-WeM

Semiconductor Manufacturing Technologies for the 45nm Crisis

Moderator: L. Larson, Sematech

8:20am **MS-WeM1 Integration Challenges for 45nm Strained Si Devices**, ***M. Sadaka***, *A. Thean, A. Barr, T. White, B. Nguyen, V. Vartanian, M. Zavala, D. Eades, S. Zollner, Q. Xie, X. Wang, R. Liu, M. Kottke,* Freescale Semiconductor **INVITED**

As power supply voltage becomes lower with successive scaling, the non-scalability of threshold-voltage and conventional gate oxide to maintain low stand-by leakage is rapidly reducing the maximum gate overdrive factor. Enhancing carrier mobility by biaxially-straining Si on relaxed SiGe on SOI and on Bulk substrates provides a viable option to sustain the continual drive current increase. Though strained-Si addition to conventional MOSFET seems minimally disruptive, the use of SiGe in CMOS devices introduces new process and device challenges, wafer quality requirements, substrate cost issues, and new metrology requirements for strain monitoring. All these challenges need to be addressed in order to prove successful manufacturability. This talk will focus on the integration challenges of strained Si devices. The process and device challenges include Ge up-diffusion into strained Si channel, dopant diffusion differences between Si and SiGe, NiSi versus CoSi, and the need for raised source drains (formed by selective epitaxy) due to Ge segregation with cobalt silicidation. Wafer quality requirements include reducing the defect density less than 10@super 3@ defects/cm@super 2@ in order to realize yielding, high density large circuits, while maintaining maximum levels of achievable strain at a reduced wafer cost relative to the cost of SOI wafers. Finally, the appropriate metrology specific to strained Si monitoring will be discussed.

9:00am **MS-WeM3 45nm Node Architecture: The Driving Force of the Ion Implantation and Activation Processes Challenges**, ***D. Lenoble***, STMicroelectronics **INVITED**

In the current development of the 65nm node, various technical approaches regarding doping processes have been evaluated to fulfill the technology requirements of poly-gate doping, ultra-shallow junctions, channel and isolation architectures and deep gradual junctions. Low thermal budget processes (solid-phase epitaxy), advanced ion implantation processes (Plasma Doping), advanced activation processes (flash or laser annealing), stressed SiGe junctions, Poly-SiGe gate, offset spacers, 0° tilt wells implants, antimony implants, etc. are some examples of processes that are evaluated by ICMs for the 65nm node. In this paper, we propose to make a review and to discuss each technique to highlight their specific benefits and drawbacks for the manufacturing of a planar 65nm technology platform. Based on this status and on the basic requirements of the 45nm node, we build different scenarios about the major technological or architectural breaks that will emerge. Then, such projections are discussed in term of future technical challenges for the ion implantation and activation processes.

9:40am **MS-WeM5 Taking SOI and Low-k Dielectrics Into 130nm and 90nm High-Volume Microprocessor Production: Challenges, Processes, Extendibility**, ***R. Stephan***, *D. Greenlaw, G. Burbach, T. Feudel, F. Feustel, K. Frohberg, F. Graetsch, G. Grasshoff, C. Hartig, T. Heller, K. Hempel, M. Horstmann, P. Huebler, R. Kirsch, S. Kruegel, E. Langer, K. Romero, H. Ruelke, H. Schuehrer, A. Wei, T. Werner, K. Wieczorek,* Advanced Micro Devices, AMD Saxony LLC, Germany **INVITED**

SOI and Low-k technologies are mature at AMD and run in high-volume production. These technologies were developed for the fabrication of the 9-metal AMD OpteronTM and AthlonTM64 microprocessors.@footnote 1@ The 130nm version has been in production for 18 months, and the 90nm product shipments began several months ago. The paper highlights several challenges found when moving from development to high-volume production. SOI process modules have been developed to support a smooth conversion from 130nm to 90nm. Basic learning can be applied for the extension to the 65nm node. Examples of advanced SOI process modules such as STI, ultra-thin gate dielectrics, gate pattering, and the Cu interconnect using CVD-deposited low-k dielectric will be shown. The early implementation of SOI and low-k dielectrics into high-volume manufacturing will allow for the successful extension into the next process generations. @footnote 1@AMD, the AMD Arrow logo, AMD Athlon, AMD Opteron and combinations thereof are trademarks of Advanced Micro Devices, Inc.

10:20am **MS-WeM7 Beyond Planar Bulk CMOS: Manufacturing Issues in the 3rd Dimension**, ***C.R. Cleavelin***, Texas Instruments **INVITED**

The continuation of highly scaled Planar Bulk CMOS has been identified @footnote1@ as very difficult, if not impossible, at or beyond the 45nm Node due to short channel effects (SCE) and other parasitic effects. Several device structure options for "non-classical" CMOS have been proposed and fabricated in research environments, e.g., Ultra-Thin Body SOI (UTB-SOI) or Multiple-Gate FET (MuGFET) both using lightly doped bodies for scaling gate length Lg well below 20nm. Although these devices offer good device characteristics and scaling opportunities, fabrication and optimization of these devices for device level CMOS integration and production present inherently difficult challenges. This talk will identify and discuss many of these integration roadblocks and manufacturing challenges and discuss possible paths to overcome them. @FootnoteText@ @footnote 1@ International Technology Roadmap for Semiconductors 2003 Edition.

11:00am **MS-WeM9 The Nanotechnology Research Institute**, ***G. Bourianoff***, Intel Corp. **INVITED**

The Semiconductor Industry Association (SIA) has recently called for the creation of the Nanotechnology Research Institute (NRI) which will be dedicated to creating new ideas and demonstrating feasibility for novel electronic switching devices with associated memory and interconnects by the year 2020. The proposed institute will be a joint effort by industry, academia and government involving university faculty and students working with industrial assignees working in state of the art facilities located on or adjacent to university campuses. Funding would come from a partnership between government and industry. This paper will give the latest information on the research program and organizational structure of the NRI. In general, the NRI will address the scientific and engineering aspects of classical information processing at nanometer scale lengths, fempto second time scales and atto Joule energies. It will consider devices and architectures that rely on state variables other than electronic charge such as spin, phase, photons, dipole orientation, magnetic flux quanta, orbital symmetries and other non-stander state variables. It will consider novel architectures that rely on nearest neighbor data flows and novel data representations that may rely on associative data structures. It will seek to understand the relationship between information and entropy and many other advanced concepts that are vital to future scaling.

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