Manufacturing Science and Technology
Room Exhibit Hall B - Session MS-TuP

Poster Session

MS-TuP1 Reactive Preclean H@sub 2@/He Plasma Prior Copper Deposition, Investigation on the First Wafer Effect and Multivariable Advanced Process Control, ***R. Petri***, *L. Bucelle,* STMicroelectronics, France

As a general concern in the semiconductor industry, the process stability is crucial and the methodology to ensure this stability becomes more and more complex. By years, the submicron technology constrains the manufacturing to introduce thorough process controls: initially guaranteed by specification limits only, it was improved by the introduction of control limits and Statistical Process Control. Recently, the industry is moving to Advanced Process Control based on a multivariable control of machine parameters. By this way, those parameters can eventually be correlated with product yield. On another hand, process integration becomes extremely sensitive to the process environment and therefore any uncontrolled modification of the reactor surface, such as reactor wall state, wall temperature, in-situ plasma clean, could generate a process drift and may induce severe yield lost or reliability issues. As a consequence, the study and the eradication of the first wafer effect, due to its impact on the manufacturing performances, has generated a lot of focus and publications. This paper is an application of the Advanced Control Process to ensure the stability of the reactive H@sub 2@/He plasma preclean process used in dual damascene structure prior copper deposition. It shows that tiny variations of the wafer processing context are easily detected by appropriate APC model. It appears that plasma potential is very dependant on process controlled parameters but also varies significantly with substrat nature as well as reactor wall temperature. We show that any process drift from the standard expected behavior is detected with the developed model. The nature of the deviation (i.e. signature) is also given. Therefore, in a manufacturing environment, APC is an extremely versatile methodology which can detect in line process drift, but also allows more fundamental investigations, like first wafer effect understanding and eradication, much easier, faster and cost effective.

MS-TuP2 A New Way to Get Steady Trichlorosilane (TCS) Vapor Flow for EPI Deposition Process, *A. Sidhwa,* ***Z. Lu***, *S. Bansal,* STMicroelectronics, Inc*; C. Cross,* STMicroelectronics, Inc.

TCS has been used for many years as silicon source in high temperature EPI applications. It is still preferred in many applications since its low material cost and high deposition rate. In TCS EPI process, hydrogen (H2) is frequently used as carrier gas to convert TCS from liquid to vapor and carry TCS vapor to reaction chambers. The flow of TCS vapor is normally controlled by a Liquid Vapor Controller (LVC). It requires stable TCS liquid temperature to achieve good repeatability of TCS vapor flow. If both low and high TCS vapor flows are required, two LVCs have to be installed in parallel to achieve both low and high flow controls. A traditional LVC controls TCS vapor flow by measuring the mass difference between incoming gas (H2) and outgoing (H2+TCS) of the controller. It can provide steady TCS vapor flow if the temperature of TCS liquid is stable. Since TCS vapor pressure is extremely sensitive to TCS temperature, LVC can no longer provide steady TCS flows if TCS temperature fluctuates. The reason is that the temperature of outgoing gas (H2+TCS) and TCS partial pressure fluctuate according to the fluctuating TCS liquid temperature. In order to resolve the overhead/delay of TCS minibubbler/ conducting lines and their temperatures, a Piezocon flow controller was introduced and installed downstream of the TCS minibubbler. Since Piezocon controller calculates the accurate TCS flows in real time and its located downstream of the whole minibubbler unit, it becomes independent of the TCS liquid temperature. Piezocon controller also has high accuracy and repeatability in a wide range of vapor flows, which includes our low and high TCS applications. Once it combines with a digital MFC, which also has high repeatability in both low and high flow, the combination would provide us very steady TCS vapor flows in both low and high ranges.

MS-TuP3 The Evaluation of a Twin Wire Arc Spray (TWAS) Process for Coated Shields used in Soft-Sputter Etch Pre-Clean Chambers, ***A. Sidhwa,*** *M. Goulding, M. Kalaga, X. Breurec, R. Pierce, T. Gandy,* STMicroelectronics, Inc

A Soft Sputter Etch (SSE) process plays a vital role in the cleaning of contacts and vias prior to the deposition of contact barriers and via liners. This paper describes the work performed at STMicroelectronics to eliminate Silicon Oxide (SiO2) defects, which are observed at the end of the Pre-Clean chamber component (quartz and shield) lifetime; the latter is specified in RF hours. During the component re-cycling process, the aluminum (Al) RF shield receives a particular surface finish after the cleaning step. It is well known that the Bead-Blast/Post-Blast Etch (PBE) process produces a relatively rough surface finish, which enhances the oxide sticking properties during subsequent wafer sputter-etch. However during such processing, a large surface area of roughness (containing a small number of nucleation sites) is produced on the surface of the shield, resulting in defects (Silicon Oxide flakes) being observed at the end of the Pre-Clean chamber lifetime: i.e., the sputter-etched oxide becomes clustered around a comparatively small surface area, with continuous growth in a vertical direction producing "Worm" defects. The latter defects constitute "stress risers," which are a key source of oxide de-fragmentation. Hence, when trying to increase the sputter-etch chamber component lifetimes from the current 60 RF hours to a significantly higher value of 250 RF hours, the problem of Worm defects becomes more significant. However by contrast, an Al RF shield with a TWAS surface finish shows no similar issues at comparable lifetime. This paper describes the evaluation and implementation of TWAS for the Al RF shield, and explains the significant impact/elimination of Worm defects due to the change in the RF shield surface condition.

MS-TuP4 Two Gas Reactive Sputtering of Oxynitride Compounds: Model and Practice, ***D.C. Carter***, *D.J. Christie, W.D. Sproul,* Advanced Energy Industries, Inc.

Reactive sputtering process control has been the subject of much research in recent years. The result of this work has been the development of methods for improving the economy and utility of this popular deposition method. Adding to the understanding of reactive sputtering techniques are functional models developed to explain the dynamics of these often difficult to control processes. Most common, both in practical use and in laboratory research have been deposition processes involving a single reactive gas producing simple binary compounds. Only in the past few years have models been extended to consider the effects of a second reactive gas. Similarly, practical understanding from empirical studies involving two reactive gasses is quite limited. The general rule recognized from models and laboratory experience holds that for the deposition of most compounds effective control in the transition region between the metallic condition and the poisoned condition requires some form of active, partial pressure or similar control. Adding a second reactive gas to the process adds great complexity to the control challenge. Carlsson et al.@super 1@ demonstrated that a two reactive gas process can exhibit a behavior called "trapping" where the sputtering target becomes trapped in a poisoned state. Only through the removal of both reactive gases would the model allow the target to recover from the poisoned state. Based on this the partial pressure of both reactive gases must be controlled to prevent the trapping behavior. We apply such control to a two reactive gas sputtering process, first in deriving solutions to mathematical models and then in practice. Using active, multi-gas control we demonstrate stable two gas reactive sputtering for the oxynitride systems of Silicon, Titanium and Aluminum and within the stable operating space we show film composition control allowing user specified film properties and performance. @FootnoteText@ 1. J. Vac. Sci. Technol., A 11(4), (1993).

MS-TuP5 Hard Mask Dual Damascene Integration Scheme for 65nm, ***G.A. Delgadino***, *T.P. Pender, M. Le, S. Li, L.Q. Xia, Y. Ye,* Applied Materials, Inc.

Smaller geometries and the use of lower Îº dielectrics in BEOL integration at 65nm and beyond will require extensive changes in dual damascene integration scheme. Traditional via-first approach reaches its limits as 248nm photoresist is replaced by thinner, weaker, poisoning-prone 193nm photoresist. In this paper presents the development of a hard mask integration solution for extending the implementation of copper/low-Îº interconnect structures at 65nm node and beyond. The scheme overcomes major challenges in low-Îº integration, minimizing ashing damage to low-Îº material and avoiding photoresist poisoning issues associated with 193nm resist. Two Hard mask materials, TiN and W were investigated and potential problems addressed. For the etching point of view, both materials showed good performance but TiN required more tradeoffs due to its lower sputtering resistance and more chemically reactive nature. On the other hand, TiN transparency in part of the visible spectrum, facilitate integration while W required modifications during deposition and/or limitations on the mask thickness. Preliminary Low shear-force CMP with different slurries demonstrated good removal rates for both materials. From the perspective of feasibility and cost, hard mask Dual Damascene

appears to be a promising candidate for competitive Copper/Low k integration.

MS-TuP6 Integration of an Ultra Low-k Dielectric in a 300mm 130nm Trench First Dual Damascene Etch Process, ***R. McGowan***, *P.J. Wolf,* International Sematech*; D. Wang,* Tokyo Electron America, Inc.

This paper describes a two level metal, 130nm dual damascene etch process development, using an ultra low-k (ULK) dielectric material (k=2.2) on 300mm wafers. The process used a dual hardmask approach in a "Trench First" etch scheme with an interlayer etch stop. Each step requires good uniformity and selectivity to the underlying layers. A BARC etch DOE (used in all recipes) and correct selection of the hardmask & barrier etch chemistries were key factors in the successful etch development. Three iterations, in an overall cycle of improvement, are given as examples, used to take the process from an initial low yield to a robust high yielding process.

MS-TuP7 Effect of Double Polishing Pad on the Shallow Trench Isolation¬Chemical Mechanical Polishing (STI-CMP) Process, *Y.J. Seo,* ***S.W. Park***, DAEBUL University, South Korea*; W.S. Lee,* Chosun University, South Korea*; S.Y. Kim,* Dongbu-Anam Semiconductor Co. Inc., South Korea

Chemical mechanical polishing (CMP) technology for global planarization of multi-level inter-connection structure has been widely studied for the next generation devices. CMP process is carrying out by pressing a rotating wafer against a moving polishing pad on which suitable slurry is dispensed. Among the consumable for CMP process, especially, polishing pad set and itâ?Ts material properties play a very important role into the removal rates and global planarization ability of CMP process. In this paper, we investigated the effects of different sets of polishing pad to apply the direct shallow trench isolation (STI)-CMP process using high selectivity slurry (HSS). As our preliminary experimental results, IC1000/JR111 pad set and IC1000/subaIV pad set have the highest selectivity. Even if selectivity is high, because IC1000/SubaIV set shows the low removal rate, we could conclude that IC1000/JR111 set is more superior than IC1000/SubaIV set. Also, the wafer map of hard pad set showed the center-fast type, and soft pad set showed the edge-fast type. Through the above results, we could select the optimum polishing pad set to achieve the direct STI-CMP process without reverse moat etch step, so we could expect the improvements of throughput, yield and stability in the ULSI fabrication process.

MS-TuP8 Effects of Slurry Temperature on the Oxide-CMP Performance, *W.S. Lee,* ***T.W. Kim***, Chosun University, South Korea*; Y.J. Seo,* DAEBUL University, South Korea

The mechanical polishing pad and chemical slurry play an important role in chemical mechanical polishing (CMP) which has recently been recognized as the most effective method to achieve global planarization in ultra large scale integrated circuit multi-level interconnections. In this paper, we have investigated CMP performance of SiO2 as a function of different temperature of slurry and pad surface. There are two ways to study the temperature effect on CMP performance: (1) by controlling the temperature of both the pad and slurry at a desired value, or (2) by adjusting only the slurry temperature and keeping the polishing pad temperature. Moreover, the relationship between the removal rate (RR) and zeta-potential as a function of slurry temperature were investigated. According to the preliminary experimental results, it appears that the observed slurry temperature dependence of RR is mainly due to the change of pad surface mechanical property with the slurry temperature. Therefore, the understanding of these temperature effects provides a foundation to optimize an oxide CMP process for ULSI multi-level interconnection technology. This work was supported by a Korea Research Foundation grant (KRF-2002-005-D00011).

MS-TuP9 Impact of Reconditioned PVD Shielding on Process Yield, *D.J. Zuck,* ***G.H. Leggett***, *D.S. Zuck,* QuantumClean

Process control is impacted by many variables in the chamber of a semiconductor process tool. Process chambers often have shielding that is removable and can be reprocessed for reuse. The effective reprocessing of this shielding can have a dramatic impact on process performance. The process deposition must be removed completely and additional contaminates can not be added to the shielding. The shielding is in close proximity to the wafer surface and often can transfer contaminates to the wafer. This shielding can include clamp rings which can contact the wafer in the edge ring exclusion area. The surface condition of this shielding must be maintained. The typical cleaning methodology for the removal of metal deposits from stainless steel shielding is corrosive and can attack the underlying base metal. Changes in surface morphology and finish can result in shorter lifetimes for parts and also have an impact on process yield. Particle contamination can result from shielding that does not have the proper surface morphology and/or surface preparation. A methodology was developed to monitor the surface condition and recondition the part when this surface morphology has deteriorated to a point where it has an impact on process yield. A method was further developed that reconditioned the surfaces and improved the lifetime of these parts. Data will be presented on the mobile ionic contamination of the parts as well as the surface finish and its impact on process performance. A comparison of surface finish with process performance will be described.

MS-TuP10 Silicon Isotope Enrichment by IRMPD of Si@sub 2@F@sub 6@: A Method for High-Efficiency Enrichment of @super 28@Si by Two-Color CO@sub 2@ Laser Irradiation, ***H. Ohba***, *A. Yokoyama, M. Hashimoto, K. Katsumata, H. Akagi,* Japan Atomic Energy Research Institute, Japan*; S. Arai,* Hill Research Corporation, Japan

The natural abundance of silicon isotopes is 92.2% @super 28@Si, 4.7% @super 29@Si and 3.1% @super 30@Si. It has been reported that an isotopically pure @super 28@Si single crystal has a thermal conductivity about 60% higher than that of a natural silicon single crystal at room temperature. This pure material is expected to contribute to the creation of higher-density silicon integrated circuits. Laser isotope enrichment processes promise low energy inputs, low capital costs and lower tails assays, hence significant economic advantages. The infrared multiple photon dissociation (IRMPD) of Si@sub 2@F@sub 6@ leads to the formation of SiF@sub 4@ and SiF@sub 2@. The Si@sub 2@F@sub 6@ with enriched @super 28@Si can be obtained by dissociating the Si@sub 2@F@sub 6@ containing @super 29@Si and @super 30@Si selectively. In order to obtain highly enriched @super 28@Si products in the case of a conventional one-color CO@sub 2@ laser irradiation, however, a high fluence and a large number of laser shot are required, and it is unsuitable for large-scale separation. So, we have studied a rapid and highly efficient method for enrichment of silicon isotopes utilizing isotopically selective IRMPD of Si@sub 2@F@sub 6@ by a two-color laser irradiation scheme. We demonstrated that the dissociation rate of Si@sub 2@F@sub 6@ molecule per pulse increased about 10 times compared with the conventional one-color irradiation. And consequently we were able to acquire the highly enriched @super 28@Si at about one tenth of the laser shots required in the case of the conventional method.

MS-TuP11 Silicon Isotope Enrichment by IRMPD of Si@sub 2@F@sub 6@: Development of Continuous Silicon Isotope Enrichment Technique for Large-Scale Production, ***K. Katsumata***, *H. Ohba,* Japan Atomic Energy Research Institute, Japan*; H. Akagi, A. Yokoyama,* Japan Atomic Energy Research Institute*; S. Arai,* Hill Research Corporation, Japan

Since it had been reported that an isotopically pure @super 28@Si single crystal has high thermal conductivity, it has been growing interests in its use to the high thermal conductive semiconductor substrate. For the expansion of the market of the enriched silicon, it may be necessary to develop a large-scale silicon isotope enrichment method. We have demonstrated a highly efficient silicon isotope enrichment utilizing infrared multiphoton dissociation (IRMPD) of Si@sub 2@F@sub 6@ irradiated with two-color CO@sub 2@ laser@footnote 1@. The scheme consists of two successive steps: At first, the Si@sub 2@F@sub 6@ molecules containing @super 29@Si and @super 30@Si are excited selectively by the irradiation at nearly resonant wavelength with weak pulsed laser beam. Then, the excited molecules are dissociated by the irradiation at non-resonant wavelength with relatively high intense pulsed laser beam. In this report, we developed continuous silicon isotope enrichment technique for the large-scale production, based on this method. An apparatus for continuous isotope enrichment consists of two TEA-CO@sub 2@ lasers, a reaction cell with a gas flow system, and instruments for the monitoring of the abundance of Si in Si@sub 2@F@sub 6@ and the production rate. Si@sub 2@F@sub 6@ gas and buffer Ar gas flowed through a reaction cell with controlling pressure and flow rate. Then isotopically selective IRMPD of Si@sub 2@F@sub 6@ molecules containing @super 29@Si and @super 30@Si were done in the reaction cell by the simultaneous irradiation with two laser pulses at different wavelengths. All of the reaction products were corrected in a trap at 77 K. After the conditions for continuous isotope enrichment had been optimized, @super 28@Si enriched up to 99 % was produced at a rate of 0.7 g/h with the yield of 63 %. @FootnoteText@ @footnote 1@A. Yokoyama, et al., US patent 2003-0034243 A1 (2002).

MS-TuP12 Field Emission Enhanced Semiconductor Thermoelectric Cooler, ***B.L. Weiss***, *P.H. Cutler, N.M. Miskovsky,* The Pennsylvania State University*; M. Chung,* University of Ulsan, South Korea*; N. Kumar,* UHV Technologies

We report the initial experimental results of the fabrication and measurements of a prototype field emission enhanced thermoelectric cooler device. The device is designed for applications in microelectronics, and operating from ambient to cryogenic temperatures. The device is fabricated using CVD deposited wide band gap (diamond and III-V nitrides) thin films. Cooling measurements are carried out in a UHV system using both thermocouple and optical thermometry. This work is motivated by a recent theoretical analysis of an efficient, compact, low power consumption thermoelectric cooler by Chung et. al. @footnote 1@. The new paradigm involves cooling via electron field emission from wide band gap materials which is based on a corrected theory@footnote 2@ of the Nottingham effect @footnote 3@ with calculated cooling rates of up to 100 W/cm@super 2@ or better. The thermoelectric cooler device proposed here uses an electric field modulated current to transport energy (i.e., heat) from a cold source to a hot source via n- and p-type carriers. This device is fabricated by combining the standard n- and p-channel solid-state thermoelectric cooler with a two-element vacuum field emission device inserted into each of the two channels which introduces an essentially infinite thermal resistance for lattice heat conduction. In the proposed cooler, the heat removed from the cold source is the average energy difference of the field emitted electrons from the n-type and p-type semiconductors. The theory predicts the average energy removed (cooling rate) increases with decreasing doping concentration and with increasing local field at the emitter surface. With typical values of doping and field, the cooling rates exceed those of standard thermoelectric coolers. The cooling device is shown to have an energy transport (i.e., heat) per electron of up to 500 meV depending on concentration and field while, in good thermoelectric coolers, it is about 50-60 meV at room temperature.} $Footnotes {@footnote 1@ Moon Chung, P.H. Cutler, N.M. Miskovsky, Nalin Kumar and V. Patel,Solid-State Electronics, 47 1745-1751, 2003. @footnote 2@ Moon Chung, P.H. Cutler, N.M. Miskovsky and T.E. Sullivan,J Vac Sci Technol B;12(2),727-36, 1994. @footnote 3@ W.B. Nottingham Phys. Rev, 59, 907, 1941.

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