Manufacturing Science and Technology
Room 309 - Session MS-MoM

Process and Equipment Integration and Development
Moderator: E.G. Seebauer, University of Illinois at Urbana Champaign

8:40am **MS-MoM2 Development of Low Resistance Copper Thin Films Using a Strain Enhanced Grain Growth Technique**, ***M. Moriyama***, *M. Shimada, H. Masuda, M. Murakami,* Kyoto University, Japan

Copper is attractive as interconnect materials of future Si-ULSI (Ultra-Large Scale Integrated) devices with linewidth of less than 100nm. The advantage of using copper (over conventional Al-alloy) as the interconnect materials is that copper has lower electrical resistivity and higher reliability. However, we have serious concern with resistivity of the ultra-narrow Cu interconnects, because the resistivity of interconnects was observed to increase rapidly by reducing the linewidth of the interconnects. The reason is believed to be due to the relatively long mean free path (~39nm) of the conducting electrons of copper. When the linewidth is less than 100nm, the electron scattering by the surface (or interface) and grain boundary becomes dominant, causing significant increase in the resistivity of the copper interconnects. In order to realize nano-scaled Si-devices, development of low resistance ultra-narrow copper interconnects is essential. The purpose of the present experiment was to explore the possibility to prepare low resistivity copper interconnects, which satisfy the designer's requirement, by determine the primary factor (film thickness or mean grain size) which controls the electrical resistivities of copper films. The film microstructures were observed by atomic force microscopy and scanning ion microscopy. The film resistance was measured by a DC four-point probe method. Our experimental result concluded that the grain boundary scattering primarily increased the resistivity of the Cu thin films, indicating that large grained films were essential for low resistivity ultra-narrow copper interconnects. We succeeded to prepare the copper thin films with giant grains by the strain enhanced grain growth technique. This technique will be promising to develop the low resistance copper interconnects for the future Si-ULSI devices.

9:00am **MS-MoM3 Processing and Characterization of PMSSQ Based Materials for Nanoporous Low-K Dielectrics**, ***P. Lazzeri,*** ITC-IRST, Italy*; J.J. Park, Z. Lin, R.M. Briber,* University of Maryland*; L. Vanzetti, M. Anderle, M. Bersani,* ITC-IRST, Italy*; R.D. Miller,* IBM Almaden Research Center*; G.W. Rubloff,* University of Maryland

Nanoporous low-K dielectrics are an essential component in future interconnect technology. We have investigated the thermal transformations by which nanoporous polymethylsilsesquioxane (PMSSQ)-based low-K dielectrics are formed through spin-casting and curing in a mixture of PMSSQ with a poly(methylmethacrylate-co-dimethylaminoethylmethacrylate) random copolymer (PMMA-co-DMAEMA) as the porogen. ToF-SIMS shows a sequence of PMSSQ fragments which change with curing, as well as the evolution of porogen related species. Over the range 200-450C, both crosslinking to form the SiO@sub 1.5@CH@sub 3@ matrix and decomposition/volatilization of the porogen occur. To understand the influence of PMSSQ precursor chemistry on the final low-K structure, we have compared two precursors with different initial SiOH content. ToF-SIMS shows the crosslinking kinetics to be faster for the high SiOH than for the low SiOH content material. The distribution of the porogen species also varies with the nature of the PMSSQ precursor: XPS reveals substantial surface depletion of porogen for the low SiOH but not for the high SiOH content material, and ToF-SIMS images indicate the formation of large porogen aggregates, but only for the low SiOH material. Thermal desorption mass spectrometry during curing shows the evolution of volatile byproducts, as expected for both the crosslinking reactions and the porogen degradation and desorption. These chemical analysis techniques yield information crucial to understanding the complex chemical and transport phenomena which determine the microscale and nanoscale properties of these nanoporous low-K dielectrics and their role in future interconnect technology.

9:20am **MS-MoM4 Multi-scale Modeling of Chemical Mechanical Planarization**, *L. Jiang, H. Simka, S. Skokov, D. Thakurta,* ***S. Shankar,*** Intel Corp.

A coherent modeling approach is presented for mechanics and transport effects in CMP process. Different regimes of material removal are identified based on first-principle analysis on slurry transport, stress, and slurry flow. Important effects of pad, glazing, conditioning, and polisher design are demonstrated with oxide polish model results. We review multiple-scale model linking with an emphasis on the innovative methods to combine flow and stress analysis from feature to wafer scale. Micron-scale models developed at Intel are presented to illustrate the complexity of particle-level dynamics in CMP and the physical processes involved in patterned wafer planarization.

9:40am **MS-MoM5 Thermal Characterization of Stacked 3D System-in-Package**, *J. Valtanen, J. Miettinen,* ***E.O. Ristolainen,*** Tampere University of Technology, Finland

Electronics development has been driven mainly by IC technology progress. Cell and line width have been continuously shrunk proving development trend called Moore's law. This has created increasing pressure to the first level interconnection. In future, traditional 2-dimensional (2D) packaging will limit product miniaturization. Therefore, components must be also joined to third dimension. A solution to this problem is a stacked System-in-Package (SiP). With this technology, great improvements over 2D packaging are achieved, such as greater packaging density, smaller size, and shorter interconnection length. The next evolution step comes in through following ways: to grind extra sand away from active ICs, to use flexible substrates and interposers. However, this technology has some problems that must be solved. For higher density of 3D package, increased power density brings new challenges to heat management. In this work, a stacked SiP structure has been studied. The package consists of three layers. In every layer, a silicon die of 3.7 mm x 8.3 mm has been joined with flip chip method onto an aramid-epoxy interposer of 6 mm x 10 mm. The silicon chips has been thinned down to 90 µm and the thickness of the interposer is 150 µm. The interposers are joined together using solder covered polymer spheres with diameter of 250 µm. So, the dimensions of whole package are 0.9 mm x 6 mm x 10 mm resulting in the total silicon efficiency of 150 %. Transient thermal responses have been measured by experiments and they are compared with simulations calculated with the FEM program Ansys. A constant heat power has been added to one chip at a time and temperature response has been measured in every chip. In this study, thermal responses, maximum temperatures, and chip-to-chip thermal interactions are achieved. In addition, differences between boundary conditions are discussed and certain design rules for chip placement are given.

10:00am **MS-MoM6 Advanced Clean Process by Supercritical Carbon Dioxide**, ***H.-J. Tu,*** *P. Chuang, C.-Y. Wang, Y.-L. Lin, H. Lo, M.-S. Zhou, M.-S. Liang,* Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan, R.O.C.

As device approaching nano-scale, it is more difficult to extend aqueous-based clean processes to future generations due to its high surface tension characteristics. An advanced clean process by supercritical carbon dioxide (SCCO@sub 2@) becomes a potential enabling technology in semiconductor industries for its specific capabilities of low surface tension, chemical inertness, and more friendly ESH (environment, safety, and health) which can overcome future wafer clean challenges. In the present work, we show that using SCCO@sub 2@ can successfully remove residue/polymer for advanced sub 100 nano-meter copper low-k interconnect fabrication. In addition, it appears that the low-k dielectric film is much less damaged by this novel technology than conventional clean process.

10:20am **MS-MoM7 Two-Gas Reactive Sputtering**, *W.D. Sproul, D.J. Christie,* ***D.C. Carter,*** Advanced Energy Industries, Inc.

Reactive sputtering with two reactive gases and one target material presents special problems. Both reactive gases affect the state of the target surface and the plasma conditions, which means that both affect common feedback control signals such as the cathode voltage and optical emission signals. Modeling has shown that the way to control the two-gas reactive sputtering process is to produce individual control signals for each gas. Experiments have confirmed the model. The reactive sputtering of titanium or silicon in a combined oxygen/nitrogen atmosphere is shown. In this study, individual partial pressure signals for each of the oxygen and nitrogen reactive gases were available from a mass spectrometer. A combination where one of the gases is controlled in the partial pressure mode and the other in a flow mode can lead to unstable operating conditions under certain process conditions. The gas operating in flow control can trap the target in a poisoned state, and the target cannot return to the unpoisoned state until both gases are removed. Both target voltage and mass spectrometer data show the existence of a high partial pressure of the flow controlled reactive gas that traps the target in the poisoned mode even when the partial pressure controlled reactive gas is removed from the system. To have a fully stable process when two reactive

gases are used requires that the partial pressure of each gas be controlled individually. When the individual partial pressures are controlled, the target does not get trapped in a poisoned state, and there is complete freedom to adjust the reactive gas partial pressures to achieve the desired film composition.

10:40am **MS-MoM8 Hydrogen Pressure Dependence of Trench Corner Rounding during Hydrogen Annealing**, ***H. Kuribayashi***, *R. Shimizu,* Fuji Electric Corporate Research and Development, Ltd., Japan*; K. Sudoh, H. Iwasaki,* Osaka University, Japan

Hydrogen annealing has become increasingly important for silicon device processes. Especially for trench gate MOSFETs, both trench corner rounding and sidewall surface smoothing are quite essential for the ruggedness and reliability of gate oxide. Though the evolution of crystal shape through surface self-diffusion during heating in vacuum has been extensively investigated, it has not been sufficiently studied in specific ambients, which are applicable to semiconductor processes. At the preceding meeting we studied shape transformation of silicon trenches with sidewall surface of (110) and (-110) during annealing in hydrogen ambient at 1000°C, and showed that the observed shape transformation can be simulated well with Mullin's continuum surface model@footnote 1@ with surface self-diffusion. In this work, to study the roll of hydrogen gas on the Si surface self-diffusion in more detail, we investigated both the hydrogen pressure dependence and the temperature dependence of the trench corner rounding for wider range of pressure (10-760Torr) and temperature (1000-1100°C), respectively. We found a remarkable effect of hydrogen on trench corner rounding. The curvature of a trench corner for a certain annealing time increases linearly with increasing hydrogen pressure. The diffusion coefficient at 1000°C deduced by the Mullin's formula decreased from 2x10@super 5@nm@super 2@/sec at 100Torr to 3x10@super 3@nm@super 2@/sec at 500Torr, which are much smaller than the one in vacuum@footnote 2@ by three to five orders of magnitude. The diffusion coefficients did not follow the Arrhenius relations for 1000-1100°C in the higher-pressure region above 100Torr, suggesting that more than one rate-limiting processes are involved in the temperature range. @FootnoteText@ @footnote 1@W.W.Mullins, J.Appl.Phys.28, 333(1957).@footnote 2@Y.-N. Yang, Elain S. Fu, and Ellen D. Williams, Surf. Sci. 356,101(1996) .

11:00am **MS-MoM9 Development of a Continuous Generation/Supply System of Highly-concentrated Ozone Gas for Low-temperature Oxidation Process**, ***S. Ichimura***, *H. Nonaka,* National Institute of Advanced Industrial Science and Technology (AIST), Japan*; Y. Morikawa, T. Noyori, T. Nishiguchi, M. Kekura,* Meidensha Corporation, Japan

Ozone has various superior characteristics compared to oxygen molecules in ultrathin oxide film formation on silicon. It realizes rapid oxidation rate at low substrate temperature, very thin transition layer in the oxide film, high electrical quality of the oxide film, etc. Those characteristics have been proved using a highly concentrated (HC) ozone generator, which supplies almost 100% ozone gas at pressure lower than 1000 Pa. The generator utilizes vaporization of pure liquid ozone accumulated in an ozone vessel. Since the liquid ozone accumulation is limited to 5 ml because of safety, the generator can supply only about 360 l ozone gas at the pressure. Considering future need in practical low-temperature oxidation process, we have developed a new system which continuously generate/supply HC ozone gas. The system is equipped with 4 ozone-vessels, and each vessel temperature can be controlled separately. During continuous operation, the condition of each ozone vessel changes stepwise with the same time interval along the following mode sequence; 1) cooling the vessel from 120K to 90K, 2) accumulation of liquid ozone by distillation of ozone/oxygen mixture gas at 90K, 3) heating the vessel from 90K to 113K and vaporization of pure liquid ozone, and 4) heating the vessel from 113K to 120 K and evacuation of the vessel. Allocating one of the 4 modes to each of the 4 ozone vessels so as to cover all the modes simultaneously, the system can supply constant flow of HC ozone gas. The maximum flow rate of the gas is 60 sccm, being enough for single wafer processing, and the ozone concentration is over 99 vol.% at the output of the system. The characteristics of the system in the formation of ultrathin oxide on 4 inch silicon wafer is examined, together with the effect in low temperature oxidation of excited state atomic oxygen which can be generated/supplied by photo-dissociation of ozone at sample position. @FootnoteText@@footnote 1@T. Nishiguchi et al. Appl. Phys. Lett. 81, 2190 (2002).

11:20am **MS-MoM10 Profile Control for Deep Silicon Etch by Sidewall Passivation in High Density Plasma**, ***M. Khbeis***, *G. Metze,* Laboratory for Physical Sciences*; K. Powell, D. Thomas, A. Pentland, J. Hutchings,* Trikon Technologies, Ltd.

Deep silicon etching of micron-sized structures is a critical step in high-aspect ratio via fabrication. This paper shows that m=0 Resonant Induction (M0RI) plasma technology coupled with the use of both etch and passivation gases produced deep via holes with unscalloped sidewalls at non-cryogenic temperatures. Process development, operational parameters, and potential applications are discussed. Wafer level packaging of high density, complex systems-on-chip is of great interest to the microelectronics industry for the production of compact devices and electronic components.@footnote 1@ Vertical integration of various unpackaged integrated circuits can be accomplished through die attachment, wafer-to-wafer bonding, thinning, and lastly high-aspect ratio backside interconnects for signal communication. During the fabrication of these 3-D systems there is a need to provide high-aspect ratio backside metal interconnects at a depth of at least 20µm. The fabrication of interconnect via holes dictate that the following etches be performed; oxide mask etch, bulk silicon etch, and buried oxide layer etch. Other potential applications for deep silicon etch include bulk micromachining for MEMS, ground/power plane connections, or re-routing of signal lines for novel packaging. In this paper, development of the deep bulk silicon etch is emphasized. To accommodate subsequent dielectric passivation and metallization steps, via holes were specified to have a profile angle of 89 to 90 degrees with absolutely no sidewall scalloping. Sidewall scalloping will impede metal transport during a high-pressure reflow process. Since deep reactive ion etch (DRIE) processes, such as Bosch, induce scalloping, alternative etch technologies that do not require switching of etchants and passivants are mandatory. @FootnoteText@@footnote 1@ J. Reche E. Korczynski, High-Density Thru-Silicon Interconnects, HDI Expo Proceedings,(2000).

11:40am **MS-MoM11 The Study on Deformation of ArF Photo Resist in Dry Etching**, ***C.-H. Shin***, *G.J. Min, C.J. Kang, J.T. Moon,* Samsung Electronics Co., Ltd., Korea

193nm ArF lithography has been introduced in DRAM industry for sub-90nm patterning. However, it has several issues in the substrate fabrication of sub-90nm patterning. First, the physical thickness of resist has been decreased less than 3000Å, which is critical point for stable pattern transfer. Second, durability of resist in the plasma was reduced due to the increase of Ohnish parameter. Third, resist is subjected to deformation when it is exposed to the plasma due to its soft chemical structure. All these factors limit the application of ArF lithography. Etching was performed in the commercially available dual frequency plasma based on O2, Ar, CO and C4F6 single gas chemistry, respectively. It was found that supply of bias power in the argon gas system led to the severe deformation of ArF photo resist. Novel techniques for the formation of protective layer will be discussed in this paper in order to suppress resist deformation with enhanced etch selectivity.

Manufacturing Science and Technology
Room 309 - Session MS-MoA

Challenges in Advanced Materials and New Processes for Semiconductor Manufacturing

Moderator: A. Testoni, Varian Semiconductor Equipment Associates

2:00pm **MS-MoA1 Research and Challenges in Nano Mechanics and Materials**, ***K.P. Chong,*** National Science Foundation **INVITED**

Mechanics at the nano-scale is quite different from continuum mechanics. Nanomechanics is basic and essential in all areas of nano science, materials and engineering. Basic principles and experimental tools, multi-scale simulation, self-assembly as well as nanomechanics in information technology, biotechnology, micro/nano electronics [M/NEM] and other issues are presented. Recent workshops, research issues, research projects, as well as opportunities and challenges in nanomechanics are also discussed.

2:40pm **MS-MoA3 Opportunities and Challenges in the Materials Supply Chain for Semiconductor Manufacturing**, ***R.J. Richardson,*** Air Products and Chemicals, Inc. **INVITED**

Over 100 gases and chemicals are used to manufacture semiconductor devices. Many of these materials present formidable challenges in synthesis, purification, analysis, container and distribution system compatibility, contamination control, ESH and regulatory issues. As we near the end of the CMOS roadmap, a large number of new materials and processes are being considered to enable the manufacture of ever-smaller device structures. Although the large number of new candidate materials appears to provide a number of new opportunities, they bring a host of challenges. Only a few of the new alternatives will eventually end up in high volume manufacturing, which poses a dilemma for a full service materials supplier beyond the decisions related to the allocation of scarce R&D resources to multiple solutions to the same problem. How these issues (e.g., purity requirements, materials compatibility studies, ESH impacts) are addressed for some of the new materials under consideration for advanced CMOS manufacturing and the various competing trends (e.g., consistency of supply vs. ever-higher purity) facing the materials supplier will be discussed.

3:20pm **MS-MoA5 New Processes and Materials for Environmentally Benign Semiconductor Manufacturing**, ***F. Shadman,*** University of Arizona **INVITED**

The environmental issues are beginning to have significant impact on both the development of new processes and the application of new materials. In this presentation, some of the technical challenges and the potential solutions will be discussed. The specific examples will include: surface preparation, new dielectric materials, gaseous emissions particularly of global warming compounds, environmental bottlenecks in chemical mechanical planarization (CMP), and finally, environmental drivers for process integration in patterning and deposition of dielectrics in copper/low-k dielectric systems.

4:00pm **MS-MoA7 Sub-100 nm Copper Wiring Challenges and Solutions**, *M. Xi, M. Yang, W.-F. Yau, J. Dukovic,* ***A. Rosenfeld,*** *N. Maity,* Applied Materials **INVITED**

With the emergence of sub-100 nm Cu-low k BEOL technology, copper-electroplating faces a new set of challenges. The combination of shrinking dimensions (coupled with an increase in aspect ratio) and increased current density, necessitate innovation in process and hardware development that can provide acceptable process integration results. Furthermore, the ever-shortened development cycle requires proliferation of new innovations into predictable and repeatable production-worthy processes in minimal development and qualification cycle time. The Cu metallization process is performed in two steps. First, thin metallic layers of barrier material (such as TaN or Ta) and Cu seed is deposited into the vias and lines that define the interconnect. Next, Cu electroplating is used to fill the interconnect structures. The function of the barrier material is to prevent Cu diffusion into the surrounding dielectric, while the Cu seed enables the electroplating fill. The key requirement for both barrier & seed layers is conformal step coverage in sub 100nm features. As such, ionized PVD technology is required to achieve the desired step coverage. To address this requirement, a novel magnetron source was developed that enables high metal ionization with a flat target. The flat target design enables low defects and low cost of ownership for the Cu Barrier-Seed process. Moving to 65 nm and below, the PVD films could be substituted by ultra-thin conformal ALD films, particularly for the barrier process. This will enable lower interconnect resistance and further reduce cost of manufacturing, by reducing the cost of consumables for both the barrier deposition and the barrier CMP processes. To address the needs of sub 100nm copper plating, a novel electroplating system featuring a small volume plating bath with individual electrolyte circulation is was developed. Conventional large volume electroplating bath systems is are adequate for 130nm productions needs, but shows limitations in the area of consistent gap fill and defect performance for sub 100nm applications. In addition, a large bath system lacks the flexibility to change chemistry quickly, which slow down the development and optimization of new processes to meet the new requirements. Root cause of the inconsistent gap fill is correlated to organic by-product build up. In one experiment, the total organic content of a large bath system is measured throughout the life of the bath. The result shows that gap fill consistency is compromised when the total organic content is above 550ppm. In contrast, the small volume plating system allows periodic dumping and refilling of the plating bath after processing a small number of wafers, such as 200 wafers. This provides two key advantages. First, incoming wafers are exposed to fresh plating solution. This minimizes the gap fill inconsistency caused by aging and breakdown of the organic additives mentioned above. Second, by dumping and refilling the small bath after a small number of wafers are processed, different chemistry can be introduced and tested efficiently, from one bath to the next. This can provide significant time and chemical savings for process development and optimization. In addition, the individual electrolyte circulation design allows different plating cells within a plating system to process with different chemistries. This design enables sequential processing, or multi-step plating within a single plating system. The advantage of multi-step plating is demonstrated with experimental results showing dramatic reduction in as plated mounding.

4:40pm **MS-MoA9 Nanoporous Organosilicates for On-Chip Applications Using Sacrificial Macromolecular Porogens**, ***R.D. Miller,*** *W. Volksen, H.-C. Kim, E. Connor, J.L. Hedrick, C.J. Hawker, T. Magbitang, V. Lee,* IBM Almaden Research Center **INVITED**

Porous organosilicates have many potential applications, including separation media, catalyst supports, high surface area materials for bio-applications and ultralow-k media for on-chip insulator applications. The latter is driven by the need for low-k insulators to minimize signal delays and crosstalk. We have studied the generation of nanoporous thin film organosilicates using sacrificial macromolecular porogens, a process that requires a tailored interaction between the pore generators and the respective matrix resin. Depending on the porogen structure, the pore generating process can be classified either as nucleation and growth or templating. Each technique produces porous materials, but the film morphologies can be quite process specific. The integration of porous organosilicates for copper interconnects puts a premium on matrix mechanical properties. These can be altered by structural variations and/or process variations. The generation, characterization and integration of porous thin organosilicate films will be discussed.

Manufacturing Science and Technology
Room 309 - Session MS-TuM

Packaging and Role of Interface Engineering in IC Processing

Moderator: L. Larson, SEMATECH

8:20am **MS-TuM1 Challenges and Advances in Packaging Technology Development for IC Processing**, ***H. Hosack,*** Semiconductor Research Corporation **INVITED**

Traditionally packaging provides isolation of the chip from the environment and a space transformation from the chip bond pads to leads compatible with connections to the outside world. With the recent increases in frequency and power dissipation in high performance microprocessors, and the advent of portable electronics, the requirements for electronic packaging are rapidly expanding not only to continuing increases in performance, but also to radically different functionality in areas such as photonics, RF, and MEMS. These new needs require complete re-thinking of packaging with the view that the die-package is a sub-system in itself, and the need is to produce this complete sub-system with optimized total performance at a minimum cost. The areas of critical importance in this sub-system view will be those areas that address the interface between the die back-end and the package. By eliminating unduly specialized work on either the chip or package in isolation, redundant effort can be minimized and device performance can be optimized. The challenges inherent in optimizing the chip-package interface include the spectrum of electrical issues, thermo-mechanical issues, and metrology. These issues are being addressed by package-chip interface solutions that not only optimize the sub-system in its present configuration but also by novel schemes that employ new materials, new signaling mediums, and reallocation of interface functions between the package and the chip. These new approaches include novel schemes such as incorporating portions of the traditionally on-chip metallization as a part of the package, non-contact chip-to-package signaling, and 3D packaging. This discussion describes the critical issues that must be addressed in this new view of package functions, as well as the status of some of the unique solutions that are being researched to provide the optimized chip-package sub-system.

9:00am **MS-TuM3 Interfacial Engineering for Reliability Improvement of Cu/Low k Interconnects**, ***P.S. Ho,*** University of Texas **INVITED**

With continuing device scaling, interfaces of dielectrics, metals and semiconductors become increasingly important in controlling the yield and reliability of devices and interconnects. Beyond the current 130 nm technology node, the implementation of low k dielectrics causes serious reliability concerns for Cu interconnects due to their weak thermomechanical properties. This paper will first discuss the role of interfaces in controlling the reliability of the Cu damascene structure, particularly regarding electromigration and stress voiding. Several approaches of interfacial engineering to improve Cu interconnect reliability will be discussed, including surface processing and overcoat layers to reduce mass transport and to increase adhesion strength. Central to these approaches is the optimization of the chemical bonding to improve the properties of interfaces and low k dielectrics. The effects on electromigration and stress voiding of Cu/low k interconnects will be discussed.

9:40am **MS-TuM5 Forming Laminar Cu/Substrate Interfaces: Vacuum vs. Electrochemical Processing**, *N.P. Magtoto, J. Liu, J. Lei, X. Zhao,* ***J.A. Kelber,*** University of North Texas **INVITED**

The nucleation and conformal growth of a Cu film on a metal or dielectric barrier substrate is of critical importance for the production of reliable interconnects. This phenomenon has been studied extensively at the vapor/solid interface, where surface science experiments carried out in vacuum or ultrahigh vacuum (UHV) can generally be applied directly to industrial thin film fabrication methods (e.g., sputter deposition). Such studies have demonstrated that the initial growth mode of Cu on various substrates is extremely sensitive to surface chemistry, and this can lead to highly variable results during real world processing. In many cases, including Si:C:H films,@footnote1@ silane-treated Ta,@footnote2@ and sapphire(0001),@footnote3@ initial 2-D growth on a dielectric or air-exposed metal substrate is enhanced by substrate hydroxylation prior to Cu deposition. This has important consequences for designing processes that are insensitive to incidental oxidation. In contrast, the situation at the electrolyte/solid interface is complex, and fundamental issues like the role of ad-atom mobilities or surfactants in film nucleation are not well understood. Kinetic measurements and in-situ STM provide only limited information.. This talk will review the enhancement of Cu 2-D growth at the vapor/solid interface, and discuss recent efforts to identify conformal vs. 3-D growth during electrodeposition, including the prospects for using monolayer concentrations of ad-atoms, such as iodine, to enhance conformal growth in additive-free environments. @FootnoteText@ @footnote1@. M. Pritchett, N. Magtoto, and J. Kelber, Thin Solid Films (in press) @footnote2@. X. Zhao, M. Leavy, N. P. Magtoto and J. A. Kelber , Thin Solid Films 415, 308 (2002) @footnote3@. C. Niu, K. Shepherd, D. Martini, J. Tong and J. A. Kelber, and D. R. Jennison and A. Bogicevic, Surface Science 465, 163 (2000).

10:20am **MS-TuM7 Challenges and Advances in Thin Film Mechanics**, ***Z. Suo,*** Princeton University **INVITED**

Devices in modern technologies have complex architectures, small feature sizes, and diverse materials. The close proximity of dissimilar materials leads to unusual fracture behaviors. A scientific understanding of these behaviors is significant for the development of the future technology. In particular, rate processes, such as creep, subscritical cracking, and ratcheting, limit the long term reliability of the interconnects. Drawing on recent experiments and models, this talk describes a channel crack in a brittle film on an underlayer. When the underlayer is compliant (e.g., a low k dielectric), the driving force on the channel crack is very large. When the underlayer creeps (e.g., a polymer), the crack velocity is set by the viscosity in the underlayer, as well as by subcritical cracking in the brittle film. When the underlayer is plastically deformable (e.g., a metal), on thermal cycling, the crack can grow in the brittle film by ratcheting deformation in the underlayer. I also discuss the use of these phenomena to measure mechanical properties at the small scale. PDF files of papers are available at http://www.princeton.edu/~suo/ Keywords: Interconnects, fracture, creep, plasticity.

Manufacturing Science and Technology
Room 309 - Session MS-TuA

Directions in Semiconductor Device Scaling for the Next Decade

Moderator: S. Shankar, Intel Corporation

2:00pm **MS-TuA1 The Future of Chip Making Is Different --- Or Is It?**, ***R. Puhakka,*** VLSI Research **INVITED**

During this downturn chip making industry has seen numerous arguments that Moore's Law has to slow down and no one can afford to continue as before. The fab cost is over $3B for leading edge fab, steppers are forecasted to cost more than $30M each, and new materials like copper, Low-K and High-K are creating new failure modes that are not well understood. In essence, the future of chip making is different. Or is it? Data shows that cost per transistor still continues to drop at historical rates. The number of transistors manufactured continues to grow fast, which shows world's appetite for technology. Simultaneously, chip industry continues to shrink the critical dimensions at a very regular rate of node per two years. All of this is more difficult and expensive. This means it's becoming more of a big company game - - a long term trend that's been in place since the eighties. The analysis, however, also shows evidence that long term growth for chips and equipment is fundamentally lower. The future is different, but not as dramatically as has been argued.

2:40pm **MS-TuA3 Technology and Manufacturing Challenges in High Tech**, *R.L. Wisnieff,* IBM Corporation; ***S.M. Rossnagel,*** IBM T.J. Watson Research Center **INVITED**

Semiconductor technology is currently going through a fundamental transition, for the last forty years the active device has been the primary limitation in circuit performance, however today the wiring that interconnects the active devices is rapidly becoming the largest factor in determining the maximum speed the circuit will operate at. The search for high performance interconnects led to the widespread adoption of copper wiring to lower the resistance and, more recently, to the introduction of low dielectric constant materials to lower the capacitance of the interconnect circuit. The research and development of copper wiring spanned a period of roughly 12 years with much of this time was spent in refining the technology to achieve high reliability and yield. The research and development of lower dielectric constant materials is being undertaken at a much faster pace over a period of 5 years materials have been developed and applied to product. This accelerated schedule has left substantial room for improvement in the materials and processes that are being used. It is likely that there will be a series of incremental improvements ultimately culminating in a wiring technology that will use air gaps.

3:20pm **MS-TuA5 The Future of Semiconductor Lithography**, ***W.J. Trybula,*** International SEMATECH **INVITED**

The technology acceleration of the semiconductor industry has placed tremendous pressures on both equipment suppliers and manufacturers. Reviewing the International Technology Roadmap for Semiconductors (ITRS) readily demonstrates this advance in technology through acceleration. By examining the market pressures, an understanding of the forces driving the semiconductor manufacturers can be obtained. The result of these pressures is demonstrated by the Lithographic exposure tools that are currently under development. 193nm tools are being introduced into widespread manufacturing. 157nm lithography is being developed for introduction in late 2005 or early 2006 with production insertion slated for 2007. Extreme UltraViolet (EUV) is also under development for with plans manufacturing insertion in 2009. In addition, Electron Projection Lithography (EPL), Maskless Lithography (MML), and nano-Imprint Lithography are all being pursued. This paper provides an overview of the technologies being developed. Details of each are provided, which encompass the methods of operation, the key drivers for each technology, the mask requirements, the advantages of the technology, and projected insertion timing based on the exposure tool manufacturers' estimates. A summary will be provided that shows the time scale of each of the technologies for insertion. The key challenges for the technologies will highlight the areas of prime consideration. A final table will be provided that estimates the total industry cost to develop the technologies that are under primary consideration for insertion in the next few years.

4:00pm **MS-TuA7 CMOS Scaling Limits and Opportunity for Nanoelectronics**, ***Y. Nishi,*** Stanford University **INVITED**

Moore's Law and the scaling principle have guided IC technology and products development in the past 3.5 decades, which has led us to sub 100nm era today. At the end of each decade IC technology community anticipated some sort of slowing down in the pace of geometry shrink, i.e.; in late 70's it was 1um as the limit of practical scaling, and in late 80's it became 0.1um as the ultimate limit. Now we are discussing 10-20nm as the ultimate limit. In the past cases, a set of technology break through allowed us further scaling, such as stepper technology and later excimer laser technology coupled with rapid thermal processing. At the same time we did not have physics driven limits in small geometry devices in the past, but now it seems there will be fundamental changes in transport phenomena in MOS transistors as geometry shrinks. The question today should be, "Do we have another break through which may bring us to sub-20nm in terms of performance, power consumption, cost and manufacturability?" If the answer is "no", we need to look into other options to partially, if not fully, replace scaled CMOS approach. This talk will cover the trends of CMOS scaling in the past, today and tomorrow, and discuss technical bottle neck and challenges mainly from device physics and technology point of view, followed by looking into several opportunities of nanoelectronic devices such as nanowires, nanotubes from device physics integration point of view.

4:40pm **MS-TuA9 John Bardeen and Transistor Physics**, ***H.R. Huff,*** International SEMATECH **INVITED**

The point contact transistor and the discovery of transistor action by Bardeen and Brattain on Dec 16, 1947,@footnote 1,2@ which evolved from studies on Shockley's field-effect principle, was the first solid-state electronic device to utilize both free-electrons and free-holes and resulted in Bardeen and Brattain receiving a patent on Oct 3, 1950.@footnote 3@ Shockley was not a co-patent holder, however, since his scientific contribution of the field-effect principle had, in retrospect, already been anticipated through a previous patent awarded to Lilienfeld in 1930.@footnote 4@ The assessment as to whether the minority-carrier holes emitted into the large grained polycrystalline, n-type Ge (or Si) sample were mainly transported from the emitter to the collector through the p-type inversion layer@footnote 5@ or exhibited some non-trivial transport as minority-carriers through the n-type bulk sample, continues to be of interest and will be discussed. In that regard, Shive's experiment clearly illustrated the importance of the geometrical configuration in determining the percent of surface versus bulk transport@footnote 6@ while Shockley's p-n (bulk) junction theory and p-n junction transistor, originally an undisclosed notebook account, facilitated the mathematical description of Bardeen and Brattain's previously disclosed transistor action@footnote 1-3@ using a one-dimensional analysis.@footnote 7@ Bardeen also comprehended that it was not efficient to modulate the conductivity of a slab of semiconductor via the field effect@footnote 8@ and, thereby, patented the essence of the first modern (MOS) transistor.@footnote 9@ This was an insulating gate modulating an n-type inversion layer via the field effect, utilizing the inversion layer to confine the minority-carrier transport, in series with a reverse-biased n-p junction, and resulted in the first recorded power gain in a solid-state amplifier.@footnote 9@ The device, described by Sah as a sourceless MOS transistor,@footnote 10@ became the basis of, for example, subsequent MOS memory DRAM and CMOS microprocessor applications. Indeed, John Bardeen, the co-inventor of the bipolar and inventor of the MOS transistor, may rightly be called the father of modern electronics. Nevertheless, Shockley deservedly shared the Noble prize in 1956 with Bardeen and Brattain for his seminal contributions of injection over a barrier, p-n (bulk) junction theory and p-n junction transistor. The scientific background, personnel involved and intertwining of these historic 1940s events are described. @FootnoteText@@footnote 1@J. Bardeen and W.H. Brattain, Phys. Rev., 74, 230-231 (1948) @footnote 2@W.H. Brattain and J. Bardeen, Phys. Rev., 74, 231-232 (1948) @footnote 3@J. Bardeen and W.H. Brattain, U.S. Patent No.2,524,035 (filed June 17, 1948; issued Oct. 3, 1950) @footnote 4@J.E. Lilienfeld, U.S Patent No. 1,745,175 (filed Oct. 8, 1926; issued Jan. 18, 1930) @footnote 5@J. Bardeen, Phys. Rev., 71, 717-727 (1947) @footnote 6@J.N. Shive, Phys. Rev., 75, 689-690 (1949) @footnote 7@W. Shockley, Bell Sys. Tech. J., 28, 435-489 (1949) @footnote 8@W.Shockley and G.L. Pearson, Phys. Rev., 74, 232-233 (1948) @footnote 9@J. Bardeen, U.S. Patent No. 2,524,033 (filed Feb. 26, 1948; issued Oct. 3, 1950) @footnote 10@C.T. Sah, Proc. IEEE, 76, 1280-1326 (1988)

Manufacturing Science and Technology
Room Hall A-C - Session MS-TuP

Poster Session

MS-TuP1 Perfluoroelastomer Sealing Performance in Plasma Environments, ***S. Wang***, *J.M. Legare,* DuPont Dow Elastomers, L.L.C.

Perfluoroelastomers (FFKM, e.g. Kalrez, etc.) are widely used as seals on semiconductor wafer processing equipment where plasma technology is applied. These processes include etching, ashing and plasma enhanced chemical vapor deposition. The seals need to exhibit good plasma resistance in order to withstand chemical attack and maintain sealing functionality. The seals must contribute minimal contamination to the process, hence particle generation and metallic contamination are of major concerns when selecting sealing materials. This paper discusses the interactions of plasma with sealing materials, and the test methods used in the evaluation, and then compares the performance of various FFKM's with varying compositions. The results indicate that conventional FFKM products, which contain carbon black or mineral fillers, are not suitable for plasma applications where both etch rate/weight loss and particle generation are critical. Unfilled FFKM's, or FFKM's with fillers that react with plasma to form volatiles, are better suited for sealing applications on semiconductor wafer processing equipment where reactive plasmas are used.

MS-TuP2 A Novel Power Supply with Arc Handling for High Peak Power Magnetron Sputtering, ***D.J. Christie***, *F. Tomasel, W.D. Sproul, D.C. Carter,* Advanced Energy Industries, Inc.

The potential of high peak power magnetron sputtering has created growing interest, because it can generate a dense plasma with high target material ion content. At the required power densities, process arcs are not avoidable. Unless properly handled, arcs generate macro-particles and target damage, limiting the usefulness of the technique. However, coatings quite suitable for industrial applications may be applied if the pulsed supply incorporates arc handling. We have created such a power supply, capable of peak powers up to 3 mega-Watts and peak currents to 3000 A, at discharge voltages reaching 2 kV. It has voltage ring-up capability for pulse by pulse plasma ignition. This new power supply technology enables the practical application of a whole new range of sputtering processes, based on pulsing magnetrons to high peak powers.

MS-TuP3 GaAs Recycling using Supercritical Fluid SCFCO@sub2@ with O@sub2@ and H@sub2@O, ***T. Momose***, *O. Otomo,* Miyagi National College of Technology, Japan

Contamination with valuable and poisnous metals such as GaAs dust produced in semicondutor technology must be controlled not to contaminate our life cycles. Most of the metals are embeded underground sealed by concrete, but not complete. Therefore, supercritical fluid (SCF) carbon dioxide (CO@sub2@) with high solubility for organic compounds was employed for simpler recycling for metals.@footnote 1@ Samples were GaAs(1:99) grains obtained from the wall of the sputtering apparatus. They(0.5 g) were kept in SCFCO@sub2@ with H@sub2@O of 4 c.c. for 30 min at a constant temperature and pressure. The treated water was analyzed using ICP (Vop-MarkII, Kyoto-Koken or Z-5700, Hitachi). However, the solubility of GaAs using SCFCO@sub2@ with H@sub2@O was low about 30 mg/L for As @footnote 2@. Therefore, to increase solubility, oxygen gas (O@sub2@) was introduced into the treatment chamber and SCFCO@sub2@ was filled and treated. The solubility at 50 °C for 30 minute was 3 g/L at 10-30 mega-Pascal (MPa) in SCFCO@sub2@ with O@sub2@ of 0.05 MPa and 6 g/L at 25 MPa in SCFCO@sub2@ with O@sub2@ of 0.15 MPa. The addition of O@sub2@ into SCFCO@sub2@ is effective to increase the solubility of Ga about two orders.@footnote 1@ T.Momose et.al, JVST, A17(4), Jul/Aug, 1999, 1391.@footnote 2@ T.Momose et.al, Proc. 55th Appl. Phys. Tohoku Local Conf., 8pB7, Tohoku Univ., Dec. 2000, 198.

MS-TuP4 Progress toward Spatially Programmable CVD, ***J. Choo***, *L. Henn-Lecordier, Y. Liu, R.A. Adomaitis, G.W. Rubloff,* University of Maryland

A preliminary sequence of experimental tests performed to obtain engineering performance data for the Programmable CVD reactor system, together with simulation-based analysis of these data, will be described in this paper. The Programmable Reactor system was developed to improve across wafer sensing and control of reactant gas composition; to demonstrate this concept, a 3-segment prototype reactor was constructed by modifying a commercial tungsten CVD cluster tool. The key design features of the prototype system include a segmented showerhead assembly which allows control of precursor gas composition to each segment, a reversed flow of residual gas up through the showerhead to reduce inter-segment gas transport, and in-situ residual gas sampling tubes within each segment. These modifications constitute a major evolution in actuator and sampling capabilities relative to conventional CVD designs. To assess the ability of the prototype system to control gas composition across the wafer surface, a sequence of experiments was performed in which the spacing between the showerhead assembly and wafer surface was varied; pure Ar, WF6, and H2 was fed to each of the 3 segments in each test. Visual observations of the deposition patterns demonstrate sharp hexagonal deposition patterns corresponding to the shape of the showerhead segments for the close-spaced experiments; the pattern becomes more diffused as spacing is increased due to increased across-wafer diffusion. Surface resistance measurements reveal the thickest deposition directly under the WF6-fed segment and measurable deposition under Ar and H2 fed segments; simulation analysis of transport within the 1D segments will show that there is significant back-diffusion down each segment from a common exhaust volume, accounting for the observed deposition patterns.

MS-TuP6 Effects of Oxidant on Polishing Selectivity in the Chemical Mechanical Planarization of W/Ti/TiN Layer, ***K.J. Lee***, *Y.-J. Seo,* DAEBUL University, Korea*; S.Y. Kim,* ANAM Semicondctor Co., Inc., Korea*; W.S. Lee,* Chosun University, Korea

Tungsten is widely used as a plug for the multi-level interconnection structures. However, due to the poor adhesive properties of tungsten on SiO2 layer, the Ti/TiN barrier layer is usually deposited onto SiO@sub 2@ for increasing adhesion ability with tungsten film. Generally, for the tungsten-chemical mechanical polishing (W-CMP) process, the passivation layer on the tungsten surface during CMP plays an important role. In this paper, the effects of oxidants controlling the polishing selectivity of W/Ti/TiN layer were investigated. The alumina(Al@sub 2@O@sub3@) abrasive containing slurry with 5 % H@SUB2@O@SUB2@ as the oxidizer was studied. As our preliminary experimental results, very low removal rates were observed for the case of no-oxidant slurry. This low removal rate is only due to the mechanical abrasive force. However, for Ti and TiN with 5 % H@SUB2@O@SUB2@ oxidizer, different removal rate was observed. The removal mechanism of Ti during CMP is mainly due to mechanical abrasive, whereas for TiN, it is due to the formation of metastable soluble peroxide complex. This work was supported by Korea Research Foundation Grant(KRF-2002-005-D00011).

MS-TuP7 Slurry Characteristics by Surfactant Condition at Copper CMP Process, ***I.P. Kim***, *N.H. Kim,* Chung-Ang University, Korea*; J.H. Lim,* Growell Telecom*; S.Y. Kim,* Dongbu-Anam Semiconductor, Korea*; E.G. Chang,* Chung-Ang University, Korea

Copper is rapidly replacing aluminum interconnections due to its higher conductivity and lower electrical resistance in the semiconductor industry. Therefore, CMP (chemical mechanical polishing) is essential technology in microelectronic fabrication for the planarization of globally complex device topography. In this study, we evaluated the characteristics by the addition of 3 different kinds of nonionic surfactant to improve the dispersion stability of slurries. Slurry stability is an issue in any industry in which settling of particles can result in poor performance. So we observed the variation of particle size and settling rate when the concentration and addition time of surfactant are changed. When the surfactant is added after milling process, the particle size and pH became low. It is supposed that the particle agglomeration was disturbed by adsorption of surfactant on alumina abrasive. The settling rate was relatively stable when nonionic surfactant is added about 0.1-1.0 wt%. When molecular weight (MW) is too small like Brij 35, it was appeared low effect on dispersion stability. It is assumed that it can't prevent coagulation and subsequent settling with too small MW. The proper quality of MW for slurry stability was presented about 500,000. Consequently, the addition of nonionic surfactant to alumina slurry has been shown to have very good effect on slurry stabilization. If we apply these results to copper CMP process, it is thought that we will be able to obtain better yield.

MS-TuP8 A Study on Recycle of Abrasive Particles in One-used Chemical Mechanical Polishing (CMP) Slurry, ***S.W. Park***, *Y.-J. Seo,* DAEBUL University, Korea*; S.Y. Kim,* ANAM Semiconductor Co., Inc., Korea

Recently, the recycle of CMP (chemical mechanical polishing) slurries have been positively considered in order to reduce the high COO (cost of ownership) and COC (cost of consumables) in CMP process. Among the composition of slurries (buffer solution, bulk solution, abrasive particle,

oxidizer, inhibitor, suspension, antifoaming agent, dispersion agent), the abrasive particles are one of the most important components. Especially, the abrasive particles of slurry are needed in order to achieve a good removal rate. However, the cost of abrasives is still very high. In this paper, we have collected the silica abrasive powders by filtering after subsequent CMP process for the purpose of abrasive particle recycling. And then, we have studied the possibility of recycle of reused silica abrasive through the analysis of particle size and hardness. Also, we annealed the collected abrasive powders to promote the mechanical strength of reduced abrasion force. Finally, we compared the CMP characteristics between self-developed KOH-based silica abrasive slurry and original slurry. As our experimental results, we obtained the comparable removal rate and good planarity with commercial products. Consequently, we can expect the saving of high cost slurry. This work was supported by Korea Research Foundation Grant(KRF-2002-041-D00235).

MS-TuP9 Corrosion Characteristics of Diffusion Barrier Ta in Copper CMP, ***D.W. Lee***, *N.H. Kim,* Chung-Ang University, Korea*; J.H. Lim,* Growell Telecom*; S.Y. Kim,* Dongbu-Anam Semiconductor*; E.G. Chang,* Chung-Ang University, Korea

The diffusion barriers are require for Cu metallization because of the higher diffusivity of Cu in Si and dielectrics. Several barrier materials such as TiN, W, and Ta(TaN) have been studied for diffusion barrier. Among them, Ta-based diffusion barrier has been put emphasis on presently. Ta-base diffusion barrier has no reaction with Cu, better adhesion to both Cu and dielectric, desirable microstucture against Cu diffusion, and heteroepitaxial relationship with Cu. On this study, The corrosion characteristics of the diffusion barrier Ta in Copper Chemical Mechanical Polishing has been investigated. Key experimental variables that has been investigated are the corrosion rate by different agents containing slurry of Cu CMP. Whenever Cu and Ta films were corroded adding each oxidizer, the corrosion rate of Ta was much lower than that of Cu. That is, the difference in the corrosion rates of Ta by oxidizer was not larger as compared with Cu. As corroded by complexing agents, the corrosion rate of Ta was close to 0. The corrosion rate of Ta increased as added HNO@footnote 1@ and CH@footnote 2@COOH compared with the reference slurry; on the other hand, it decreased with addition of HF. In addition, resulting corrosion rate went up with lower pH of agent. However, the corrosion rates by agents were significant small. Hence, it doesn't affect on the removal rate of Cu CMP practically. Consequently, this can be explained by assuming that the mechanical effect dominates than the chemical effect on the polishing rate of Ta(TaN). @FootnoteText@ @sub 3@ @sub 3@.

MS-TuP10 Measurement of Energy Flux at the Substrate in a Magnetron Sputter System Using an Integrated Sensor, ***S.D. Ekpe***, *S.K. Dew,* University of Alberta, Canada

Knowledge of the energy flux in a sputter deposition system is essential in predicting the properties of the growing film. The use of discrete sensors such as thermocouples for heat measurement has a potential contact problem due to the temperature jump between the surface of the wall and the surrounding gas especially at very low pressures. Embedded sensors such as a microfabricated polysilicon thin film thermistor eliminates the problem associated with the discrete sensors. In this study, the fabricated sensor is calibrated using ohmic self-heating before the deposition plasma is switched on, and also after the plasma is switched off (passive mode). At low pressures (up to 20 mTorr), pressure has an insignificant effect on the thermal resistance of the sensor. For substrate temperatures of up to 250°C, the sensor response is linear with input power. Values of steady state energy flux measured with the sensor range from 5 to 46 mW/cm@super2@ for aluminum and 14 to 114 mW/cm@super2@ for copper depending on the process conditions, and compare well with those determined theoretically. Magnetron power was varied between 75 and 300 W, gas pressure 5 - 10 mTorr and substrate-target distance 10.8 - 21 cm.

MS-TuP11 Temperature Sensor for Multi-layered Substrate using Optical Fiber type Low-coherence Interferometry, ***K. Takeda***, *T. Shiina, M. Ito, Y. Okamura,* Wakayama University, Japan*; N. Ishii,* Tokyo Electron Ltd., Japan

Multi-layered substrates, such as silicon on insulator (SOI) are very useful for MEMS and so on. In the fabrication processes of multi-layered substrates, plasma etching is frequently employed. In such process, the temperature control of each layer, especially top layer, will be required to realize much finer pattern because the interlayer of SOI etc. is dielectric with low thermal conductivity. We have developed novel temperature sensor for measuring each layer of multi-layered substrates using low-coherence interferometry. The sensor is based on Michelson interferometer, which consists of a super luminescent diode (SLD: wavelength = 1550 nm), a laser diode (LD: wavelength = 850 nm), a scanning reference mirror, optical fibers and so on. In this sensor, the optical pass length of each layer is derived from the length between peaks of SLD interference signals. The shift of each optical pass length is precisely measured by Michelson interferometer using LD, which uses the same optical path as that using SLD. The sensor is, therefore, robust to mechanical and temperature disturbances. We have evaluated the shift of each layer of the three-layered substrate. The top and bottom layers of the substrate are silicon, 360 μm in thickness. The interlayer is made of quartz, 1 mm in thickness. As a result, it has been verified that the shift of optical length of each layer is proportional to each temperature measured by thermo-couple sensors, which corresponds to theoretical values. From these results, we have confirmed that the developed sensor can measure the temperature of each layer without continuous monitoring the shift of optical pass length if the initial temperature is known.

MS-TuP13 Calibration Standards for X-ray Metrology Systems using a Traceable High-resolution Diffractometer, ***D. Windover***, *J. Cline,* National Institute of Standards and Technology

The wealth of information that can be obtained from the characterization of thin film structures by means of X-rays techniques has lead to a dramatic increase in their use in recent years. However, currently their are no traceable standards available to calibrate the behavior of these new specialized characterization systems. High resolution X-ray instruments require an entirely new type of artifact to characterize both the the parallel beam optics and the performance of the goniometers. Likewise, X-Ray reflectivity requires accuracy in the incident and reflection angles orders of magnitude higher than needed for previous conventional powder diffraction calibration. This work details current efforts for providing NIST Standard Reference Materials for high resolution X-ray diffraction and reflectivity that are traceable to the SI. We focus primarily on the construction and calibration of an advanced X-ray diffractometer designed from the onset to offer flexibility in its configuration and traceable measurements. Features include: high intensity, well characterized, parallel beam X-rays produced using a rotating anode and finely controlled goniometer rotations with both accuracy and precision monitored by optical encoders. We discuss the calibration of the accuracy for the @theta@ and 2@theta@ axes through the method of circle closure. We demonstrate both vibration and temperature effects on goniometer positioning and discuss current improvements to the system designed to account for these effects. Proposed structures for high resolution and reflectivity standards will be presented.

Manufacturing Science and Technology
Room 326 - Session MS-WeM

Sensors, Metrology, and Control
Moderator: A. Diebold, SEMATECH

8:20am **MS-WeM1 Critical Dimension and Remaining Film Thickness Within Wafer Uniformity Improvement by Advanced Process Control Based on Optical Integrated Metrology**, ***J. Luque***, *G.P. Kota, V. Vahedi,* Lam Research Corporation

The first generation of advanced process control using integrated metrology in polysilicon etch processes has been focused on correcting wafer averaged critical dimension (CD). Schemes have ranged from feed-forward to feed-forward/feedback closed loop control. In all these cases the information from optical CD is used to obtain a target wafer averaged CD and minimize the lot-to-lot and within lot- variations of post-etch CD by correcting perturbations from lithography and etch steps. In the present work we explore some of the cases where improvement of isolated to dense loading, within wafer CD uniformity after gate etch or uniformity of the remaining films in recess etch applications is important. Because device performance is directly related to the CD, it is necessary to improve the uniformity of the CDs as much as is important to reach the specific target CD. Correction of the CD within wafer uniformity can be achieved by feedback of the CD information to the track/scanner cluster (litho step) or by feed-forward to the etch module. We show how non-uniformities generated in a concentric pattern by the litho step can be partially or completely eliminated during the etch step using a tunable temperature gradient in the chuck of a Lam Versys 2300 etching system. This approach to improve CD uniformity opens a path to more complex advanced process control that will deliver simultaneous CD and uniformity control. The results from this method should be better than those from schemes based on just averaged CD control. Similar approach is investigated in etch processes that can be characterized by simple thin film measurement instead of full optical profile characterization.

8:40am **MS-WeM2 Real-time In-situ Chemical Sensing in GaN MOCVD for Advanced Process Control**, ***S. Cho***, *G.W. Rubloff,* University of Maryland; *M.E. Aumer, D.B. Thomson, D.P. Partlow,* Northrop Grumman Corporation

Gallium nitride is a strong candidate material for next generation semiconductor devices for high frequency, high power electronic applications. Despite the potential of this material, the industry has yet to realize a systematic methodology for reproducible manufacturing at the high performance levels envisioned. As a joint project between the University of Maryland and Northrop Grumman, we have addressed this challenge with the use of a real-time in-situ chemical sensing technique. Residual gas analysis downstream to the MOCVD process has enabled us to monitor in real-time the by-product species due to the deposition reaction as well as other background impurity species inherent to the process. A metric derived from the by-product signals provided us with a real-time means for accurately predicting the crystal quality of the material as determined by the post-process ex-situ XRD (X-ray Diffraction) with an average uncertainty of 5% or less. Background impurity levels in the gas-phase were also closely correlated to the post-process ex-situ PL (Photoluminesence) measurements for material quality. In addition, time-integration of the by-product signals during the deposition process generated metrology for predicting and controlling the thickness of the individual layers in the GaN-based HFET structure. This creates opportunities for advanced process control based on real-time in-situ sensing, with the promise of major benefit in reproducibility and cost reduction in GaN-based semiconductor manufacturing.

9:00am **MS-WeM3 Flexible Simulation Tools for Design, Control, and Optimzation of Semiconductor Processing Systems**, ***R.A. Adomaitis,*** University of Maryland **INVITED**

Physically based simulations are valuable tools for understanding the chemical and physical mechanisms responsible for spatial non-uniformities in films produced by chemical vapor deposition systems. In this talk, an alternative will be presented to the "traditional" (e.g., CFD-based) approaches to high-fidelity equipment simulation. This work was motivated by the need for flexible simulation tools that allow rapid evaluation of reactor design choices and that interface readily with available optimization, process control, and numerical analysis tools. An object-oriented framework was created to generate modular simulation elements corresponding to CVD reactor physical components, as well as simulator elements derived from the abstraction of boundary-value problem based model solution (global spectral) methods and the other numerical methods necessary to solve the nonlinear equation models. The role of information technology issues and distributed computing concepts in implementing this framework will be presented. Results of our simulation-based design and prototype testing of the Programmable Chemical Vapor Deposition reactor system, a highly-controllable CVD system under development at UMd, and our interaction in redesigning CVD systems with an industrial research partner will be discussed. It will be shown that the flexibility built in to the simulation methodology from the outset is critical to enabling a relatively rapid simulation/experimental-evaluation/redesign cycle in these CVD reactor design and construction projects.

9:40am **MS-WeM5 Spatial Uniformity as a Key Challenge in Semiconductor Process Control**, ***D.S. Boning,*** Massachusetts Institute of Technology **INVITED**

Semiconductor process control has advanced to address manufacturing needs -- primarily wafer to wafer uniformity of device and interconnect structures -- using improved metrology, real-time, and run-by-run control techniques. Here, the need for improved spatial uniformity is discussed, and the challenges for advanced process control in achieving these needs outlined. First, the impact of variation on integrated circuits of wafer to wafer, within wafer, and within die variation is considered, highlighting that yield and performance can depend at least as strongly on spatial uniformity as on wafer to wafer uniformity. Within die uniformity in particular pose difficult challenges; examples include uniformity in interconnect geometry (e.g. pattern dependent CMP and plating effects such as copper dishing and erosion), as well as device geometry and electrical properties (e.g. channel length variation due to lithography and plasma etch pattern dependencies). Finally, the resulting needs and challenges for process control are discussed: metrology must evolve to enable observation of within die variations, models are needed to relate control parameters to within die as well as across wafer results, and algorithms are needed that can address both spatial and temporal variation objectives.

10:20am **MS-WeM7 In-situ Defect Metrics Based on Real-Time Sensor Integration and Analysis**, ***J.A. Mucha,*** INFICON, Inc.

The concept of advanced metrology is not new to the semiconductor industry. However, the focus of attention always seems to be on increasing the capabilities of visual inspection for defects even though yield-affecting defects include non-visible electrical defects, parametric defects and electrical faults whose root cause is often difficult to determine. The "2001 SIA International Roadmap for Semiconductors: Yield Enhancement" notes that current Data Management Systems (DMS) have limited abilities to incorporate real-time in-situ sensor data that can be correlated with lot and wafer-based data. Further, current DMS are even more limited in their abilities to use the information in a yield-predictive way in spite of the fact that real-time analysis of such data would result in more rapid identification and prioritization of defect generating mechanisms to a broad sector of engineering group. In this presentation, the sensor-integration and analysis system, FabGuardÃ¢, is used to address these shortcomings by combining sensor output with logic and signal analysis to create real-time in-situ metrics for wafer health. These can then be used to track potential non-visible yield-loss defects in a way that can drive continuous product improvement with decreased emphasis on in-line and ex-situ metrology. The use of residual gas analysis in monitoring the degas operation in PVD cluster tools is shown to be a capable for generating metrics that sensitive to process variations exhibited by prior processing equipment such as etch, ash and CVD. Case studies of applying this metrology are presented that identify root causes of contamination-induced yield-limiting defect mechanisms.

10:40am **MS-WeM8 Prototype Development of Four-Point Probe with 100 µm Probe-Spacing for Resistivity Measurements**, ***M. Suzuki***, *Y. Sato, T. Ogiwara,* NTT-AT, Japan; *S. Kiyota, K. Watanabe,* Kiyota Manufacturing Co., Japan; *N. Matsubayashi,* AIST, Japan; *S. Matsumoto,* Keio University, Japan

The four-point probe technique has been used commonly to measure the semiconductor resistivity. It is, however, difficult to detect changes in resistivities over distances smaller than 3 mm because of the standard probe-spacing of 1 mm. With the reduced dimension of devices, it is very significant to determine resistivity variations on a very small scale. Thus we have developed the prototype of the four-point probe with 100 µm probe-spacing and confirmed the adaptability for practical use. The four probes are made from 50-µm-diameter tungsten carbide wire, and their apexes are ground down to a radius of 20 µm. It is found that the tip apex is

durable and is not contaminated after 1.5 x 10@super 5@ times probing onto the Si surface. The measurement system is constructed with mechanical driving parts, a commercial dc current source, and a digital voltage meter under the design concept same as the conventional four-point probe technique. We have demonstrated that it is possible to measure the resistivity radially across a Si wafer very near the wafer edge (about 0.5 mm), while conventional system with 1 mm probe-spacing was limited to measure the resistivity to the points of about 4 mm from the wafer edge. This 100-μm probe can also measure the resistivity in the phosphorus-doped poly-silicon film of 0.5 x 0.5 mm@super 2@ on an oxidized Si wafer. Our results suggest that the probe can measure a resistivity distribution on one LSI chip area, and that this system will be used as a monitoring tool for various fabrication processes. This project was performed with the financial support of Ministry of Economy, Trade, and Industry, Japan.

Vacuum Technology
Room 323 - Session VT+MS-ThM

Reproducibility, Precision, and Accuracy of Vacuum and Process Measurements

Moderator: R. Dobrozemsky, Vienna University of Technology, Austria

8:20am **VT+MS-ThM1 Component Requirements for ALD Technology**, ***T.E. Seidel,*** Genus, Inc; *J. Mason, A. Londergan, S. Ramanathan,* Genus, Inc. **INVITED**

In the last several years Atomic Layer deposition (ALD) has emerged as a commercial technology. This technology is a variant of CVD, and therefore requires reactor and reactor related components for operation under well-controlled vacuum conditions. The requirements include fast gas switching, precisely controlled gas delivery systems with high performance Mass Flow Controller and / or Pressure Controllers, precise control of gas delivery line temperatures, heated walls and substrate susceptors, and quality down stream pumps to provide suitable flow and pressure capacity. Precursor usage and costs must be managed as well. Ancillary requirements include sensitive RGA's and fast response baratrons. There are gaps in he performance of components and the users requirements. As and example, today's fast gas switching valves have a lifetimes of the order of one to a few million cycles, but lifetimes of the order of 10 million cycle are needed. Substrate and gas line temperature control is critical. Additionally, because the precursors used in this technology are particularly reactive, the downstream pump components must be robust. This review provides a generic status and progress of the ALD field followed by generic requirements and requirement gaps for components used in ALD.

9:00am **VT+MS-ThM3 Towards Improved Control of PVD Processes for Nano-Structured Me-aC:H Coatings@footnote 1@**, ***M.A. Taher,*** *B. Feng, A.G. Shull,* Caterpillar Inc.; *B. Johs, G. Pribil,* J.A. Woollam Company Inc.; *C.C. Klepper, E.P. Carlson, R.C. Hazelton, E.J. Yadlowsky,* HY-Tech Research Corporation

The reliability and durability of machine components such as bearings and gears can be enhanced through the application of metal-containing amorphous carbon (Me-aC:H) coatings, deposited by physical vapor (PVD) techniques such as sputtering. Commercial sputtering systems used for tribological coatings often employ computerized recipe managers to attain a certain level of reproducibility in the coating process. In most cases, these recipe managers control the deposition process through an open loop, time stepping approach where deposition parameters are varied within a particular time frame, and the process is repeated consistently from batch to batch. This type of control generally provides a level of reproducibility that is acceptable in applications where the component benefits from the coating but does not depend on it for full functionality. However, in applications where the coating is integrated into the machine component design, creating a prime-reliance on the coating, higher levels of coating consistency are required. Such levels may involve the adoption of in-situ sensors integrated with a closed-loop deposition control system. To build such a successful control system, knowledge of the relationships between the input process factors, the sensed variables, and the critical coating characteristics is necessary. In this study, a set of in-situ sensors that included a residual gas analyzer, an optical emission spectrometer, an optical absorption spectrometer, a Langmuir probe and a spectroscopic ellipsometer were explored. Three Design-of-Experiment (DoE) test runs were conducted which explored the effects of the coating process input factors on the output sensor signals and the critical coating characteristics. Results of these experiments are presented and a closed-loop control strategy is discussed. @FootnoteText@ @footnote 1@This work was partially supported by the Department of Commerce through its NIST ATP program award number 70NANBH0H3048.

9:20am **VT+MS-ThM4 A Portable Reference Gas for InSitu Calibration of Residual Gas Analyzers**, ***R.E. Ellefson,*** *W.P. Schubert, L.C. Frees,* INFICON, Inc.

A new design for a portable source of reference gas with a fixed flow rate has been developed for producing a repeatable pressure in the ion source of a residual gas analyzer (RGA). The fixed flow rate of gas flowing through the fixed conductance of the isolation valve located between the process vacuum system and the RGA produces a repeatable pressure at the ion source of the RGA. The flow rate of 1x10@super -4@ Torr-l/s of Ar (and selected impurities) through the typical conductance of 10 l/s produces a reference pressure of 1x10@super -5@ Torr in the ion source. The ability to produce a repeatable pressure at the ion source on demand enables calibration of the mass scale, electron multiplier (EM) gain and measurement of absolute sensitivity. Data on sensitivity versus time is shown as an example of a quality assurance method for determining the stability of operation of an RGA and to determine when sensitivity or EM gain adjustment is necessary. The same reference gas source can be used for the calibration of closed ion source RGAs that have their own pumping system. The mechanical design minimizes the pressure burst at turn on and accomplishes viscous flow of the gas mixture. Data is presented on consumption rate, expected lifetime, shipping exemptions, temperature dependence of flow rate and species fractionation over lifetime. Methods for species abundance calibration in the RGA are also presented.

10:00am **VT+MS-ThM6 Specific Reference Calibration - A More Practical Approach to Vacuum Reproducibilty**, ***G.D. Lempert,*** Soreq N.R.C., Israel

Increasing demands for quality control, both in production as well as in R&D, have resulted the proliferation of instrument measurement calibration. However, despite the fact that vacuum measurement is often made with significantly larger uncertainties and errors than other physical or thermodynamic quantities, the calibration of vacuum measurement instrumentation, in particular in the high vacuum range, is generally ignored or neglected. Objective practical difficulties have been identified and defined which make vacuum measurement calibration problematic and very often not practically feasible. The requirements for vacuum measurement uncertainties for most practical vacuum systems have been assessed. In an effort to make reproducible vacuum measurement more accessible, a more practical approach to vacuum measurement calibration has been defined and developed. The approach incorporates a vacuum calibration system, whose specifications and design satisfy the accuracy requirements for all but the most demanding users of vacuum technology. Calibration results are presented which provide justification for the approach. In addition the new approach defines a concept of Specific Reference Calibration, SRC. SRC does not necessarily provide calibration of the users vacuum measurement instruments. However SRC does enable practically defining and attaining reproducible vacuum process conditions in the users vacuum system, with significant advantages over conventional calibration. The new approach is aimed to overcome the difficulties, which have inhibited the proliferation of vacuum measurement calibration up to this time, and to facilitate the attainment of reproducible vacuum conditions and processes.

10:20am **VT+MS-ThM7 Characterisation of a Fully Automated, Static Expansion Vacuum Standard at the National Physical Laboratory, UK**, ***J.C. Greenwood,*** *P. Carroll,* National Physical Laboratory, UK

A new, fully automatic, Static Expansion vacuum standard has recently been constructed to replace the existing manually operated system. The new instrument incorporates a number of design improvements which will be described. It is of all metal construction and operates from atmospheric pressure down into the UHV region. This paper discusses some of the procedures and measurements that have been performed to characterise the new standard. These include; mapping temperature distributions across and between the parts of the system; measuring the effects of inter-vessel valves on the pressure distribution; developing an improved measurement equation for the pressure generated in the standard, and comparison against existing vacuum standards that have been involved in recent international comparisons. We will show that calibration results taken from the new standard and the existing standards are equivalent.

10:40am **VT+MS-ThM8 A New Look at the Modulated Bayard-Alpert Gauge**, ***B.R.F. Kendall,*** Elvac Laboratories; *E. Drubetsky,* Televac Division of The Fredericks Company

There is an increasing need for accurate vacuum measurements below 10@super-9@ Torr. Ordinary Bayard-Alpert gauges may have large and unpredictable errors at these pressures because of x-ray and other unwanted effects. Several special gauges have been developed to overcome these problems. One of the most cost-effective is the Modulated Bayard-Alpert Gauge (MBAG), first described by P.A. Redhead in 1960 and subsequently investigated in detail in many other laboratories. These gauges were widely used in Europe for several decades. We have evaluated several different MBAGs, ranging from first-generation glass-envelope types to a new miniature metal-envelope version. Performance data are given for operation in various modulation modes. An advantage of these gauge tubes is that, if necessary, they can be used as conventional BA gauge tubes with existing controllers. Some versions can be electronically adjusted for uniform sensitivity. The design of demodulation circuitry is discussed. X-ray errors causing gauges to over-read by several hundred

percent at 10@super-10@ Torr can be essentially eliminated by using the modulation principle.

11:00am **VT+MS-ThM9 Dose Reproducibility in Axcelis GSD Implanters Using Stabil-Ion Gauge**, ***R.C. Johnson,*** INNOViON Foundry Ion Implantation Engineering

Long-term dose reproducibility and tool to tool dose matching in the Axcelis GSD end-station is critically dependent on process chamber pressure measurement and Pressure Compensation factor selection. Pressure Compensation factor (PCOMP) determination is well-established. Pressure measurement in the GSD end-station depends on accurate, repeatable gauge capability: incorrect pressure measurements directly lead to dose errors. For example, the dose equation using PCOMP tells us that for a modest PCOMP value of 30%, a chamber pressure measurement error of 2E-5 torr can result in a dose error up to 6% at normal process pressures. The original HCIG used for pressure measurement was not capable of meeting the requirements for good dose control since gauge to gauge differences were not controlled and gauge accuracy was only on the order of 30%. Axcelis introduced the Granville-Phillips 360 Stabil-Ion gauge to improve dose reproducibility through much improved gauge to gauge matching (+/-6%) and more accurate gauge output. This paper discusses the details of the care and feeding of the Stabil-Ion gauge system and it's impact on process dose and process trends.

11:20am **VT+MS-ThM10 How Stable are Spinning Rotor Gauges**, ***R.F. Chang,*** National Institute of Standards and Technology

The spinning rotor gauge is an excellent transfer standard in the pressure range of 0.0001 to 10 Pa (10@super -6@ to 0.1 torr) because of the remarkable stability exhibited by its accommodation coefficient. The stability comes from the fact that the accommodation coefficient depends mainly on the rotor surface properties of roughness and cleanliness, and does not change as long as these surface properties remain the same. Therefore, as common sense might dictate, one must avoid altering the rotor surface properties mechanically or chemically by not scratching the rotor surface or exposing it to corrosive agents. It is important that the accommodation coefficient remain constant when a spinning rotor gauge is moved from one laboratory to another such as in an inter-laboratory comparison or proficiency test. The level of confidence of the agreement between two laboratories is limited by how much the accommodation coefficient may have shifted in transit. For example, to transfer a spinning rotor gauge from one vacuum chamber to another, one must remove and reinstall the suspension head. During this procedure, the rotor comes into contact with the inner wall of the vacuum housing (thimble) and may be scratched. Sometimes the rotor is removed from the thimble for shipping, which requires additional handling of the rotor. By measuring the accommodation coefficient before and after various handling and cleaning procedures, we have quantified their effects on the accommodation coefficient. The results and impacts on gauge calibrations, including some surprises, will be presented and discussed.

11:40am **VT+MS-ThM11 Practical Procedures for the Frequency Corrections of the Spinning Rotor Gauge Residual Drag**, ***J. Setina,*** Institute of Metals and Technology, Slovenia

Spinning rotor gauge (SRG) uses a magnetically levitated steel ball as sensing element to measure low gas pressure, which is determined from the decay of the rotational speed of the rotor caused by the momentum transfer to the surrounding gas molecules. In addition we also have a small, gas pressure independent component to the measured SRG signal. This is called a residual drag (RD), and the main sources are eddy currents induced in the ball by asymmetries in the magnetic suspension field and eddy currents induced in surrounding metallic components by the rotating component of the ball's magnetic moment. In general, the RD depends on the ball rotational speed. The SRG operates the ball in a pre-selected frequency window, usually from 405 to 415 Hz, and the RD changes during the gas pressure measurement as the ball speed changes. The frequency dependence can be observed as saw-tooth variation of readings during continuous operation at constant pressure. For accurate measurements the frequency dependence of the RD has to be considered also. The commercial SRG controllers do not have the ability to take into account the frequency dependence of the RD and to make automatic on line corrections. The corrections have to be done separately by the user. We will describe our methods to determine the frequency dependence of the residual drag and procedures to perform the corrections to the pressure readings. The RD and its frequency dependence are unpredictable in magnitude for a given suspension of the rotor. Both can change considerably when the rotor is re-suspended. It is our experience that the frequency dependence remains reproducible during uninterrupted suspension, if vertical alignment or position of the suspension head stays well fixed. It is our experience also, that the behavior of the RD of the same ball is different in various suspension heads of different SRG controllers.

Author Index

Bold page numbers indicate presenter