Monday Morning, November 3, 2003

High-k Gate Dielectrics and Devices Topical Conference
Room 317 - Session DI-MoM

Electronic Properties of High-k Dielectrics and their Interfaces

Moderator: R.L. Opila, University of Delaware

8:20am **DI-MoM1 Attempting the Unthinkable: Replacing SiO@sub 2@ with High-k Materials as the Gate Dielectric for Scaled Devices*, G.D. Wilk,*** ASM **INVITED**

The rapid pace of scaling CMOS technology has led to considerable attention in the area of high-k gate dielectrics. Since SiO@sub 2@ gate dielectrics are expected to have unacceptably high leakage current for most applications, high-k materials are of interest for producing lower leakage currents while maintaining similar device performance to SiO@sub 2@. Various high-k materials have been studied for this purpose recently, but it is clear that many important characteristics, which are already well known for SiO@sub 2@, have yet to be understood for any high-k material. To date, most high-k materials systems have exhibited the expected gate leakage reduction compared to SiO@sub 2@ of the same equivalent oxide thickness (EOT), but significant issues remain with respect to mobility degradation and threshold voltage shifts. Progress toward understanding these issues has been made over the past few years, yet controlling regions at both the channel and gate Si interfaces is still of critical importance to the success of any high-k material. Both physical and electrical analysis will be presented to highlight the key fundamental properties of high-k gate dielectrics, and how processing optimization has improved film quality. Characterization techniques such as electron energy loss spectroscopy (EELS) in scanning transmission electron microscopy (STEM), medium energy ion scattering (MEIS), X-ray Photoelectron Spectroscopy (XPS), Fourier transform infrared spectroscopy (FTIR) as well as electrical device properties will be presented.

9:00am **DI-MoM3 Challenges and Progress on High-K Devices and Materials*, H.-H. Tseng,*** Motorola **INVITED**

High-K gate dielectric research is critical for advanced technology because the standby power increases significantly for ultra-thin SiO2 based gate dielectric. Although progress has been made in the past, there are huge challenges remained to be solved. This paper presents the challenges and progress of High-K devices and materials. Issues related to High-K device performance such as transconductance and mobility degradation, and high threshold voltage will be discussed. Challenges of reliability related topics such as threshold voltage instability, negative bias temperature instability (NBTI), stress-induced leakage current (SILK) will also be presented. Recent progress to address these challenges will be discussed. Finally, new research directions of High-K/gate electrode stack to meet the future technology requirements will be outlined.

9:40am **DI-MoM5 First Principles Studies of the Electronic and Atomic Structures of ZrO@sub 2@/Si and ZrSiO@sub 4@/Si Interfaces*, R. Puthenkovilakam,*** *Y.-S. Lin, J.P. Chang,* University of California, Los Angeles

First principles simulations using density functional theory is employed to investigate the electronic properties of ZrO@sub 2@/Si and ZrSiO@sub 4@/Si interfaces for their potential applications in metal-oxide-semiconductor field effect transistors. Tetragonal zirconia and zircon are used to model ZrO@sub 2@ and ZrSiO@sub 4@, respectively, and the interfaces are formed by lattice matching their (001) surfaces to the Si(100) surface. The electronic structure of ZrO@sub 2@/Si interfaces showed partial occupation of zirconium d states at the Fermi level when the zirconium coordination is different from its bulk coordination. These partially occupied states lie within the silicon band gap, forming conductive paths under an applied potential field, thus are detrimental to the device performance. However, ZrSiO@sub 4@/Si interface showed no partial occupation of zirconium d states at Fermi level. Hydrogen passivation of zirconium dangling bonds as well as oxygen bridging at the interface are shown to effectively remove the partial occupancy of d orbitals. The calculated band offsets of ZrO@sub 2@/Si interfaces showed asymmetric band alignments, with conduction band offsets between 0.73-0.98 eV and valence band offsets between 3.70-3.95 eV for different zirconium and oxygen coordinations at the ZrO@sub 2@/Si interfaces. The ZrSiO@sub 4@/Si interface resulted in a more symmetric band alignment with a much higher conduction band offset of 1.90 eV and a valence band offset of 2.98 V. These results suggest that ZrSiO@sub 4@ forms a superior interface with silicon compared to ZrO@sub 2@ and can be an ideal candidate for replacing SiO@sub 2@ as a gate insulator in silicon based microelectronics and additional interface preparation or post-deposition annealing are required for ZrO@sub 2@ to yield adequate electronic properties.

10:00am **DI-MoM6 X-ray Photoelectron Spectroscopy (XPS) and Spectroscopic Ellipsometry (SE) Study of Hafnium Silicate Alloys Prepared by Remote Plasma Assisted Chemical Vapor Deposition: Comparisons between Conduction Band Offset Energies and Optical Band Gaps*, J.G. Hong,*** *N.A. Stoute, G. Lucovsky, D.E. Aspnes,* North Carolina State University

Thin films of hafnium silicate alloys, (HfO@sub 2@)@sub x@(SiO@sub 2@)@sub 1-x@, were prepared by remote plasma enhanced chemical vapor deposition (RPECVD) using down-stream injected Hf t-butoxide as the Hf source gas and silane as the Si source gas; chemically-active species from a remotely excited O@sub 2@/He plasma were used to drive the CVD reaction. Alloy compositions were determined by Rutherford backscattering (RBS), and were used to calibrate Hf-to-O spectral ratios obtained by on-line Auger electron spectroscopy (AES). XPS spectra were then obtained for the O 1s, Si 2p, Hf 4d and Hf 4f core levels, and the core level binding energies of these features were analyzed as a function of the alloy composition x. All core binding energy levels decreased (i.e., became more positive) as the Hf fraction x increased, paralleling the behaviors previously reported for O 1s, Si 3p, and Zr 3d core level energy shifts in zirconium silicate alloys. The Hf silicate alloy shifts are consistent with the charge transfer expected on the basis of the relative electronegativities of Hf, Si and O. As in case of Zr silicates, the total shift of the O 1s core level in Hf silicates, ~3.1 eV, is larger than the average shift of the Hf 4d and Si 2p core levels, ~ 2 eV. Finally, the XPS results will be compared with on-line AES, X-ray absorption spectroscopy (XAS), and vacuum ultra-violet spectroscopic ellipsometry (SE) results to determine the compositional variations of the conduction and valence band offset energies with respect to Si, and to compare theses with the compositional variation of the optical band gap.

10:20am **DI-MoM7 Photoemission Study of High-k Gate Dielectric/Si(100) Heterostructures - Chemical Bonding Features and Energy Band Alignment*, S. Miyazaki,*** Hiroshima University, Japan **INVITED**

The characterization of chemical and electronic structures of high-k dielectrics as well as the quantification of defect state distributions is of great importance for the implementation of the high-k dielectric gate stack in sub-100nm technology generations. For some high-k dielectrics such as Ta@sub 2@O@sub 5@, Al@sub 2@O@sub 3@, ZrO@sub 2@ and HfO@sub 2@, we have experimentally determined the energy band alignments to Si(100) with an thin interfacial Si-oxide or nitride from high-resolution XPS measurements and defect state distributions in the high-k dielectrics and at the interfaces form total photoelectron yield measurements.@footnote 1-3@ We have extended our research to characterize the chemical and electronic structures of Y@sub 2@O@sub 3@, Pr-silicates and Hf-aluminates on Si(100) including interfacial SiO@sub x@. In this presentation, recent our results will be review to demonstrate how the energy bandgaps of practically-thin high-k dielectrics such as HfO@sub 2@ and Y@sub 2@O@sub 3@ and of an ultrathin Si-nitride barrier can be determined from the analysis of energy loss spectra of O1s (or N1s) photoelectrons and, for the system of Y@sub 2@O@sub 3@ formed on Si(100), how the energy band alignment can be determined with combination of the measured bandgap and the valence band lineup as obtained from the analysis of XPS valence band spectra of heterostructures with thin dielectrics. Also, we show that total photoelectron yield spectroscopy is a useful tool for quantifying the energy distribution of electronic defect states for thin high-k dielectric/Si(100) systems. @FootnoteText@@footnote 1@S. Miyazaki, J. Va. Sci. Technol. B19, (2001) 2212. @footnote 2@S. Miyazaki, M. Narasaki, M. Ogasawara and M. Hirose, Microelec. Eng., 59 (2001) 373. @footnote 3@M. Yamaoka, M. Narasaki, H. Murakami and S. Miyazaki, Proc. of 2nd Int. Semicond. Technol. Conf. (2002, Tokyo) Abst. No. 57.

11:00am **DI-MoM9 Separate and Independent Control of Interfacial Band Alignments and Dielectric Constants in Transition Metal-rare Earth Ternary Oxides*, D.G. Schlom,*** Pennsylvania State University*; J.L. Freeouf,* Oregon Graduate Institute*; G. Lucovsky,* North Carolina State University

The electronic structure of transition metal, Tm, and trivalent rare earth, Re, binary (TmO@sub x@ and Re@sub 2@O@sub 3@) and ternary mixed oxides (TmRe@sub x@O@sub y@) are qualitatively different from those of silicon oxide, silicon nitride, and silicon oxynitride alloys. The lowest conduction band states are associated with localized anti-bonding d*-states of the Tm/Re atoms, rather than extended Si 3s*-states, and/or O/N 2p*-states. Based on quantitative agreement between the Zr silicate anti-bonding state electronic structure obtained from Zr M@sub 2,3@ and O K@sub 1@ XAS spectra, and ab initio calculations on small clusters, the ordering and overlap of anti-bonding Zr 4d*- and 5s*-states, and Si 3s*-states in the O K@sub 1@ spectra is the same as the features of the conduction band electronic structure that determine band-offset energies at Si-Zr silicate alloy interfaces. These relationships have been extended to Re ternary oxide compounds, including LaAlO@sub 3@ and GdScO@sub 3@, through direct comparisons between O K@sub 1@ XAS spectra and band edge optical absorption constants obtained from analysis of SE measurements extending to 9 eV. As a result of near-neighbor interactions between Tm and Re d-states induced by bonding to a common O atom, ternary oxide minimum band gaps, and conduction band offset energies are increased in oxide phases containing Tm and Re species. This identifies new and technologically important opportunities for band gap engineering at the atomic scale. Relative energy shifts of coupled Re and Tm d*-states are important for the ultimate scaling of CMOS devices since they increase the effective band gaps/offset energies for ternary oxides containing highly polarizable Sc, Ti, Nb, and Ta atoms above what had previously been proposed as a fundamental limitation inferred from the band gaps and/or band offset energies of their respective binary oxides.

11:20am **DI-MoM10 A Materials and Electronics Properties Study of the ZrO@sub 2@/Si and SiO@sub 2@ Interfaces***, **C.M. Lopez**, N.A. Suvorova,* University of North Carolina, Chapel Hill*; A.A. Suvorova, M. Saunders,* University of Western Australia*; E.A. Irene,* University of North Carolina, Chapel Hill

Zirconia, ZrO@sub 2@, thin films were grown on single crystal MgO(100), Si(100) and on amorphous SiO@sub 2@ by ion beam sputter deposition of Zr metal at room temperature and subsequent oxidation both in-situ and ex-situ at 250°C and 600°C, respectively. The optical properties of MgO, sputter-deposited Zr, and ZrO@sub 2@ were determined by in-situ spectroscopic ellipsometry in the photon energy range of 1.5-4.5 eV. Based upon ellipsometric thicknesses obtained, a volume expansion of 1.28 Zr to ZrO@sub 2@ was observed. This value is in contrast to the value assuming bulk densities, 1.54. Refractive index values for ZrO@sub 2@ ranged from 2.18 to 2.52 for the given spectral range. Time of flight mass spectrometry of recoiled ions (TOF-MSRI), analytical electron microscopy, and spectroscopic ellipsometry were used to investigate the material properties of all samples with special attention to the composition and extent of the interface formed between ZrO@sub 2@ and the Si substrate. To compliment these techniques, electrical measurements were performed on fabricated Pt/ZrO@sub 2@/Si capacitors also prepared in vacuo to determine the interface trap state density, fixed charge, and dielectric constant for the overall film stack. The nature of the interface is correlated with the resultant electronic properties of the interface.

11:40am **DI-MoM11 Interface and Materials Properties of High-k Gate Stack Structures***, **S. Sayan**, X. Zhao, R.A. Bartynski, T. Emge, M. Croft, T. Gustafsson, D. Vanderbilt, E.L. Garfunkel,* Rutgers University

In this presentation, we describe recent results using soft x-ray photoemission (SXPS), inverse photoemission (IPE), and x-ray absorption spectroscopy (XAS) to examine HfO2 gate dielectrics and their interfaces with silicon and metal layers. In selecting an alternative (high-K) gate insulator, many parameters in addition to dielectric constant and thermal stability must be considered, including the barrier heights for tunneling. The SXPS and IPES results are used to determine the densities of states above and below the Fermi energy, in particular to elicit useful information on barrier heights. We find that interface dipoles affect the "effective workfunction" of metals via change in electrostatic potential as well as the band alignments, where the specific alignment depends on the interface properties. We have also performed first-principles density functional calculations to study the properties of the crystalline phases of HfO2 and ZrO2. The densities of valence and conduction bands are calculated and compared to experimental measurements. The thickness, layered structure, and crystal phase of the as-deposited and annealed films have been studied by XRD, XAS, MEIS, RBS and HRTEM. The authors would like to acknowledge useful interactions with colleagues at and NCSU (J.P. Maria, G. Parsons, G. Lucovsky and A. Kingon), J.Robertson (Cambridge University.UK), R. Tung (CUNY) and K.P. Cheung (ECE, Rutgers University) We also acknowledge the SRC for financial support.

High-k Gate Dielectrics and Devices Topical Conference
Room 317 - Session DI-MoA

High-k Dielectric Stability

Moderator: Y.J. Chabal, Agere Systems

2:00pm **DI-MoA1 Etching and Thermal Stability of Zirconium and Hafnium Oxide High-k Dielectrics*, J.P. Chang,*** University of California, Los Angeles **INVITED**

The aggressive down-scaling of the silicon based metal-oxide-semiconductor field effect transistor (MOSFET) replies strongly on the materials and the resultant electrical properties associated with the dielectric material employed to isolate the transistor gate from the silicon. Currently, the major challenges in integrating high-k materials include a thorough understanding of the thermal stability of these materials on silicon and an effective etching chemistry in patterning these materials. In this talk, I will discuss current research progress in atomic layer controlled deposition of high-k dielectric films on silicon with tailored electronic, chemical, interfacial, thermal, and mechanical properties, followed by discussions on plasma patterning of the high-k materials. Specifically, research work on ZrO@sub 2@ and HfO@sub 2@ thin films and their thermal stability, dielectric function, and integration on silicon surfaces will be presented. The talk will focus on linking the molecular coordination and film morphology to the electronic properties of the high-k dielectrics, and elucidating the reaction pathways leading to the deposition of thermally stable, stoichiometric, amorphous, smooth, uniform, and highly conformal high-k dielectrics. Plasma enhanced etching of metal oxides in halogen based chemistries will be presented, including the effect of ion energy and ion type on etching rate and etching selectivity. I will also highlight some new research directions that aim at enabling the predictive engineering of a superior high-k/silicon interface and its associated device performance through ab initio calculations.

2:40pm **DI-MoA3 Structure and Stability of Alternative High-K Gate Dielectrics*, S. Stemmer,*** University of California, Santa Barbara **INVITED**

This talk will present an overview of extrinsic and intrinsic stability issues of high-k dielectrics, such as ZrO@sub 2@, HfO@sub 2@, Y@sub 2@O@sub 3@, their alloys with SiO@sub 2@ or Al@sub 2@O@sub 3@, and their interfaces with electrodes and Si. While thermodynamics predicts that all high-k gate dielectrics currently under investigation are stable in contact with Si, interfacial reactions have been reported. We show that gate oxide stoichiometry and processing conditions, such as oxygen excess or reducing conditions, can explain reactions and are consistent with predictions from thermodynamics. Intrinsic stability issues include phase separation of silicates and aluminates, and will be discussed in the context of equilibrium as well as metastable phase diagrams, respectively. A combination of experimental methods is needed to experimentally analyze the stability of these ultrathin layers. We have used electron energy-loss spectroscopy (EELS), atomic resolution Z-contrast imaging, high-resolution transmission electron microscopy, small angle x-ray scattering (SAXS) and x-ray absorption spectroscopy fine structure analysis (XANES) to dielectric layers after high temperature anneals necessary for CMOS device processing. For example, phase separated microstructures of Hf-silicate films with different compositions show different morphologies and kinetics, due to mechanisms of microstructural evolution by nucleation and growth, and spinodal decomposition, respectively, consistent with the predictions from metastable phase diagrams. SAXS is used to study the kinetics of phase separation. Oxygen deficiency can lead to silicide reactions, whereas oxygen excess in the films is responsible for interfacial silicate reactions in rare earth oxide films on Si. This research was performed in collaboration with J.-P. Maria, A. Kingon, G. Parsons, P. Lysaght, P. C. McIntyre, S. Ramanathan, and T.P. Ma.

3:20pm **DI-MoA5 Hafnium Silicate High-K Dielectric Etch with High Selectivity to Si at Low Wafer Temperatures***, S. Ramalingam,* Lam Research Corporation*; **C.B. Labelle,*** Advanced Micro Devices*; S.D. Lee, G.P. Kota, C. Lee, V. Vahedi,* Lam Research Corporation

Advanced microprocessors require the use of increasingly thin gate oxide materials to achieve the highest performance. To date, these materials have consisted primarily of SiO2 and nitridized SiO2, but the leakage current behavior of these materials becomes undesirable as they are successively thinned (=12Å). A potential solution to this problem is replacement of SiO2 by an insulator with a higher dielectric constant (high k). Keeping with current integration schemes, gate etching would then require etching through the polysilicon and high-k materials, stopping on the underlying silicon. However, high-k materials have proven very challenging to etch, specifically due to the low volatility of etch products, which typically require an aggressive approach to the etch, most notably including high temperatures. Key etch issues include selectivity to polysilicon/bulk silicon and masking material, redeposition of high k materials on the poly gate sidewalls, and altering of the poly gate profile and/or CD. A Lam 2300 SeriesTM silicon etch reactor has been used to etch photoresist-masked polysilicon gate wafers with HfSiOx gate dielectric. A BCl3-based process has been developed that provides excellent selectivity to polysilicon, no high k redeposition, and <10Å silicon recess. Selectivity to Si is attained at low ion energy and through passivation of the surface by formation of Si-B bonds. A key advantage of this process over those currently in practice is that wafer temperatures higher than those in typical gate etch processes are not necessary. Key etch results will be presented, including analysis of the impact of a boron-based etch process on gate doping.

3:40pm **DI-MoA6 Post Deposition Stability of High-k Dielectrics to Air Exposure and its Implications to Interface Reactivity*, T. Gougousi,*** *D. Niu, R.W. Ashcraft, G.N. Parsons,* North Carolina State University

Post-deposition stability of the gate oxide is an important issue for advanced gate stacks. For this study, group III and IV high-k dielectrics films are deposited on Si by PECVD or by metal sputtering and ex-situ oxidation in N@sub 2@O. After deposition the dielectrics are permitted to react with ambient H@sub 2@O and CO@sub 2@ for extended periods and their stability is monitored as a function of time using FTIR. We find that group III (Y and La) based-films are generally susceptible to reactions with H@sub 2@O and CO@sub 2@ forming hydride and carbonate species. For PVD La films, the oxidation temperature affects the film stability significantly. Films oxidized at 600°C show signs of reaction within minutes of air exposure while films oxidized at 900°C are stable for exposures up to two weeks. Y@sub 2@O@sub 3@ CVD films deposited at 400°C also show high reactivity with H@sub 2@O. Post deposition inert anneals at 900°C in N@sub 2@ improves the film stability significantly. In-situ capping of the Y@sub 2@O@sub 3@ films with 500Å of a-Si reduces greatly the amount of OH detected in the films. Group IV (Hf and Zr) based film exhibit superior stability as compared to the group III films, however. Carbonate formation is verified for both HfO@sub 2@ and ZrO@sub 2@ films. OH is practically undetectable in the films even after ambient exposure for six months. The effect of the OH incorporation on the interface stability will be discussed, and examples of OH promoted reactions between the dielectric film and the Si substrate or polysilicon gate metal will be presented.

4:00pm **DI-MoA7 Growth, Characterization and Thermal Stability of High-K Gate Stacks*, E.L. Garfunkel,*** *T. Gustafsson, D.G. Starodub, S. Sayan, L.V. Goncharova, D. Vanderbilt, X. Zhao, R.A. Bartynski,* Rutgers University*; T. Nishimura,* Murai Project, Japan*; Y.J. Chabal,* Rutgers University **INVITED**

We describe recent results using medium energy ion scattering (MEIS), soft x-ray photoemission (SXPS), inverse photoemission (IPES), electron microscopy (TEM), infrared spectroscopy (FTIR), electrical methods and first-principles calculations to examine high-K gate dielectrics and their interfaces with silicon and metal layers. MEIS has proven extremely helpful in presenting accurate elemental depth profiles of high-K films on Si, Ge and GaAs, especially related to the problem of interface composition. Our isotopic labeling results give new insight on oxygen incorporation and diffusion in high-K films. In selecting an alternative (to SiO2) gate insulators, many parameters in addition to dielectric constant and thermal stability must be considered, including the barrier heights for tunneling. Our SXPS and IPES experimental results are complemented by first-principles density functional calculations to study the properties of the different crystalline phases of HfO2 and ZrO2. It is found that the band gap, barrier height and dielectric response of these two materials are phase dependent. The densities of states are calculated and compared to various experimental measurements. The thickness, layered structure, and crystal phase of the as-deposited and annealed films have been studied by diffraction (XRD), x-ray adsorption (XAS), MEIS and TEM. Critical electrical and materials changes occur during post-processing at elevated temperature. We discuss these changes, including the decomposition of the films in reducing environments in the 900-1100Â°C range. Finally, FTIR results on initial surface reactivity and ALD/CVD film growth are presented. The authors would like to acknowledge productive interactions with colleagues at Agere, IBM, NCSU and Stanford. We also acknowledge the SRC/Sematech FEP Center and the NSF for financial support.

4:40pm **DI-MoA9 Hafnium Germanosilicate Thin Films for Gate and Capacitor Dielectric Applications: Thermal Stability Studies***, S. Addepalli,* *P. Sivasubramani, P. Zhao, M.J. Kim, M. El-Bouanani, B.E. Gnade, R.M. Wallace,* University of North Texas

The use of SiO@sub 2@-GeO@sub 2@ mixtures in gate and capacitor dielectric applications is hampered by the inherent thermodynamic instability of germanium oxide. Studies to date have confirmed that germanium oxide is readily converted to elemental germanium.@footnote 1,2@ In sharp contrast, germanium oxide is known to form stable compounds with transition metal oxides such as hafnium oxide (hafnium germanate, HfGeO@sub 4@).@footnote 3@ Thus, the incorporation of hafnium in SiO@sub 2@-GeO@sub 2@ may be expected to enhance the thermal stability of germanium oxide via Hf-O-Ge bond formation. In addition, the introduction of transition metal would simultaneously enhance the capacitance of dielectric thereby permitting a thicker dielectric, which reduces leakage current.@footnote 4@ In this study, the thermal stability and electrical properties of PVD-grown hafnium germanosilicate (HfSiGeO) films on Si(100) substrate were investigated. XPS, RBS, HR-TEM, C-V and I-V results for germanosilicate films after deposition and subsequent annealing treatments will be presented. Our results indicate that the thermal stability of the hafnium germanosilicate films is drastically affected not only by the presence or formation of elemental germanium during annealing, but also by the germanium content in the film. This work is supported by DARPA through SPAWAR Grant No. N66001-00-1-8928, and the Texas Advanced Technology Program. @FootnoteText@ @footnote 1@ W. S. Liu, J .S. Chen, M.-A. Nicolet, V. Arbet-Engels, K. L. Wang, J. Appl. Phys. 72, 4444 (1992), and, Appl. Phys. Lett. 62, 3321 (1993).@footnote 2@ W. S. Liu, M.-A. Nicolet, H.-H. Park, B.-H. Koak, J.-W. Lee, J. Appl. Phys. 78, 2631 (1995). @footnote 3@ P. M. Lambert, Inorg. Chem. 37, 1352 (1998).@footnote 4@ G. D. Wilk, R. M. Wallace and J. M. Anthony, J. Appl. Phys. 89, 5243 (2001).

High-k Gate Dielectrics and Devices Topical Conference
Room 317 - Session DI-TuM

High-k Dielectric Growth and Processing

Moderator: R.L. Opila, University of Delaware

8:20am **DI-TuM1 Effects of Transistor Fabrication Process Conditions on Electrical Characteristics of High-k Gate Dielectrics***, **G. Bersuker**, P. Zeitzoff, G.A. Brown, J. Gutt, N. Moumen, J. Peterson, J. Barnett,* International Sematech*; B.H. Lee,* International Sematech, Korea*; C.H. Lee, S. Gopalan, N. Chaudhary, Y. Kim, C. Young, P.S. Lysaght, H.-J. Li, M. Gardner, R.W. Murto, H.R. Huff,* International Sematech **INVITED**

Comprehensive evaluation of high-k materials for gate dielectric applications requires fabrication of transistor test structures. The complex fabrication process includes several operations employing highly reactive ions, which may potentially affect electrical performance of the high-k materials. It is, therefore, critical from a materials evaluation standpoint to separate intrinsic properties of high-k dielectrics from process-related effects. The latter is the focus of this investigation. In particular, we concentrate on the charging problem associated with high-k materials, which appears to be one of the major factors affecting threshold voltage and mobility in high-k gate dielectric transistors. Our results demonstrate high sensitivity of the high-k films to the transistor fabrication process conditions. It is shown that electrical properties of gate stacks fabricated with a variety of combinations of ALD and MOCVD Hf-based dielectric compositions can be greatly affected by process-induced charges (PIC). PIC caused by negatively charged ions and/or electron trap inducing species may accumulate in the area of the high-k film exposed to various plasma operations during post gate definition processing (such as poly etch, ash/clean and spacer deposition). These contaminants may diffuse under the gate during subsequent high temperature processing and adversely affect device performance. Significant dependence of the electrical characteristics on the process scheme employed for the transistor fabrication complicates the evaluation of the intrinsic properties of the high-k gate dielectrics.

9:00am **DI-TuM3 Characteristics of High-k Gate Dielectric Formed by Oxidation of Sputtered Hf/Zr/Hf Thin Fims on the Si Substrate***, H.-D. Kim, **Y. Roh**, N.-E. Lee, C.-W. Yang,* Sungkyunkwan University, Korea

Recently, high-k gate oxide have been extensively investigated to overcome the problems such as large leakage current caused by the direct tunneling through extremely thin SiO@sub 2@. We previously demonstrated that simple oxidation of sputtered Hf thin films on Si results in HfO@sub 2@HfSi@sub x@O@sub y@ stacked high-k gate oxides simultaneously with excellent physical and electrical properties; negligible hysteresis, excellent EOT value (1.2 nm) and low leakage current (2 X 10@super -3@ A/cm@super 2@ at 1.5 V after compensating the flatband voltage). In this work, we further investigated the characteristics of high-k gate dielectric formed by the oxidation of Hf/Zr/Hf film (1.5 nm) deposited on the Si substrate by a sputtering method. The oxidation and annealing were performed at 500~800 °C for 60~120 min under O@sub 2@ ambient and at 500~900 °C for 30~60 min under N@sub 2@ ambient, respectively, in furnace. To form MOS capacitors, Pd gate was thermally evaporated on the HfO@sub 2@ film using a shadow mask with circular dots. We found that the electrical properties of MOS devices with oxidized Hf/Zr/Hf film are further improved as compared to those obtained after oxidizing single Hf film with same thickness (i.e., 1.5 nm) In addition to the negligible hysteresis, we obtained the EOT value of 1.15 nm and the leakage current density of 4.2 X 10@super -3@ A/cm@super 2@ at -3 V. More importantly, the deterioration of high-k gate oxide caused by high-temperature oxidation and/or annealing processes drastically minimized. For example, even after the 900 °C oxidation of Hf/Zr/Hf film, EOT and leakage current density were 1.37 nm and 2.78 X 10@super -6@ A/cm@super 2@ at -3 V, respectively. We speculate that this improvement is due to the minimization of undesirable SiO@sub 2@ formation between High-k oxide and Si. These results, as well as further investigation of physical properties of the samples using XPS, will be presented at the conference.

9:40am **DI-TuM5 Study of ZrO@sub 2@ Initial Stage Deposition on Si(100) During High Vacuum Chemical Vapor Deposition***, **Z. Song**, R.D. Geil, D.J. Crunkleton, V.L. Wahlig, B.R. Rogers,* Vanderbilt University

ZrO@sub 2@ is a potential high-k material to replace SiO@sub 2@ gate dielectrics in MOSFET devices. Electrical and structural requirements of the gate dielectric dictate that these layers will be significantly less than 10 nm thick. Studies of the initial stages of ZrO@sub 2@ deposition is needed in order to create an abrupt, low defect interface with silicon. In this work, we used atomic force microscopy (AFM), spectroscopic ellipsometry (SE), X-ray photoelectron spectroscopy (XPS), and transmission electron microscopy (TEM) to study the initial deposition behavior of ZrO@sub 2@ films. Films were deposited at pressures of 10@super -5@ to 10@super -4@ Torr and substrate temperatures of 250 to 450 °C. We observed a transition from 3D growth to 2D growth. These results suggest that a deposition temperature greater than 350 °C is needed to form a uniform film.

10:00am **DI-TuM6 Thin Film Growth and Composition Characterization of Hafnium Oxide Grown on Surface Treated Silicon by Atomic Layer Deposition***, **R. Inman**, A. Deshpande, G. Jursich,* American Air Liquide

New materials are needed for future generation of semiconductor devices and hafnium oxide along with silicate and aluminate combinations continue to show promise for meeting stringent demands of the gate dielectric insulator layer in CMOS transistors. In this critical application, film growth needs to be well controlled by process conditions and deposition requires high level of conformality as layer thickness extends below 100 nm dimension and more complex gate geometries are proposed. To best serve these requirements, atomic layer deposition is an ideal method of growing such films. In this work, thin films of hafnium oxide were deposited on Si(100) substrates by means of atomic layer deposition (ALD) technique using tetrakis(diethylamino)hafnium precursor. The resulting composition and purity of these films were determined at different substrate temperatures using x-ray and Fourier Transform Infrared (FTIR) spectroscopies. FTIR studies confirmed that the resulting films are relatively free of carbon contamination and provided a measure of hydroxyl groups in the film. The kinetics of film growth was also investigated by measuring film thickness as a function of substrate temperature and reagent pulsing characteristics. The thickness measurements indicated a relatively mild inverse temperature dependence of film growth in the range of 250 - 350 C. The cycle number dependence of film growth was examined at both high and low cycle number in order to infer the nucleation growth of the film. These results will be presented using Si substrates with different surface treatments.

10:20am **DI-TuM7 The Effect of Hf Content in Liquid Precursor on the Properties of Mist Deposited Ultra-Thin Films of HfSiO@sub 4@***, **K. Chang**, K. Shanmugasundaram,* The Pennsylvania State University*; D.-O. Lee, P. Roman, P. Mumbauer,* Primaxx Inc.*; J.R. Ruzyllo,* The Pennsylvania State University

Ultra-thin (<10nm) films of hafnium silicate formed by mist deposition method for gate dielectric application in advanced MOS devices were investigated. Precursors with Hf:Si ratio of 0.103:1, 0.276:1, and 1:1 were prepared to investigate the effect of Hf content on mist deposition process and film characteristics. MOS capacitors were fabricated for electrical characterization using Pt gate electrode. The Hf composition in the HfSiO@sub 4@ film was analyzed with angle-resolved X-ray photoelectron spectroscopy. The 1:1 precursor resulted in 12.6 at.% of Hf in the film and 7.5 at.% of Hf was obtained in the HfSiO@sub 4@ film deposited with 0.103:1 precursor. Deposition rate of HfSiO@sub 4@ linearly increases with the Hf content in the precursor even though the Hf composition in the film didn't scale in the same order. Despite the difference in Hf content of the precursor, an interfacial oxide 2.2nm ~ 3.0nm thick was always detected by transmission electron microscopy. Through electrical characterization, it was determined that the obtained gate stacks feature an equivalent oxide thickness of 0.8nm ~ 1.5nm depending on the process. It is postulated that the lower EOT is caused by Hf diffusion from HfSiO@sub 4@ film during thermal treatment step and lower EOT of the interfacial layer. For lower EOT of the interfacial oxide, higher Hf content in the precursor is needed. Using 1:1 precursor, EOT 1.5nm HfSiO@sub 4@ thin film is deposited with leakage current density of less than 1×10@super -2@ A/cm@super 2@.

10:40am **DI-TuM8 The Effect of Surface Preparation and Post Growth Annealing on the Thickness and Composition of High-k Layers Grown on Silicon***, T. Conard,* IMEC, Belgium*; R.K. Champaneria, P. Mack,* Thermo Electron, UK*; R.G. Vitchev,* Facultes Universitaires Notre-Dame De La Paix (FUNDP), Belgium*; R.G. White, **J. Wolstenholme**,* Thermo Electron, UK

The move to high-k materials for gate dielectrics brings with it a new set of parameters that require characterisation. As with silicon dioxide, the thickness of the layer must be measured but, in addition, the thickness of any intermediate layer must be measured also. The chemistry of the intermediate layer is likely to affect the electrical properties of the layer and therefore needs to be understood along with the factors that affect this chemistry. XPS has an information depth that is similar to the thickness of the layers and, therefore, can be used to characterise them. If the information depth is controlled by varying the photoelectron emission angle (angle resolved XPS or ARXPS) more information becomes available. Thickness of surface and subsurface layers can be measured with accuracy and precision. The chemical state of each component of the material can also be determined and the distribution of chemical states within the layer can be measured. Since no material is removed during the measurements, ARXPS can be regarded as a non-destructive technique. This technique has been used to analyse HfO2 and Al2O3 layers on silicon prepared by ALD or MOCVD. A comparison will be made of the layers grown on relatively thick (up to ~1 nm) silicon oxide with those grown on thin oxide layers and on layers containing nitrided SiO2. It will be shown how XPS and ARXPS can determine the effect of the preparative method on the thickness of the layers and the chemical states of the component materials. The results will be presented in the context of those on the same materials from other techniques.

11:00am **DI-TuM9 Si and Ge Surface Functionalization Characterized by In Situ and Ex Situ Infrared Spectroscopy**, *M.M. Frank,* IBM T.J. Watson Research Center and Rutgers University*; M.-T. Ho, S. Dörmann, C.-L. Hsueh,* Rutgers University*; L.J. Webb, N.S. Lewis,* California Institute of Technology*; S. Rivillon,* Rutgers University*; O. Pluchery,* Université Paris 6, France*;* ***Y.J. Chabal****,* Rutgers University

Chemical functionalization and passivation of semiconductor surfaces is often necessary to foster uniform nucleation and high-quality interface formation in the deposition of ultrathin high-@kappa@ gate dielectrics and organic films. To understand the formation of such monolayers in wet, gaseous, or ultra-high vacuum environments, it is desirable to monitor surface reactions in situ. Utilizing infrared absorption spectroscopy, we have achieved such in situ monitoring with submonolayer sensitivity. We have performed both in situ and ex situ studies to gain mechanistic insight into surface chemical reactions on HF-etched, mostly H-terminated Si and Ge surfaces. Chemical species studied include: Cl, supplied via gas phase and wet chemistry, enabling subsequent activation of the Si substrate through hydroxylation; trimethylaluminum (Al(CH@sub 3@)@sub 3@) and other metal organic precursors, to initiate homogeneous atomic layer deposition or chemical vapor deposition of high-@kappa@ gate dielectrics (Al@sub 2@O@sub 3@ and HfO@sub 2@) onto hydrogen-terminated Si; and alkyl groups from wet chemistry, to passivate the Si. In particular, we shed light on the reactivity of Si-CH@sub 3@ and metal-CH@sub 3@ species formed in reactions with organic high-@kappa@ precursors and in wet chemical passivation. On Ge, we are investigating hydrogen passivation in HF using in situ methods, as well as the oxidation of such passivated surfaces. We compare and contrast the passivation and oxidation mechanisms on Si and Ge substrates.

11:20am **DI-TuM10 Plasma Deposition of RuO@sub2@ on HfO@sub2@ for Gate Electrode Applications***,* ***D.B. Terry****, J.M. Doub, G.N. Parsons,* North Carolina State University

Ruthenium-based metals are potential candidates for gate electrodes in advanced gate stack applications. The detailed structure of the interface between high-k dielectrics and the gate metal will be important to maintain low equivalent oxide thickness, but the effect of metal deposition on the high-k/metal interface structure is not known. We have deposited RuO@sub2@ metal from Tris-tetramethyl-heptadianato Ru (Ru TMHD) introduced downstream from a remote N@sub2@O plasma at 365 and 500°C, and examined the deposited film and interface structure using Auger and X-ray photoelectron spectroscopies. The growth rate at 500°C is approximately twice that at 365°, and films show some evidence for N and C incorporation, consistent with the 250°C decomposition temperature of the Ru TMHD. Based on AES results, the O/Ru ratio is larger for the films deposited at higher temperature. Because of the difference between the oxidizing and reducing environments in CVD processing, we expect that metallic oxides such as RuO@sub2@ will result in different metal/dielectric interface structure than for elemental metal/dielectric interfaces. To examine the role of deposition chemistry on interface structure, several thicknesses of RuO@sub2@ have been deposited by plasma CVD on HfO@sub2@ formed in our lab by atomic layer deposition. The effect of HfO@sub2@ surface structure, and the trends in RuO@sub2@ composition with film thickness determined using AES and XPS will be presented and discussed.

11:40am **DI-TuM11 Novel Ultra-thin TiAlO@sub x@ Alloy Oxide for New Generation of Gate Dielectric***,* ***W. Fan,*** Northwestern University*; S. Saha, B. Kabius, J.M. Miller, J.A. Carlisle, O. Auciello,* Argonne National Laboratory*; S.Y. Li, V.P. Dravid, R.P.H. Chang,* Northwestern University*; C. Lopes, E.A. Irene,* University of North Carolina, Chapel Hill

A novel TiAlO@sub x@ alloy oxide has been developed and studied as an alternative gate oxide material for CMOS devices (patent pending). Ultra-thin TiAl (3:1) films with physical thickness 3-20 nm were grown on n-Si (100) by sputter deposition. In-situ oxidation was then performed by using both molecular oxygen (P=1.0x10@super -3@ Torr) and atomic oxygen sources (P=1.0x10@super -4@ Torr). The formed TiAlO@sub x@ exhibits amorphous structure on Si, as revealed by XRD and TEM analyses. In-situ XPS study shows that a full oxidation of TiAl can be achieved at 500@super o@C using both oxygen sources. However, the TiAlO@sub x@ layer formed through atomic oxygen annealing presented a leakage current 150 times lower than the one with molecular oxygen annealing. Since both Ti and Al have more negative oxide formation energies than Si, the presence of Ti and Al at the interface with Si significantly reduces the formation of interfacial SiO@sub x@. It has been confirmed by XPS depth profile, ellipsometry and cross-sectional TEM, which revealed ~1 nm SiO@sub x@ layer formed at the oxide/semiconductor interface with 500@super o@C oxidation. The amorphous TiAlO@sub x@ layer with equivalent oxide thickness (EOT) of 1.7 nm and negligible hysteresis was obtained via atomic oxygen exposure at 500@super o@C, exhibiting high permittivity (~30) and low leakage current density (1.2x10@super -2@ A/cm@super 2@). After post deposition annealing with top gate electrode in place, the leakage was further improved and reached 5.4x10@super -5@ A/cm@super 2@. Furthermore, extended study shows that a full transition of TiAl to TiAlO@sub x@ can be accomplished at room temperature by exposure to atomic oxygen beam. Interfacial SiO@sub x@ formation, therefore, was completely eliminated and TiAlO@sub x@ layer with EOT less than 1 nm was achieved on Si. @FootnoteText@*This work was supported by the U.S. Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.@.

High-k Gate Dielectrics and Devices Topical Conference
Room 317 - Session DI-TuA

High-k Dielectric Characterization

Moderator: E.L. Garfunkel, Rutgers University

2:40pm **DI-TuA3 Invited Paper*, E. Cartier*,** IBM T.J. Watson Research Center **INVITED**

3:20pm **DI-TuA5 Enhanced Tunneling in Symmetric Stacked Gate Dielectrics with Ultra-thin HfO@sub 2@ Layers (0.5-10. nm) Sandwiched between Thicker SiO@sub 2@ Layers (1.5 nm)*, C.L. Hinkle*,** *C. Fulton, G. Lucovsky, R.J. Nemanich,* North Carolina State University

A novel method for obtaining the tunneling mass, m@sub eff@, and conduction band offset energy with respect to Si, E@sub B@, for high-k gate dielectrics is presented. It is based on a quantum mechanical WKB-approximation that explains large bias dependent increases in tunneling in symmetric stacked devices with ultra-thin HfO@sub 2@ layers (~0.5 nm) sandwiched between thicker SiO@sub 2@ layers (~1.0-1.5 nm) as compared with reference devices with homogenous SiO@sub 2@ dielectrics. J-V traces for substrate injection indicate a marked departure from the approximately exponential bias dependence of homogenous dielectrics for V@sub ox@ = V@sub g@ - V@sub fb@ >1 V. This correlates with differences between the tunneling attenuation factors, @alpha@@sub i@t@sub i@ = 4@pi@t@sub i@(2m@sub effi@E@sub Bi@)@super 0.5@/h, in the constituent layers, i, where t@sub i@ is the i@super th@ layer thickness. For V@sub ox@ >1 eV, small decreases in @alpha@t(SiO@sub 2@) compared to larger decreases in @alpha@t(HfO@sub 2@) result in a marked increase in their ratio. For V@sub ox@ > 1.5 V, there is minimal attenuation in the HfO@sub 2@ layer, so that the tunneling current is determined predominantly by the SiO@sub 2@ layer. At V@sub ox@ = 3V, the relative current with respect to the reference Si device is >1000. By analyzing these data, and increasing the thickness of the HfO@sub 2@ layer beyond 2 nm to determine the thickness at which relative tunneling begins to decrease due to increased attenuation in that component of the stack, values of m@sub eff@ = 0.15±0.05 m@sub o@ and E@sub B@ = 1.4±0.2 eV are obtained for HfO@sub 2@.

3:40pm **DI-TuA6 Observation of Bulk HfO@sub 2@ Defects by Spectroscopic Ellipsometry*, H. Takeuchi,*** *D. Ha, T.-J. King,* University of California at Berkeley

HfO@sub 2@ (hafnium oxide) is a promising candidate to replace SiO@sub 2@-based films as the gate dielectric in ultra-scaled MOSFETs, due to its thermal stability in contact with Si, compatibility with a conventional CMOS process flow, and moderately high dielectric constant (20-25). The electrical characteristics of HfO@sub 2@ films, such as equivalent SiO@sub 2@ thickness (EOT), leakage current density, hysteresis in capacitance vs. voltage curves, fixed charge density and resultant field-effect carrier mobilities, have been extensively investigated. However, the physical mechanism for deviation from ideal behavior is not yet well understood. In particular, not much is known about bulk defects inside HfO@sub 2@ and their impact on electrical characteristics and the thermal stability of HfO@sub 2@. In this study, we report a bulk defect in HfO@sub 2@ which can be detected as an optical absorption peak by spectroscopic ellipsometry (SE). 12.5nm-thick HfO@sub 2@ films were formed by oxidation of pure Hf films in a cold-wall rapid thermal annealing (RTA) reactor. Absorption coefficients near the absorption edge were extracted by the data inversion method, in which the optical constants for short wavelength were calculated using the thickness obtained from long wavelength data. The obtained optical bandgap of 5.7eV matches very well with theoretical calculation and VUV measurement reported by other groups, and a shift due to crystallization was also detected. In addition, an extra absorption peak was observed in 4.5~5.0eV range. The energy difference between this absorption peak and the bandgap corresponds well to the trap energy extracted from measurement of the temperature dependence of Poole-Frenkel current. Hence, the peak is associated with electron transition from the valance band to the trap energy level inside the bandgap. This peak reduces with oxidation annealing time, indicating that the defects can be attributed to oxygen vacancies in the HfO@sub 2@ film.

4:00pm **DI-TuA7 Chemically Abrupt Interfaces between Lanthanum Aluminate and Silicon for Alternative Gate Dielectric Applications*, L.F. Edge,*** *D.G. Schlom,* Pennsylvania State University*; S.A. Chambers,* Pacific Northwest National Laboratory*; C.L. Hinkle, G. Lucovsky,* North Carolina State University

LaAlO@sub 3@ is one of the most promising alternative gate dielectrics for the replacement of SiO@sub 2@ in silicon MOSFETs. Single crystalline LaAlO@sub 3@ is known to have a dielectric constant of 24 and an optical bandgap of 5.6 eV. The band offsets between LaAlO@sub 3@ and Si have been predicted to be in the range 2.1 to 3.5 eV for electrons and 1.0 to 1.9 eV for holes. It will be shown that LaAlO@sub 3@ is stable in contact with silicon under standard MOSFET processing conditions. Epitaxial Si has been grown by MBE on single crystals of LaAlO@sub 3@ and annealed at 1026C, which is a standard implant activation anneal for MOSFETs, and the interface remained stable and free of SiO@sub 2@. A major challenge in the growth of alternative gate dielectrics on Si is the formation of unwanted SiO@sub 2@ at the interface. One technique to prevent the formation of SiO@sub 2@ is to grow in a low temperature and excess oxidant regime. We have investigated the oxidation kinetics of Al and La, both individually and together (codeposition), to determine the minimum oxygen partial pressure required to achieve fully oxidized LaAlO@sub 3@. Using these optimized conditions, amorphous LaAlO@sub3@ films as thin as 1.0 nm have been grown on silicon by MBE. AES and XPS analyses indicate that the films are fully oxidized and show no SiO@sub 2@ at the interface, even after prolonged exposure of the films to air.

4:20pm **DI-TuA8 Medium Energy Ion Scattering Studies of the Structure and Composition of Epitaxial SrTiO@sub 3@ Films on Silicon*, L.V. Goncharova*,** *D.G. Starodub, E.L. Garfunkel, T. Gustafsson,* Rutgers University*; D.G. Schlom,* Pennsylvania State University

Thin crystalline oxide films on silicon show a wide range of new electronic, optical, and magnetic properties with potential impact on novel devices. Precision control of the composition, stoichiometry and structure of such films and the ability to characterize the films and their interfaces are therefore of central importance. We have used high-resolution medium energy (~ 100 keV) ion scattering (MEIS) to investigate the composition and structure as a function of depth of thin (40-250 Å) crystalline SrTiO@sub 3@ films on Si (100). As ion beams are penetrating, and the ion-solid interaction is well understood, this technique allows us to get quantitative information both about the film/vacuum and about the film/substrate interface structure. Different channeling and blocking geometries have been utilized to distinguish epitaxial/amorphous regions, to characterize the chemical composition of the SrTiO@sub 3@/Si interface and also to give information about structural parameters. Thin SrTiO@sub 3@ films were grown epitaxially on Si(001) at the low temperatures in an excess of oxygen.@footnote 1@ Our MEIS results show that films grown by this method have A-site (SrO) termination. We further show that submonolayer amounts of strontium silicide, used in the initial stages of growth, are fully eliminated from the interface after growth is completed and that instead Ti has diffused into the interface region. The SrTiO@sub 3@/Si interface was confirmed to be crystalline; however the geometrical structure deviates significantly both from the 'bulk' epitaxial film and from the substrate. Possible structural models for the transition region and mechanisms of titanium incorporation in the interface region will be discussed. @FootnoteText@ @footnote 1@ J. Lettieri, J.H. Haeni, and D.G. Schlom, J.Vac.Sci.Technol. A 20 (2002) 1332.

4:40pm **DI-TuA9 In-situ and Ex-situ Characterization of Barium Strontium Titanate Thin Films on Thermal SiO@sub 2@/Si Substrates*, N.A. Suvorova*,** *C.M. Lopez,* University of North Carolina, Chapel Hill*; A.A. Suvorova, M. Saunders,* University of Western Australia*; E.A. Irene,* University of North Carolina, Chapel Hill

Alternative materials with high dielectric constant (k) are in demand for replacement of SiO2 in MOSFET devices. Barium strontium titanate (BST) is one of possible candidate for DRAM applications. The most important requirement for the incorporation of an alternative gate dielectric is to maintain a high quality interface with Si comparable to that of SiO2 /Si. Similar to other high k materials for BST this is a major problem due to interface reaction with Si. One potential solution is the use of a thermal SiO2 ultra thin underlayer, which helps to minimize the reaction between high k dielectric and Si as well as maintain the high interface quality. However this solution degrades the k values of the two film gate stack. The present study is aimed toward optimizing the SiO2 underlayer thickness in order to maintain the interface quality yet minimize the effect on k. The results from this optimization study are presented with emphasis on the key process parameters that improve the dielectric film stack. For in-situ growth characterization of BST film grown on thermally oxidized Si substrates spectroscopic ellipsometry has been used. Studies of material properties have been complemented with analytical electron microscopy. Electrical characterization has been employed for ex-situ studies of Pt/BST/SiO2/Si structures. From conductance-voltage analysis, the interface trap density Dit was observed to significantly decrease for the capacitors grown on oxidized Si substrates and annealed in forming gas.

5:00pm **DI-TuA10 Band Offsets at Ba- SrTiO@sub 3@ / Si Interfaces***, F. Amy*, *A. Wan, A. Kahn,* Princeton University

The continuous drive toward faster electronics and scaling down of MOSFET device dimensions requires alternatives to SiO@sub 2@ for gate dielectrics. High-k dielectrics have therefore received considerable attention from industry and the scientific community. Crystalline perovstike oxides such as SrTiO@sub 3@ and BaTiO@sub 3@ are of special interest and offer several advantages. First, they can be MBE-grown lattice-matched to Si (or Ge) substrates with very low interface state density.@footnote 1@ Second, they can serve as a buffer layer for the growth of semiconductors, opening possibilities for integrating Si electronics and III-V optoelectronics. However, several issues concerning these materials remain to be fully addressed, among which band offsets with Si and other semiconductors. In this work, we use a SrTiO@sub 3@(100 Å)/BaSrO(11 Å)/Si structure grown by MBE, and X-ray and UV photoemission spectroscopy to study core levels and valence band respectively. Depending on surface preparation, including ex-situ UV ozone, O@sub 2@ or UHV annealing, the valence band maximum position shifts by more than 2 eV, whereas very little if any shift is observed on core levels. These findings indicate that surface composition and morphology are of paramount importance in the UPS determination of electronic structure, and may explain discrepancies between results reported in the literature. Our investigation of clean and stoichiometric SrTiO@sub 3@ surface indicates that its conduction band minimum is located 0.4 eV (± 0.4) below the one of silicon. An in-depth investigation of the role of surface preparation is being pursued, and results on BaTiO@sub 3@/SrTiO@sub 3@/Si samples will be reported. @FootnoteText@ @footnote 1@ . R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. 293, 468 (2001)

High-k Gate Dielectrics and Devices Topical Conference
Room Hall A-C - Session DI-TuP

Poster Session

DI-TuP1 Investigation of Initial Growth Stage of HfO@sub 2@ Films on Si (100) Grown by Atomic-layer Deposition using In-situ Medium Energy Ion Scattering, ***H.S. Chang***, *H. Hwang,* Kwangju Institute of Science and Technology (KJIST), South Korea; *M.-H. Cho, Y.J. Cho, K.J. Kim, D.W. Moon,* Korean Research Institute of Standards and Science (KRISS), South Korea

The initial growth stage of HfO@sub 2@ films on p-type Si(100) grown by atomic-layer deposition (ALD) was investigated using in-situ medium energy ion scattering (MEIS). The interaction between adsorbed HfCl@sub 4@ molecules and Si substrate was examined in relation to the film thickness, substrate temperatures, and surface states of the Si substrates. Interfacial reaction between Hf and Si at the initial growth stage was occurred and significantly depended on the surface state of the Si. The hafnium silicate with an amorphous structure was grown on the oxidized Si substrate at an initial growth stage. In particular, the interfacial layer thickness and the stoichiometry of the layer were depended on the surface state of Si substrate. As thickness of the film increased, the silicate formation was gradually changed into HfO@sub 2@ state. The physical analysis of the films with XPS and TEM also supported the interfacial reactions. Based on the interfacial interaction at the initial growth stage, we suggested the model for the interaction between Hf and Si at the initial growth stage in relation to the atomic size, bonding characteristics, and formation energy. This study will be helpful to understand the interfacial reactions at the initial growth stage and to control the reactions for the application of high-k dielectrics.

DI-TuP2 Effects of Annealing Temperature on the Characteristics of HfO@sub 2@/HfSi@sub x@O@sub y@ High-k Gate Oxides, ***H.-D. Kim***, *Y. Roh, D. Jung, N.-E. Lee,* Sungkyunkwan University, Korea

Several candidates for the future high-k gate oxides have been extensively studied by many research groups to overcome the problems such as large leakage current caused by the direct tunneling through extremely thin SiO@sub 2@. Recently, we reported that simple oxidation of sputtered Hf films on Si produces HfO@sub 2@/HfSi@sub x@O@sub y@ high-k oxides with excellent properties. We argued that the effective k of HfO@sub 2@/HfSi@sub x@O@sub y@ film may be controlled by changing the thickness ratio between HfO@sub 2@ and HfSi@sub x@O@sub y@. In this work, we further investigated the characteristics of HfO@sub 2@/HfSi@sub x@O@sub y@ high-k gate oxides to clarify the roles of annealing process. The 1.5 nm Hf film was directly deposited on Si substrate by sputtering at plasma power of 50 W for 4 min. Oxidation was performed at 500 °C for 60 min, followed by annealing at 500-900 °C in furnace under N@sub 2@ ambient. Pd gate metal was thermally evaporated on the HfO@sub 2@ film. Using the physical and electrical measurement techniques, we confirmed that the oxidation of the thin Hf films on Si results in the HfO@sub 2@/HfSi@sub x@O@sub y@ stack layer with the excellent electrical properties; negligible hysteresis, excellent EOT value (1.2 nm) and low leakage current (~2 X 10@super -3@ A/cm@super 2@ at 1.5 V after compensating V@sub fb@). Furthermore, we found that the level of leakage current decreases as annealing temperature increases. However, over 500 °C, annealing deteriorates the EOT value; e.g., 1.2 and 1.7 nm EOT values were obtained from 500 and 900 °C samples, respectively. We speculate that both thickness increase of HfO@sub 2@/HfSi@sub x@O@sub y@ films and the formation of additional SiO@sub 2@ layer between HfSi@sub x@O@sub y@ and Si cause these phenomena. We therefore suggest that annealing temperature must be carefully controlled to maintain the excellent characteristics of HfO@sub 2@/HfSi@sub x@O@sub y@ high-k gate oxides.

DI-TuP3 Thermal Stability of Al- and Zr- doped HfO@sub 2@ Thin Films by DC Magnetron Sputtering, ***Y.E. Hong***, *Y.S. Kim, D.H. Ko, D.W. Lee,* Yonsei University, South Korea; *J.-H. Ku,* Samsung Electronics, South Korea

Currently, high-k materials are under consideration as replacements for SiO@sub 2@ because physically thick film with high dielectric constant is possible solution for reducing leakage current. Among some metal oxides such as Al@sub 2@O@sub 3@, ZrO@sub 2@, and HfO@sub 2@, particularly HfO@sub 2@ exhibits excellent material properties such as high permittivity of up to 30, energy gap of 5.6eV and thermal stability in contact with silicon. However, after post-deposition annealing above 400°C, as-deposited amorphous HfO@sub 2@ crystallizes which may induce grain boundary leakage current. In addition, annealing in an oxygen rich ambient leads to fast diffusion of oxygen through the HfO@sub 2@, resulting in the growth of uncontrollable interfacial layer between HfO@sub 2@ and silicon substrate. In this study, we investigated comparatively the thermal stability properties of HfO@sub 2@ based films with Al- and Zr-doping. HfO@sub 2@ was prepared by sputtering Hf target in a mixture of oxygen and argon at room temperature. Al- and Zr-doping is achieved by co-sputtering using Al and Zr target. And the compositions of the doped films were controlled by target power. After the formation of the films, annealing at 500~900°C for 5min by furnace in N@sub 2@ ambient was followed. The compositions and the chemical states of the oxide films were confirmed by RBS and XPS. The crystallization temperature of the HfO@sub 2@ film which has 10% Al was 900°C. However, most of the Zr-doped HfO@sub 2@ films were crystallized from as deposited condition. As an annealing temperature increases, HRTEM analyses of the all doped films show the increased interfacial layer thickness, and the interfacial layer of the Zr-doped HfO@sub 2@ films is thicker than the Al-doped. The increased CET and leakage current values through CV/IV measurements and dielectric constant difference between Al- and Hf-doped HfO@sub 2@ films will be presented and discussed.

DI-TuP5 NH@sub 3@ Nitridation Effect on HfO@sub 2@-Al@sub 2@O@sub 3@ Films in the MOS Capacitor, ***C. Lee***, *J. Choi, M. Cho, C.S. Hwang, H.J. Kim,* Seoul National University, Korea

High-k gate dielectrics, such as HfO@sub 2@ and Al@sub 2@O@sub 3@, have been investigated as an alternative to SiO@sub 2@ for low power device due to high dielectric constant, thermodynamic compatibility of the interface with Si substrate, and a relatively large band gap. We investigated the nitrogen diffusion behavior and electrical characteristics, especially flat band voltage (V@sub fb@) shift and V@sub fb@ hysteresis by NH@sub 3@ nitridation of the MOS capacitors. The nitrided MOS capacitors include the various high-k gate dielectric stacks such as Pt gate/HfO@sub 2@/p-type Si, Pt gate/HfO@sub 2@-Al@sub 2@O@sub 3@/p-type Si, and Pt gate/capping Al@sub 2@O@sub 3@-HfO@sub 2@-Al@sub 2@O@sub 3@/p-type Si. HfO@sub 2@ and Al@sub 2@O@sub 3@ films were deposited on p-type epitaxial Si (100) wafers with a resistivity of 1 @ohm@cm by atomic layer deposition (ALD) technique using HfCl@sub 4@, Al(CH@sub 3@)@sub 3@ and H@sub 2@O at 300°C after RCA SC1 and HF cleaning. Post deposition annealing (PDA) of the samples was performed with rapid thermal annealing (RTA) at 700°C, 800°C, and 900°C in NH@sub 3@ for 30 seconds. Post-metallization annealing (PMA) of Pt-top electrodes was performed at 400°C for 30 min. under a 5% H@sub 2@ + 95% N@sub 2@ atmosphere. V@sub fb@ shifted negatively with increasing nitridation temperature, but it moved positively with increasing Al@sub 2@O@sub 3@ thickness. HfO@sub 2@-Al@sub 2@O@sub 3@ film showed excellent V@sub fb@ shift and hysteresis characteristics when it was post-metallization annealed in NH@sub 3@ at 800°C for 30 seconds. NH@sub 3@ nitridation effect on Pt gate/HfO@sub 2@-Al@sub 2@O@sub 3@/p-type Si MOS capacitors with increasing PDA temperature was analyzed by electrical evaluation, Auger Electron Spectroscopy (AES), atomic force microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM).

DI-TuP6 Structural and Electrical Characterization of Aluminum Oxynitride Thin Films Obtained by RF-Sputtering, ***J.J. Araiza***, UAZ, Mexico; *M.A. Aguilar,* CICATA-IPN, Mexico, Spain; *C. Falcony, M. Jergel,* CINVESTAV-IPN, Mexico

The structural and electrical characteristics of aluminum oxynitride thin films deposited on silicon substrates by rf-sputtering are reported. The properties of the films were studied as a function of the deposition parameters, such as substrate temperature, RF sputtering power and the relative amount of argon and nitrogen gases introduced to the chamber. The films were characterized by atomic force microscopy, transmission and scanning electron microscopy, X ray diffraction, Infrared and Uv-vis spectroscopy and ellipsometry. Metal-Oxide-Semiconductors structures were also fabricated with the films deposited. Films with characteristics close to aluminum oxide and aluminum nitride were obtained, depending on the deposition parameters. It was found that the films can withstand electric fields up to 4.5 MV/cm, without observing destructive breakdown, with dielectric constants up to 8.7. In addition, the as deposited films present a surface roughness lower than 1.6 nm, refractive indexes from 1.5 to 2.0 and deposition rates up to 7.0 nm/min.

DI-TuP7 Plasma and Thermal Etching of High-k Materials for ALD Chamber Cleaning, *B. Ji*, ***D. Wu***, *R.M. Pearlstein, S.A. Motika, E.J. Karwacki, M.J. Plishka,* Air Products and Chemicals, Inc.

High dielectric constant (high-k) materials such as Al@sub 2@O@sub 3@, HfO@sub 2@, and ZrO@sub 2@ are deposited onto semiconductor wafer surfaces by atomic layer deposition (ALD) in integrated circuits manufacturing. High-k ALD reactors must undergo periodic chamber cleaning to remove deposition residues from the internal surfaces of the reactor in order to maintain production yield. Due to their high chemical inertness and extremely low volatility, etching and cleaning high-k deposition residues has been technically challenging. By combining thermochemical calculations and experimental screening, we have identified BCl@sub 3@ as the most effective reagent for removing high-k materials from ALD chambers. We will report both plasma and thermal etching of Al@sub 2@O@sub 3@, HfO@sub 2@, and ZrO@sub 2@ using BCl@sub 3@. We will discuss the chemical mechanism of BCl@sub 3@-metal oxide reaction, and the influence of various process parameters on high-k materials etch rate.

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