Plasma Science and Technology
Room 315 - Session PS-MoM

Critical Dimension Etching

Moderator: K. Seaward, Agilent Laboratories

8:20am **PS-MoM1 Not Quite 50 Years of Plasma Etching**, ***R.A. Gottscho***[1], Lam Research Corp. **INVITED**

Since the advent of plasma etching in the manufacturing of semiconductor devices in the 1970s, both industry and technology have changed dramatically. In the '70s, integrated device manufacturers (IDMs) dominated the industry. IDMs built systems by starting with "sand" and using equipment of their own design and fabrication. For example, hexode etchers were created by Bell Labs, the Reinberg reactor came from Texas Instruments, and electrostatic chucks came from IBM. Today, IDMs buy plasma processing equipment with processes developed, at least partly, by the equipment companies. Fabless companies have sprouted and grown ubiquitous as foundries have become a dominant source of chip supply. In the early '80s, debates raged over the relative merits of single wafer processing for 4-6" wafers. Today, batch etchers cannot be found in the fab despite their inherent throughput advantages. Single wafer processing of 12" wafers with unprecedented control is the norm. Now, we see the advent of integrated metrology and even more advanced process control. Over this time period, gate lengths have shrunk from >1 um to

9:00am **PS-MoM3 Chemical Topography Analyses of Photoresist Patterns Exposed to HBr/O2 and Cl2/O2 Trimming Plasma Processes**, ***E. Pargon***, *O. Joubert, L. Vallier,* CNRS/LTM, France; *S. Xu,* Applied Materials

Nowadays, a way to bypass the lithography limitation in typical gate etch processes is to introduce a step of "resist trimming" prior all the other classical etch steps. Resist trimming induces a lateral erosion of the photoresist mask to reach a range of dimension smaller than the resolution of the lithography. To better understand the mechanisms involved in this process, an experimental procedure based on XPS has been developed to determine the chemical composition and thickness of the reactive layers formed both on top and sidewalls of the resist features during the process. The processes are performed in a high density plasma source (ICP) and two trim chemistries are investigated: HBr/O@sub2@ and Cl@sub2@/O@sub2@. The XPS analyses show that the transformations occurring on the resist sidewalls can well explain the faster trim rate obtained with a HBr/O@sub2@ chemistry. Indeed, the XPS results reveal that HBr/O@sub2@ is a very reactive chemistry leading to the formation of very thin (0.5 @nm@) reactive layers on the resist sidewalls, while when using Cl@sub2@/O@sub2@, there is a competition for the adsorption sites between atomic Chlorine and Oxygen leading in this case to thick (1.5 @nm@) carbon rich chlorine reactive layers on the resist sidewalls. Other plasma parameters (pressure, bias and source powers) have also been studied and we have obtained good correlations between the trim rate and the modifications measured by XPS on the resist sidewalls. In most cases, with the Cl@sub2@/O@sub2@ chemistry, a decrease in trim rate is well correlated with an increase in reactive layer thickness on the resist sidewalls and with a decrease of the O/Cl ratio in the reactive layer. Finally, this XPS experimental procedure enables us to better understand the mechanisms involved in resist triming processes and to determine the key plasma parameters that drive such processes.

9:20am **PS-MoM4 Aspect Ratio Dependent Etching in the Si-Treatment Process of the Source and Drain Area of sub 90 nm Devices**, ***K.H. Bai***, *M.C. Kim, B.Y. Nam, K.K. Chi, C.J. Kang, W.S. Han, J.T. Moon,* Samsung Electronics Co., Korea

As feature dimension shrinks down to nano scale of sub 90 nm, the aspect ratio increases up to more than 10 even at the source/drain area of the self-aligned contact (SAC) sturcture of the DRAM devices. The small open areas of the contact holes for the sub 90 nm devices require enough Si-treatment at the source/drain area to get a reliable contact resistance. However, usually the low-biased etching condition of the soft etch plasma has severe aspect ratio dependent etching (ARDE) phenomena, leading a lot of Si3N4 loss at the shoulder of SAC sturcture. To overcome the severe ARDE in the high aspect ratio structure, we investigated the ratio of radical to ion flux at the top and bottom surface of the contact holes. Because the low bias of the soft etching condition, the radicals collide to the side wall surface multiple times before reaching the hole bottom. Therefore, the radical flux at the bottom of the hole is affected by the sticking coefficient controlled by the surface temperature. However, another important key factor controlling the ARDE is the radical density in the plasma. We found that the surface coverage of the contact hole is greater than 1, the temperature becomes a less important factor in controlling the ARDE. In this work, we investigated the ARDE of our Si-treating plasma in our sub 90 nm scale devices as functions of the radical density and temperature, finding a condition nearly free from ARDE. As a result, the loss of Si3N4 at the shoulder of the gate electrode was reduced by 70%, also improving contact resistances at the source/drain more than 10%.

9:40am **PS-MoM5 Loading Effect Study on Cl@sub 2@+HBr Plasma Etching of Polysilicon**, ***W. Jin***, *H.H. Sawin,* Massachusetts Institute of Technology

The effect of etching product buildup, i.e. loading effect, in an inductively coupled plasma etcher for polysilicon etching with Cl@sub 2@+HBr chemistry is studied. In addition to the depletion of reactants, etching products can be fragmented upon collision with energetic electrons into various Si-containing species, with subsequent deposition on the substrate and chamber walls. The role of Si-containing species on the plasma-surface interaction has to be included in the surface kinetic model database for the simulation of etching process. This work uses real plasma beam/QCM to measure the etching yield under different ion bombardment energy and temperatures, and adds SiCl@sub 4@ in Cl@sub 2@/HBr feed gas to mimic the effect of Si-loading observed in a real ICP etcher. The study indicates that the Si-loading can reduce the etching yield significantly, due to the ion-enhanced deposition of Si-containing species on the substrate. The effect of etching yield reduction is more pronounced at lower Si-loading. The plasma beam composition was measured with a mass spectrometer as a function of feed gas composition and Si-loading. The reduction of etching yield at different Si-loading can be explained by the relative concentration of Si, SiCl and SiCl@sub 2@ species at different Si-loading. The surface composition was measured with X-ray photoelectron spectroscopy after etching. The surface composition does not show significant change with Si-loading. A surface kinetics model was developed to relate the etching yield to the beam composition, ion energy and substrate temperature. The insensitivity of surface composition to the Si-loading can also be explained by this model.

10:00am **PS-MoM6 Pattern Deformations during Resist Trimming Process and its Suppression by He-diluted O@sub 2@/SO@sub 2@ Chemistry**, ***H. Morioka***, *M. Tajima, M. Terahara, M. Nakaishi, I. Hanyu,* Fujitsu Limited, Japan

In addition to CD control, accuracy of pattern transcription in resist trimming and gate etching process, what is called pattern fidelity, has become more important with scaling of ULSI devices. Various pattern deformations during resist trimming, such as line-end shortening, often become serious obstacles to high-density device integration because they narrow the alignment margin and prevent the scaling of design rule. We measured line width reduction (amount of trimming) and the line-end shortening during trimming and gate etching process. Experiments were performed on an ICP etcher. O@sub 2@-base chemistry was used to "trim" resist patterns. The gate stack consisted of 1nm gate oxide, 100nm Poly-Si, and 30nm SiO@sub 2@, which was coated by organic BARC and patterned by ArF lithography. We found that the line-end shortening was larger than the line width reduction, and this disparity increased with increasing trimming time, which was accompanied by pattern deformations in specific patterns, such as L-shape corner. This pattern dependent resist erosion can be related to excessive etchant flux in the convex area. In order to suppress these disparity and pattern deformation, we investigated He/O@sub 2@/SO@sub 2@ chemistry, in which SO@sub 2@ was a source of lateral etching inhibitor that is mild to ArF resist, and oxygen was main etchant of trimming. He-dilution was used to control the trimming rate and suppress condensation of sulfur compounds. Optimizing etchant/inhibitor ratio by means of O@sub 2@/SO@sub 2@ ratio, we have succeeded in reducing line-end shortening and suppressing pattern deformations for trimming of sub-100nm resist patterns. In optimized conditions, trimming amount was almost the same as line-end shortening, and proximity effect (dense-iso differnce) of trimming was smaller than 5nm. Therefore we have fabricated 25nm gate poly-Si patterns by He/O@sub 2@/SO@sub 2@ trimming (from 80nm to 25nm) and conventional poly-Si gate etching process.

10:20am **PS-MoM7 On the Roughness of Etched Silicon**, ***A.A.E. Stevens***, *H.C.W. Beijerinck,* Eindhoven University of Technology, The Netherlands

The smaller the etched features, the more important the roughness of the etched feature surface becomes. Not only for integrated circuits, but also

[1] **AVS 50th Anniversary Invited Speaker**

for, e.g., photonic crystals, the surface roughness might limit the device quality. By using in situ (spectroscopic) ellipsometry and mass spectrometry, the effect of Ar@super +@ ions and XeF@sub 2@ etch precursor on the etch mechanism has been studied, simultaneously collecting information regarding the roughness evolution. Analysis of the XeF@sub 2@ reactivity and SiF@sub x@ products in contrast to the reaction layer composition shows that the reaction layer thickness, i.e. the surface fluorine content, scales with the roughness. This implies, that the SiF@sub x@ layer build up suggested in literature can be explained by the increasing roughness of the surface, thus the effective surface area increase of the etched Si samples. Furthermore, the etched Si samples have been analyzed with an AFM for comparison with the in situ ellipsometry results. The same trends in roughness evolution have been observed for the ellipsometry measurements and the AFM measurements, corroborating the used ellipsometry models. To learn about the role of the etch precursor and ions in the roughening of the surface during etching, the Family-Vicsek scaling theory of the surface roughness has been applied. The scaling coëfficients @alpha@ and @beta@, representing lateral correlations on the surface and time dependent roughness evolution, respectively, have been derived from the AFM data analysis. Since specific @alpha@ and @beta@ values are related to the surface processes occurring during the etching, the application of the scaling theory aids in understanding the role of the ions and etch precursor in the roughening process.

10:40am **PS-MoM8 Investigation of Trim Etching Process for Formation of Si/High-K Gate Stack**, ***K.M. Tan***, National University of Singapore; *W.J. Yoo,* National University of Singapore, Singapore; *L. Chan,* Chartered Semiconductor Manufacturing, Singapore

In recent years, a photoresist trimming technique based on the current 248nm and 193nm lithography technology are being developed to achieve smaller gates. In this work, we investigated the trimming technique to directly apply to the etching of the Si/SiO@sub 2@ and Si/HfO@sub 2@ gate stacks to further reduce the gate length. The trimming process developed using an industry standard ICP etcher consists of a main etch step followed by a trimming step using HBr, SF@sub 6@ and Cl@sub 2@. When HBr and SF@sub 6@ were used, a Si layer was trimmed at the rate of 17nm per minute at a pressure of 80mTorr, a bias power of 60W and an inductive power of 400W. A higher trim rate was obtained by using a higher inductive power and also by replacing HBr with Cl@sub 2@. However, the use of Cl@sub 2@ resulted in the decrease of the selectivity of Si to the underlying SiO@sub 2@, and thus reduced the maximum allowable trimming time. The trimming rate varied with pressure with an initial increase from 40mTorr to 70mTorr and a subsequent decrease from 70mTorr to 80mTorr. According to the results obtained for all the etch conditions used, HfO@sub 2@ produced a much slower etch rate than SiO@sub 2@ regardless of whether Cl@sub 2@ or HBr was used, and this resulted in a higher etch selectivity of Si to the underlying dielectric. As a result, a longer trimming time was allowed for HfO@sub 2@ than SiO@sub 2@. It was interesting to find out that an etching profile after the trimming step could be more anisotropic than that before the trimming step. Further studies are in progress to obtain 65nm trimmed gate structures from 130nm patterns using the 193nm photolithography technology.

11:00am **PS-MoM9 50nm Gate Electrode Patterning using a Neutral Beam Etching System**, ***S. Noda***, *S. Samukawa,* Tohoku University, Japan; *H. Nishimori, T. Ida, T. Arikado,* Semiconductor Leading Edge Technologies, Inc. (Selete), Japan; *K. Ichiki,* Ebara Research Co., Ltd., Japan

The increased packing density of ultra large-scale-integrated circuits (ULSI) requires ultra thin dielectric films that have low leakage current and are extremely reliable in metal-oxide-silicon (MOS) devices. High-k dielectrics films have been identified as leading candidates to replace conventional SiO@sub 2@ gate dielectrics in future ultra large-scale integrated circuits. However, the high-k films are more fragile and defective materials in comparison with the SiO@sub 2@-based thin films. As a result, the process-induced damages are very serious problems, such as charge-build-damages, changes in film quality and generation of defects by the irradiation of charged particles (ions and electrons) and VUV photons during the plasma etching processes. To break-through these problems, we developed a high-efficiency neutral beam etching system using negative ions generated in the pulse-time-modulated inductively coupled plasma (TM-ICP).@footnote 1@ In this system, high-density (1-4mA/cm@super 2@) and low-energy (10-100eV) neutral beams are effectively extracted from the pulsed plasma. It is expected that the neutral beam etching is promising candidate for the damage-free high-k gate electrode patterning. In this paper, we evaluated characteristics of the poly-Si gate etching using fluorine (SF@sub 6@) and chlorine (Cl@sub 2@) based gas chemistries. Highly anisotropic 50nm poly-Si etching profiles could be obtained with no degradation of extremely fine resist patterns in the case of the chlorine based neutral beams. The electrical properties of MOS capacitors will also be presented in comparison with the results in the conventional plasma etching systems. @FootnoteText@ @footnote 1@ S. Samukawa, K. Sakamoto and K. Ichiki, J. Vac. Sci. Technol. A20, 1566 (2002).

11:20am **PS-MoM10 Surface and Reactor Dynamics Governing Photoresist Trim and Organic BARC Open Plasma Processing**, ***D.J. Cooperberg***, Lam Research Corporation; *S. Johnston, D. Horak,* IBM Microelectronics; *V. Vahedi,* Lam Research Corporation

Photoresist trimming is employed to obtain acceptable feature profiles in sub-130nm linewidths. For logic applications, the process offers a means of shrinking gate length to values that are smaller than can be printed directly with a chosen lithographic technology. When organic bottom anti-reflective coatings (O-BARC) are used to assist photolithography the photoresist trimming can be performed before, during, or after an in-situ O-BARC opening process. The trimmed PR and opened O-BARC are used as a mask for either a hardmask open or a gate etch process. In this talk we will present process trends for O@sub 2@/CF@sub 4@/N@sub 2@ photoresist trim and O-BARC open plasma processing. We have measured the effect of several reactor settings as well as wafer topology on vertical and trim (lateral) etch rates. Reactor settings studied include inductively coupled power, bias power, gas mixture, and electrode temperature. In addition, the effects of variations in exposed area, local pattern density, and microloading or aspect ratio have been studied. It will be shown that local pattern density gradients over a length scale @>=@ the gas mean free path can effect etch uniformity. Trim rates are measured during the O-BARC open process and the trim process separately. It will be shown that the dependence of trim rate on aspect ratio changes dramatically during these two steps. Our experiments are used to identify the appropriate semi-empirical models for the surface kinetics and intra-feature transport which govern feature scale profile evolution. Additionally our experiments can be used to partially characterize reactor dynamics and the transport of the primary etchant, O atoms.

11:40am **PS-MoM11 3-Dimensional Modeling of Pulsed Inductively Coupled Plasmas: A Method to Improve Uniformity@footnote 1@**, ***P. Subramonium***, *M.J. Kushner,* University of Illinois at Urbana-Champaign

Continuous wave (CW) operation of inductively coupled plasma (ICP) reactors having asymmetric pump ports or feedstock gas injection may produce asymmetric densities of radicals and fluxes to the substrate. These asymmetries are often intensified by positive feedback between regions of higher conductivity producing higher power deposition and higher ionization rates, which in turn increase the conductivity. Pulsed ICPs have been investigated as a means to extract negative ions to the substrate to reduce charging damage. Pulsed ICPs may also provide a means to reduce or eliminate asymmetries by reducing this positive feedback. In this paper, results from a 3-dimensional model for pulsed ICPs having such asymmetries will be discussed. As these long-term phenomena are difficult to resolve in multi-dimensional plasma equipment models a computationally parallel hybrid model has been developed to both speed the calculation and to better represent the physical processes. Results for pulsed ICPs in Ar, Ar/Cl@sub 2@, Ar/C@sub 2@F@sub 6@ gas mixtures will be discussed while varying pulse repetition frequency (5 - 20 kHz), duty cycle (10% - 70%), power (200 - 800 W) and pressure (5 - 20 mTorr). We found that the non-uniformities in species densities which feedback through the plasma conductivity are generally reduced during the afterglow of the pulsed plasma. In the afterglow, without the nonuniform source function, diffusion smooths the plasma density profile, providing a more uniform set of initial conditions for the next power pulse. The ionization source during the subsequent power pulses is therefore more uniform. As a result, time averaged plasma properties for pulsed plasmas are more uniform compared to CW excitation. Uniformity generally improves with decreasing duty cycle and decreasing repetition rate. @FootnoteText@ @footnote 1@ Work supported by Semiconductor Research Corporation and National Science Foundation.

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