Plasma Science and Technology
Room 315 - Session PS+MM-MoA

MEMS Etching
Moderator: F.G. Celii

2:00pm **PS+MM-MoA1 Understanding Deep Silicon Etching: Mechanisms for Formation and Removal of Sidewall Passivation**, ***M.L. Steen,*** IBM T.J. Watson Research Center*; T.J. Dalton,* IBM Semiconductor Research and Development Center*; C.K. Tsang, R.W. Nunes, J. Vichiconti, E.A. Sullivan, B.N. To, D. Barrett,* IBM T.J. Watson Research Center

One of the interesting aspects of deep silicon etching is the diversity of process requirements. In addition to high throughput, many applications have added demands on profile shape and surface morphology. Supporting such applications hinges on rational control of sidewall passivation. Two fluorine-based methods are used to achieve high silicon etch rates, each with its own variation of sidewall passivation. Most widely used is time-multiplexed deep etching (TMDE), wherein the etching and passivating cycles are performed sequentially. Sidewall passivation is accomplished via polymer deposition at room temperature. Alternately, a second method involves cryogenic cooling of the wafer to reduce lateral etching. However, problematic to both of these processes, the thickness of the sidewall-passivating layer is not uniform with etch depth. In cryogenic etching, the blocking layer is very thin, thereby making it difficult to maintain a consistent thickness over the entire etch depth. In TMDE, the thickness of the polymer covering decreases rapidly at greater depths and lateral etching increases there to form an undesirable bowed or barreled etch profile. This is particularly problematic for applications that have tight specifications for sidewall structure. Our goal is to understand the role the passivating layer plays in the formation of sidewall structure. Toward this goal, a number of process variables were explored using a commercial, inductively-coupled plasma etcher. We report a method that tailors the shape of the profile through better control of the formation and subsequent removal of the passivating layer. A significant increase in the silicon etching rate, minimization of mask undercut, and substantial reduction in bowing will be discussed. Overall, our method demonstrates enhanced process performance and flexibility to meet a broad range of needs in deep silicon etching.

2:20pm **PS+MM-MoA2 Improvement of Anisotropy and Aspect Ratio of a Pattern Etched in Bosch Process by using a Faraday Cage**, ***J.-H. Min,*** *G.-R. Lee, J.-K. Lee, S.H. Moon,* Seoul National University, Korea*; C.-K. Kim,* Ajou University, Korea

Bosch process, which consists of sequentially alternating etch and deposition steps using SF@sub 6@ and C@sub 4@F@sub 8@ plasmas, has been widely used for deep silicon etching in the fabrication of MEMS due to its advantages for obtaining patterns of high aspect ratio and anisotropy. Because the opening sizes of many MEMS structures are considerably large (about 1~100 μm), the electric field at the convex corner of a micro feature is locally distorted such that ions travel inside the etched pattern with a broad angular distribution. As a result, the flux of ions incident on the bottom surface is decreased with an increase in the etch depth, which eventually limits the maximum aspect ratio obtained in Bosch process. This limiting factor cannot be overcome by optimizing process variables. In this study, a Faraday cage, defined as a box made of conductor walls, was used to overcome this limitation. In the Faraday cage system, ions enter perpendicular to the sheath formed along the top grid plane of the cage and travel inside the cage maintaining the initial incident direction because electric potential in the cage is unaffected by outside voltages and therefore is the same throughout. Accordingly, the trajectory of ions, which has a narrow angular distribution determined by the grid pitch of and the sheath thickness on the top plane, is not changed at the convex corner of the micro feature or inside the pattern located in the cage. It was confirmed by an ion angular-energy distribution analyzer that the angular distribution of ions entering the pin hole of 10-μm-diameter, which is the same as the size of pattern opening, is narrower in the cage system than in the case of no cage. As a result, the aspect ratio and the anisotropy of the etched pattern were improved by using a Faraday cage in Bosch process.

2:40pm **PS+MM-MoA3 Exploring Microdischarges for Manufacturing and Sensing Applications**, ***Y. Gianchandani,*** University of Michigan **INVITED**

The increasing diversity of applications in microsystems for sensing and actuation motivates a significant amount of research in lithography-based fabrication techniques. The general goals for these processes include the facilitation of structural complexity and material diversity, amongst others. This talk will address how microplasmas (which are ignited between co-planar or stacked thin film metal electrodes patterned on a single wafer surface) can facilitate certain types of structural complexity by permitting materials such as Si to be etched in unique ways; and how micro-arcs (which are ignited between a micromachined electrode array and planar workpiece) can facilitate material diversity by permitting stainless steel and other metals to be micromachined for devices such as cardiac stents. Beyond manufacturing issues, the ability to predict and control microdischarges permits them to be exploited in transduction schemes. Spectroscopic sensing of chemicals in both gas and liquid phase is an obvious application. For example, microdischarges to liquid microchannels have been used to detect inorganic contaminants such as lead and chrome in water. However, the converse application, which is the use of liquids to serve as inexpensive but tunable sources for radiation wavelengths that are otherwise not easy to generate, may also offer value. These issues will be addressed as well.

3:20pm **PS+MM-MoA5 Feature Scale Model of Etching High Aspect Ratio Structures in Silicon using SF@sub 6@/O@sub 2@ Plasma**, ***J. Belen,*** *S. Gomez,* University of California, Santa Barbara*; M.W. Kiehlbauch, D.J. Cooperberg,* Lam Research Corporation*; E.S. Aydil,* University of California, Santa Barbara

The need to etch high aspect ratio features (depth-to-width) such as deep holes and trenches in Si arises in manufacturing of microelectromechanical systems and capacitors in memory devices. Anisotropic plasma etching of such features is achieved by taking advantage of energetic ion bombardment of the surface in the normal direction in conjunction with sidewall passivation with a film that is resistant to etching. Feature profile evolves as a result of various ion-assisted etching, passivation and deposition processes that occur on the feature surfaces. A fundamental and quantitative understanding of the balance between these processes is necessary for achieving control over the feature profile shape. We have developed a semi-empirical feature scale model of Si etching in an SF@sub 6@/O@sub 2@ plasma. This model is used to quantify etching kinetics and to identify the important parameters that affect profile evolution. Information from plasma diagnostics and previously published data are used to estimate F, O, and ion fluxes as well as ion energy and angular distributions. These estimates are used as input to the profile simulations in order to reduce the degrees of freedom in the model. Experimentally inaccessible parameters such as the spontaneous chemical etch rate constant, F and O sticking coefficients, ion-enhanced etch yield and ion scattering parameters are determined by matching the experimentally observed and simulated feature profiles under different plasma etching conditions. The mask undercut and the slope of the feature sidewalls are controlled by the F-to-O flux ratio. Two distinct mechanisms for sidewall passivation are identified: (a) surface oxidation, which is thought to be prevalent at high and intermediate F-to-O ratios where the sidewalls are either negatively tapered (bowed out) or vertical, and (b) redeposition of reaction products, which results in positively tapered sidewalls at low F-to-O ratios.

3:40pm **PS+MM-MoA6 Etching of High Aspect Ratio Structures in Si using SF@sub 6@/O@sub 2@ Plasmas**, ***S. Gomez,*** *J. Belen,* University of California, Santa Barbara*; M.W. Kiehlbauch,* Lam Research Corporation*; E.S. Aydil,* University of California, Santa Barbara

Plasma etching of high aspect ratio (depth-to-width) structures in Si is a crucial step in manufacturing trench capacitors for memory devices, and integrated components for microelectromechanical systems (MEMS). We have investigated etching of deep features (~10 μm) with high aspect ratios (~50) using plasmas maintained in mixtures of SF@sub 6@ and O@sub 2@ gases. The etching experiments were conducted in a low pressure (5-80 mTorr), high density, inductively coupled plasma etching reactor with a planar coil to maintain the discharge and with radio frequency (rf) biasing of the substrate electrode to achieve independent control of the ion flux and ion energies. Specifically, we have studied the effects of pressure, rf-bias voltage and SF@sub 6@-to-O@sub 2@ gas ratio on the etch rate, feature profile and selectivity using Si wafers patterned with 0.5-0.35 μm diameter holes in a SiO@sub 2@ mask. Visualization of the profiles using SEM is complimented by plasma diagnostics such as optical emission spectroscopy in conjunction with actinometry and mass spectrometry to understand the key factors that control the anisotropy, selectivity and etch rate. Oxygen ionization and dissociation products (O and O@super +@) oxidize the feature sidewalls and help achieve anisotropic etching through the sidewall passivation mechanism. F-to-ion flux ratio and F-to-O flux ratio are found to be the important internal plasma parameters that determine

the etch rate and anisotropy. The mask undercut and the slope of the sidewalls is determined by the F-to-O ratio in the plasma. Increasing the SF@sub 6@-to-O@sub 2@ ratio in the feed gas increases F-to-O ratio and makes mask undercutting worse because passivation by O atoms cannot keep up with chemical etching by F atoms. As F-to-O ratio is decreased, effective sidewall passivation by O atoms results in nearly vertical sidewalls. Further reduction in F-to-O ratio results in sidewalls that slope inwards towards the bottom of the feature.

4:00pm **PS+MM-MoA7 Via Drilling on Silicon Wafers using the Cryogenic Process**, ***T. Tillocher***, *A. Basillais, X. Mellhaoui, P. Lefaucheux,* GREMI, France*; M. Boufnichel,* ST Microelectronics*; R. Dussart, P. Ranson,* GREMI, France

Plasma etching has an important place in microelectronics and microsystems industries. Some techniques, especially Bosch and cryogenic processes, enable the realization of high aspect ratio structures. The Bosch process is widely used in spite of scalloped profiles whereas the cryogenic process is quicker and presents smooth etched surfaces. Via (12 µm in diameter) drilling on silicon wafers is achieved by cryogenic etching in an industrial ICP reactor (Alcatel 601E). A SF6/O2 plasma is created and expands toward a polarized and cooled silicon wafer. Plasma parameters are optimised so as to obtain vias with an anisotropic profile with a high etch rate. End to end vias were performed with an average etch rate about 7µm/min by etching separately the two sides of the wafer. Yet, all of them did not meet right in the middle of the plate as it should be and their shape is not reproducible in the whole wafer. This seems to be due to a non enough homogeneous cooling system. Moreover, some defects, such as bowing and undercut lead to an increase of the final diameter of the via and hence must be limited. A process including a soft etching step, an over-passivating step, and a standard etching step leads to a significant reduction of these defects. O2/SF6 ratio is adjusted in the two first steps. Additionally, it was shown that bias voltage has a strong influence on the profiles : its increase is not synonym of a deeper etching but a slightly greater volume etched. Crystal orientation dependent etching also appeared at lower temperatures and particularly in the direction what can explain negative slopes in this cases.

4:20pm **PS+MM-MoA8 Si, SiO@sub 2@ Feature Etching for MEMS Fabrication: A Combined Simulator Coupling Local Transport, Surface Etch, and Profile Evolution Models**, ***G. Kokkoris***, *C. Boukouras, A. Tserepi,* National Center for Scientific Research (NCSR) "Demokritos", Greece*; A.G. Boudouvis,* National Technical University of Athens (NTUA), Greece*; E. Gogolides,* National Center for Scientific Research (NCSR) "Demokritos", Greece

Profile control during feature etching is a central requirement in the manufacturing processes of microelectromechanical systems (MEMS) or microelectronics devices. Simulation of the feature profile evolution can contribute to this challenge. The purpose of this work is a complete simulator for feature etching. The goal is to predict the effect of the bulk plasma phase to the feature profile, and is accomplished through the coupling of the following component modules: 1) a local transport model: local fluxes of neutrals and ions inside features are calculated taking into account shadowing and re-emission phenomena.@footnote 1@ 2) a surface etch model: local etch rates at each elementary surface of the structure are calculated through site balances. Si, SiO@sub 2@ substrate etching models under fluorine or fluorocarbon plasmas have already been developed.@footnote 2@ 3) a profile evolution algorithm: the level set method@footnote 3@ is fed with the local etch rates and moves the feature profile. The complete simulator can be used to a) validate suggested surface models through comparison with experimental data, b) investigate and explain the influence of feature size and surface morphology on etch rates (e.g. reactive ion etching lag phenomenon@footnote 4@, effect of roughness on etch rates) and c) simulate and optimize processes such as the BOSCH process@footnote 5@ for the etching of high aspect ratio Si structures, where pulsed alternating flows of SF@sub 6@ and C@sub 4@F@sub 8@ gases are used. @FootnoteText@ @footnote 1@V. K. Singh, E. S. G. Shaqfeh, and J. P. McVittie, J. Vac. Sci. Technol. B 10, 1091 (1992).@footnote 2@E. Gogolides, P. Vauvert, G. Kokkoris, G. Turban, A. G. Boudouvis, J. Appl. Phys. 88, 5570 (2000).@footnote 3@J. A. Sethian, J. Comp. Phys. 169, 503 (2001).@footnote 4@G. Kokkoris, E. Gogolides, A. G. Boudouvis, J. Appl. Phys. 91, 2697 (2002).@footnote 5@F. Larmer, A. Schilp, German Patent DE 4241045.

4:40pm **PS+MM-MoA9 In-Situ On-wafer Monitoring for Charge Build-up Voltage during Plasma Process**, ***T. Shimmura***, *S. Soda, M. Koyanagi, K. Hane, S. Samukawa,* Tohoku University, Japan

High-aspect-ratio SiO@sub 2@ contact hole etching is one of the key processes in the fabrication of ULSI devices. However, charge accumulation in contact holes during etching is one of the main causes of serious problems, such as charge-build-up damage, etching-stop, and microloading effects. Therefore, it is very important for realization of the next generation semiconductor devices to understand the mechanism of such electric charge accumulation and to be in control of plasma processes. As a result of our previous research, it was clear that deposited fluorocarbon film in contact holes shows high electric conductivity by ion irradiation.@footnote 1@ This paper reports on in-situ on-wafer monitoring for the build up charging potential during plasma processes. We were developed the device used for measuring charging potential. This device consists of Poly-Si(300 nm)/SiO2(1.7 µmm)/Poly-Si(300 nm) stacked layer structure. The contact hole of 300 nm diameter is formed to top Poly-Si layer and SiO@sub 2@ layer, and the numbers of holes were 6,400,000. The potential of top and bottom Poly-Si electrode were measured during plasma exposure with/without deposited fluorocarbon film. The potential difference between top and bottom Poly-Si electrode without the deposited fluorocarbon film is about 70 volts. On the other hand, in the case that the deposited fluorocarbon film exists on sidewall, the potential difference between top and bottom electrode was hardly observed. This result shows that the sidewall deposited fluorocarbon film has high electric conductivity and mitigates the electric charge accumulation at the contact hole bottom during SiO@sub 2@ etching processes. @FootnoteText@ @footnote 1@ T. Shimmura, S. Soda, S. Samukawa, M. Koyanagi and K. Hane, J. Vac. Sci. Technol. B, 20 2346 (2002).

5:00pm **PS+MM-MoA10 Plasma Etching of Chromium as a Hard Mask for a Complex Metal Stack Etch**, ***D. Cruz***, UCLA/Sandia National Laboratories*; M.G. Blain,* Sandia National Laboratories*; J.P. Chang,* University of California, Los Angeles

We have investigated the etching of chromium in an inductively coupled plasma (ICP) reactor and its etching selectivity to Al and SiO@sub 2@. Chromium is being utilized as a hard mask in etching a three-layer aluminum/silicon dioxide metal stack to form a self-aligned structure of 4µm in depth. The stack comprises the basis for a micro-cylindrical ion trap mass analyzer. The chromium etching chemistry was chlorine based, with the addition of He, Ar, and O@sub 2@. The Cr samples, approximately 2500 Å thick, were e-beam evaporated on two and three layers of Al/SiO@sub 2@ stacks. Chemical vapor deposited silicon dioxide was used as a hard mask to pattern Cr into 2-micron sized features. The selectivity of chromium to silicon dioxide during the He/Cl@sub 2@/Ar/O@sub 2@ chromium etch was 15:1. During the main chromium etch, the etch rate was determined to be approximately 1500 Å/min, at a pressure of 10 mTorr and 250 V DC bias. The He/Cl@sub 2@/Ar/O@sub 2@ discharge provided a fast etch rate with no plasma induced damage. Once the chromium was patterned, the Al/SiO@sub 2@ stack was exposed to an ICP Al etch, utilizing a Cl@sub 2@/BCl@sub 3@ based plasma chemistry, followed by an ICP SiO@sub 2@ etch, utilizing SF@sub 6@/Ar/N@sub 2@/O@sub 2@. These two chemistries were used alternatively until all layers of the stack were etched through in a self-aligned fashion. The etch rate ratios of Al and SiO@sub 2@ to chromium were 70:1 and 25:1, respectively. The overall final stack etch totaled about 22 minutes. No grassing or sputtering was noted on the sample, however profile control of the Al layer is an issue due to the lack of a sidewall forming polymer source. Chromium seems to be a promising hard mask, having high selectivity to the ICP Al etch and ICP SiO@sub 2@ etch. @FootnoteText@ Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

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