Manufacturing Science and Technology
Room 309 - Session MS-TuM

Packaging and Role of Interface Engineering in IC Processing

Moderator: L. Larson, SEMATECH

8:20am **MS-TuM1 Challenges and Advances in Packaging Technology Development for IC Processing*, H. Hosack,*** Semiconductor Research Corporation **INVITED**

Traditionally packaging provides isolation of the chip from the environment and a space transformation from the chip bond pads to leads compatible with connections to the outside world. With the recent increases in frequency and power dissipation in high performance microprocessors, and the advent of portable electronics, the requirements for electronic packaging are rapidly expanding not only to continuing increases in performance, but also to radically different functionality in areas such as photonics, RF, and MEMS. These new needs require complete re-thinking of packaging with the view that the die-package is a sub-system in itself, and the need is to produce this complete sub-system with optimized total performance at a minimum cost. The areas of critical importance in this sub-system view will be those areas that address the interface between the die back-end and the package. By eliminating unduly specialized work on either the chip or package in isolation, redundant effort can be minimized and device performance can be optimized. The challenges inherent in optimizing the chip-package interface include the spectrum of electrical issues, thermo-mechanical issues, and metrology. These issues are being addressed by package-chip interface solutions that not only optimize the sub-system in its present configuration but also by novel schemes that employ new materials, new signaling mediums, and reallocation of interface functions between the package and the chip. These new approaches include novel schemes such as incorporating portions of the traditionally on-chip metallization as a part of the package, non-contact chip-to-package signaling, and 3D packaging. This discussion describes the critical issues that must be addressed in this new view of package functions, as well as the status of some of the unique solutions that are being researched to provide the optimized chip-package sub-system.

9:00am **MS-TuM3 Interfacial Engineering for Reliability Improvement of Cu/Low k Interconnects*, P.S. Ho,*** University of Texas **INVITED**

With continuing device scaling, interfaces of dielectrics, metals and semiconductors become increasingly important in controlling the yield and reliability of devices and interconnects. Beyond the current 130 nm technology node, the implementation of low k dielectrics causes serious reliability concerns for Cu interconnects due to their weak thermomechanical properties. This paper will first discuss the role of interfaces in controlling the reliability of the Cu damascene structure, particularly regarding electromigration and stress voiding. Several approaches of interfacial engineering to improve Cu interconnect reliability will be discussed, including surface processing and overcoat layers to reduce mass transport and to increase adhesion strength. Central to these approaches is the optimization of the chemical bonding to improve the properties of interfaces and low k dielectrics. The effects on electromigration and stress voiding of Cu/low k interconnects will be discussed.

9:40am **MS-TuM5 Forming Laminar Cu/Substrate Interfaces: Vacuum vs. Electrochemical Processing***, N.P. Magtoto, J. Liu, J. Lei, X. Zhao,* ***J.A. Kelber,*** University of North Texas **INVITED**

The nucleation and conformal growth of a Cu film on a metal or dielectric barrier substrate is of critical importance for the production of reliable interconnects. This phenomenon has been studied extensively at the vapor/solid interface, where surface science experiments carried out in vacuum or ultrahigh vacuum (UHV) can generally be applied directly to industrial thin film fabrication methods (e.g., sputter deposition). Such studies have demonstrated that the initial growth mode of Cu on various substrates is extremely sensitive to surface chemistry, and this can lead to highly variable results during real world processing. In many cases, including Si:C:H films,@footnote1@ silane-treated Ta,@footnote2@ and sapphire(0001),@footnote3@ initial 2-D growth on a dielectric or air-exposed metal substrate is enhanced by substrate hydroxylation prior to Cu deposition. This has important consequences for designing processes that are insensitive to incidental oxidation. In contrast, the situation at the electrolyte/solid interface is complex, and fundamental issues like the role of ad-atom mobilities or surfactants in film nucleation are not well understood. Kinetic measurements and in-situ STM provide only limited information.. This talk will review the enhancement of Cu 2-D growth at the vapor/solid interface, and discuss recent efforts to identify conformal vs. 3-D growth during electrodeposition, including the prospects for using monolayer concentrations of ad-atoms, such as iodine, to enhance conformal growth in additive-free environments. @FootnoteText@ @footnote1@. M. Pritchett, N. Magtoto, and J. Kelber, Thin Solid Films (in press) @footnote2@. X. Zhao, M. Leavy, N. P. Magtoto and J. A. Kelber , Thin Solid Films 415, 308 (2002) @footnote3@. C. Niu, K. Shepherd, D. Martini, J. Tong and J. A. Kelber, and D. R. Jennison and A. Bogicevic, Surface Science 465, 163 (2000).

10:20am **MS-TuM7 Challenges and Advances in Thin Film Mechanics*, Z. Suo,*** Princeton University **INVITED**

Devices in modern technologies have complex architectures, small feature sizes, and diverse materials. The close proximity of dissimilar materials leads to unusual fracture behaviors. A scientific understanding of these behaviors is significant for the development of the future technology. In particular, rate processes, such as creep, subscritical cracking, and ratcheting, limit the long term reliability of the interconnects. Drawing on recent experiments and models, this talk describes a channel crack in a brittle film on an underlayer. When the underlayer is compliant (e.g., a low k dielectric), the driving force on the channel crack is very large. When the underlayer creeps (e.g., a polymer), the crack velocity is set by the viscosity in the underlayer, as well as by subcritical cracking in the brittle film. When the underlayer is plastically deformable (e.g., a metal), on thermal cycling, the crack can grow in the brittle film by ratcheting deformation in the underlayer. I also discuss the use of these phenomena to measure mechanical properties at the small scale. PDF files of papers are available at http://www.princeton.edu/~suo/ Keywords: Interconnects, fracture, creep, plasticity.

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