Tuesday Afternoon, November 4, 2003

Manufacturing Science and Technology
Room 309 - Session MS-TuA

Directions in Semiconductor Device Scaling for the Next Decade

Moderator: S. Shankar, Intel Corporation

2:00pm **MS-TuA1 The Future of Chip Making Is Different --- Or Is It?**, ***R. Puhakka,*** VLSI Research **INVITED**

During this downturn chip making industry has seen numerous arguments that Moore's Law has to slow down and no one can afford to continue as before. The fab cost is over $3B for leading edge fab, steppers are forecasted to cost more than $30M each, and new materials like copper, Low-K and High-K are creating new failure modes that are not well understood. In essence, the future of chip making is different. Or is it? Data shows that cost per transistor still continues to drop at historical rates. The number of transistors manufactured continues to grow fast, which shows world's appetite for technology. Simultaneously, chip industry continues to shrink the critical dimensions at a very regular rate of node per two years. All of this is more difficult and expensive. This means it's becoming more of a big company game - - a long term trend that's been in place since the eighties. The analysis, however, also shows evidence that long term growth for chips and equipment is fundamentally lower. The future is different, but not as dramatically as has been argued.

2:40pm **MS-TuA3 Technology and Manufacturing Challenges in High Tech**, *R.L. Wisnieff,* IBM Corporation; ***S.M. Rossnagel,*** IBM T.J. Watson Research Center **INVITED**

Semiconductor technology is currently going through a fundamental transition, for the last forty years the active device has been the primary limitation in circuit performance, however today the wiring that interconnects the active devices is rapidly becoming the largest factor in determining the maximum speed the circuit will operate at. The search for high performance interconnects led to the widespread adoption of copper wiring to lower the resistance and, more recently, to the introduction of low dielectric constant materials to lower the capacitance of the interconnect circuit. The research and development of copper wiring spanned a period of roughly 12 years with much of this time was spent in refining the technology to achieve high reliability and yield. The research and development of lower dielectric constant materials is being undertaken at a much faster pace over a period of 5 years materials have been developed and applied to product. This accelerated schedule has left substantial room for improvement in the materials and processes that are being used. It is likely that there will be a series of incremental improvements ultimately culminating in a wiring technology that will use air gaps.

3:20pm **MS-TuA5 The Future of Semiconductor Lithography**, ***W.J. Trybula,*** International SEMATECH **INVITED**

The technology acceleration of the semiconductor industry has placed tremendous pressures on both equipment suppliers and manufacturers. Reviewing the International Technology Roadmap for Semiconductors (ITRS) readily demonstrates this advance in technology through acceleration. By examining the market pressures, an understanding of the forces driving the semiconductor manufacturers can be obtained. The result of these pressures is demonstrated by the Lithographic exposure tools that are currently under development. 193nm tools are being introduced into widespread manufacturing. 157nm lithography is being developed for introduction in late 2005 or early 2006 with production insertion slated for 2007. Extreme UltraViolet (EUV) is also under development for with plans manufacturing insertion in 2009. In addition, Electron Projection Lithography (EPL), Maskless Lithography (MML), and nano-Imprint Lithography are all being pursued. This paper provides an overview of the technologies being developed. Details of each are provided, which encompass the methods of operation, the key drivers for each technology, the mask requirements, the advantages of the technology, and projected insertion timing based on the exposure tool manufacturers' estimates. A summary will be provided that shows the time scale of each of the technologies for insertion. The key challenges for the technologies will highlight the areas of prime consideration. A final table will be provided that estimates the total industry cost to develop the technologies that are under primary consideration for insertion in the next few years.

4:00pm **MS-TuA7 CMOS Scaling Limits and Opportunity for Nanoelectronics**, ***Y. Nishi,*** Stanford University **INVITED**

Moore's Law and the scaling principle have guided IC technology and products development in the past 3.5 decades, which has led us to sub 100nm era today. At the end of each decade IC technology community anticipated some sort of slowing down in the pace of geometry shrink, i.e.; in late 70's it was 1um as the limit of practical scaling, and in late 80's it became 0.1um as the ultimate limit. Now we are discussing 10-20nm as the ultimate limit. In the past cases, a set of technology break through allowed us further scaling, such as stepper technology and later excimer laser technology coupled with rapid thermal processing. At the same time we did not have physics driven limits in small geometry devices in the past, but now it seems there will be fundamental changes in transport phenomena in MOS transistors as geometry shrinks. The question today should be, "Do we have another break through which may bring us to sub-20nm in terms of performance, power consumption, cost and manufacturability?" If the answer is "no", we need to look into other options to partially, if not fully, replace scaled CMOS approach. This talk will cover the trends of CMOS scaling in the past, today and tomorrow, and discuss technical bottle neck and challenges mainly from device physics and technology point of view, followed by looking into several opportunities of nanoelectronic devices such as nanowires, nanotubes from device physics integration point of view.

4:40pm **MS-TuA9 John Bardeen and Transistor Physics**, ***H.R. Huff,*** International SEMATECH **INVITED**

The point contact transistor and the discovery of transistor action by Bardeen and Brattain on Dec 16, 1947,@footnote 1,2@ which evolved from studies on Shockley's field-effect principle, was the first solid-state electronic device to utilize both free-electrons and free-holes and resulted in Bardeen and Brattain receiving a patent on Oct 3, 1950.@footnote 3@ Shockley was not a co-patent holder, however, since his scientific contribution of the field-effect principle had, in retrospect, already been anticipated through a previous patent awarded to Lilienfeld in 1930.@footnote 4@ The assessment as to whether the minority-carrier holes emitted into the large grained polycrystalline, n-type Ge (or Si) sample were mainly transported from the emitter to the collector through the p-type inversion layer@footnote 5@ or exhibited some non-trivial transport as minority-carriers through the n-type bulk sample, continues to be of interest and will be discussed. In that regard, Shive's experiment clearly illustrated the importance of the geometrical configuration in determining the percent of surface versus bulk transport@footnote 6@ while Shockley's p-n (bulk) junction theory and p-n junction transistor, originally an undisclosed notebook account, facilitated the mathematical description of Bardeen and Brattain's previously disclosed transistor action@footnote 1-3@ using a one-dimensional analysis.@footnote 7@ Bardeen also comprehended that it was not efficient to modulate the conductivity of a slab of semiconductor via the field effect@footnote 8@ and, thereby, patented the essence of the first modern (MOS) transistor.@footnote 9@ This was an insulating gate modulating an n-type inversion layer via the field effect, utilizing the inversion layer to confine the minority-carrier transport, in series with a reverse-biased n-p junction, and resulted in the first recorded power gain in a solid-state amplifier.@footnote 9@ The device, described by Sah as a sourceless MOS transistor,@footnote 10@ became the basis of, for example, subsequent MOS memory DRAM and CMOS microprocessor applications. Indeed, John Bardeen, the co-inventor of the bipolar and inventor of the MOS transistor, may rightly be called the father of modern electronics. Nevertheless, Shockley deservedly shared the Noble prize in 1956 with Bardeen and Brattain for his seminal contributions of injection over a barrier, p-n (bulk) junction theory and p-n junction transistor. The scientific background, personnel involved and intertwining of these historic 1940s events are described. @FootnoteText@@footnote 1@J. Bardeen and W.H. Brattain, Phys. Rev., 74, 230-231 (1948) @footnote 2@W.H. Brattain and J. Bardeen, Phys. Rev., 74, 231-232 (1948) @footnote 3@J. Bardeen and W.H. Brattain, U.S. Patent No.2,524,035 (filed June 17, 1948; issued Oct. 3, 1950) @footnote 4@J.E. Lilienfeld, U.S Patent No. 1,745,175 (filed Oct. 8, 1926; issued Jan. 18, 1930) @footnote 5@J. Bardeen, Phys. Rev., 71, 717-727 (1947) @footnote 6@J.N. Shive, Phys. Rev., 75, 689-690 (1949) @footnote 7@W. Shockley, Bell Sys. Tech. J., 28, 435-489 (1949) @footnote 8@W.Shockley and G.L. Pearson, Phys. Rev., 74, 232-233 (1948) @footnote 9@J. Bardeen, U.S. Patent No. 2,524,033 (filed Feb. 26, 1948; issued Oct. 3, 1950) @footnote 10@C.T. Sah, Proc. IEEE, 76, 1280-1326 (1988)

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