Manufacturing Science and Technology
Room 309 - Session MS-MoM

Process and Equipment Integration and Development
Moderator: E.G. Seebauer, University of Illinois at Urbana Champaign

8:40am **MS-MoM2 Development of Low Resistance Copper Thin Films Using a Strain Enhanced Grain Growth Technique**, ***M. Moriyama***, *M. Shimada, H. Masuda, M. Murakami,* Kyoto University, Japan

Copper is attractive as interconnect materials of future Si-ULSI (Ultra-Large Scale Integrated) devices with linewidth of less than 100nm. The advantage of using copper (over conventional Al-alloy) as the interconnect materials is that copper has lower electrical resistivity and higher reliability. However, we have serious concern with resistivity of the ultra-narrow Cu interconnects, because the resistivity of interconnects was observed to increase rapidly by reducing the linewidth of the interconnects. The reason is believed to be due to the relatively long mean free path (~39nm) of the conducting electrons of copper. When the linewidth is less than 100nm, the electron scattering by the surface (or interface) and grain boundary becomes dominant, causing significant increase in the resistivity of the copper interconnects. In order to realize nano-scaled Si-devices, development of low resistance ultra-narrow copper interconnects is essential. The purpose of the present experiment was to explore the possibility to prepare low resistivity copper interconnects, which satisfy the designer's requirement, by determine the primary factor (film thickness or mean grain size) which controls the electrical resistivities of copper films. The film microstructures were observed by atomic force microscopy and scanning ion microscopy. The film resistance was measured by a DC four-point probe method. Our experimental result concluded that the grain boundary scattering primarily increased the resistivity of the Cu thin films, indicating that large grained films were essential for low resistivity ultra-narrow copper interconnects. We succeeded to prepare the copper thin films with giant grains by the strain enhanced grain growth technique. This technique will be promising to develop the low resistance copper interconnects for the future Si-ULSI devices.

9:00am **MS-MoM3 Processing and Characterization of PMSSQ Based Materials for Nanoporous Low-K Dielectrics**, ***P. Lazzeri,*** ITC-IRST, Italy*; J.J. Park, Z. Lin, R.M. Briber,* University of Maryland*; L. Vanzetti, M. Anderle, M. Bersani,* ITC-IRST, Italy*; R.D. Miller,* IBM Almaden Research Center*; G.W. Rubloff,* University of Maryland

Nanoporous low-K dielectrics are an essential component in future interconnect technology. We have investigated the thermal transformations by which nanoporous polymethylsilsesquioxane (PMSSQ)-based low-K dielectrics are formed through spin-casting and curing in a mixture of PMSSQ with a poly(methylmethacrylate-co-dimethylaminoethylmethacrylate) random copolymer (PMMA-co-DMAEMA) as the porogen. ToF-SIMS shows a sequence of PMSSQ fragments which change with curing, as well as the evolution of porogen related species. Over the range 200-450C, both crosslinking to form the SiO@sub 1.5@CH@sub 3@ matrix and decomposition/volatilization of the porogen occur. To understand the influence of PMSSQ precursor chemistry on the final low-K structure, we have compared two precursors with different initial SiOH content. ToF-SIMS shows the crosslinking kinetics to be faster for the high SiOH than for the low SiOH content material. The distribution of the porogen species also varies with the nature of the PMSSQ precursor: XPS reveals substantial surface depletion of porogen for the low SiOH but not for the high SiOH content material, and ToF-SIMS images indicate the formation of large porogen aggregates, but only for the low SiOH material. Thermal desorption mass spectrometry during curing shows the evolution of volatile byproducts, as expected for both the crosslinking reactions and the porogen degradation and desorption. These chemical analysis techniques yield information crucial to understanding the complex chemical and transport phenomena which determine the microscale and nanoscale properties of these nanoporous low-K dielectrics and their role in future interconnect technology.

9:20am **MS-MoM4 Multi-scale Modeling of Chemical Mechanical Planarization**, *L. Jiang, H. Simka, S. Skokov, D. Thakurta,* ***S. Shankar,*** Intel Corp.

A coherent modeling approach is presented for mechanics and transport effects in CMP process. Different regimes of material removal are identified based on first-principle analysis on slurry transport, stress, and slurry flow. Important effects of pad, glazing, conditioning, and polisher design are demonstrated with oxide polish model results. We review multiple-scale model linking with an emphasis on the innovative methods to combine flow and stress analysis from feature to wafer scale. Micron-scale models developed at Intel are presented to illustrate the complexity of particle-level dynamics in CMP and the physical processes involved in patterned wafer planarization.

9:40am **MS-MoM5 Thermal Characterization of Stacked 3D System-in-Package**, *J. Valtanen, J. Miettinen,* ***E.O. Ristolainen,*** Tampere University of Technology, Finland

Electronics development has been driven mainly by IC technology progress. Cell and line width have been continuously shrunk proving development trend called Moore's law. This has created increasing pressure to the first level interconnection. In future, traditional 2-dimensional (2D) packaging will limit product miniaturization. Therefore, components must be also joined to third dimension. A solution to this problem is a stacked System-in-Package (SiP). With this technology, great improvements over 2D packaging are achieved, such as greater packaging density, smaller size, and shorter interconnection length. The next evolution step comes in through following ways: to grind extra sand away from active ICs, to use flexible substrates and interposers. However, this technology has some problems that must be solved. For higher density of 3D package, increased power density brings new challenges to heat management. In this work, a stacked SiP structure has been studied. The package consists of three layers. In every layer, a silicon die of 3.7 mm x 8.3 mm has been joined with flip chip method onto an aramid-epoxy interposer of 6 mm x 10 mm. The silicon chips has been thinned down to 90 µm and the thickness of the interposer is 150 µm. The interposers are joined together using solder covered polymer spheres with diameter of 250 µm. So, the dimensions of whole package are 0.9 mm x 6 mm x 10 mm resulting in the total silicon efficiency of 150 %. Transient thermal responses have been measured by experiments and they are compared with simulations calculated with the FEM program Ansys. A constant heat power has been added to one chip at a time and temperature response has been measured in every chip. In this study, thermal responses, maximum temperatures, and chip-to-chip thermal interactions are achieved. In addition, differences between boundary conditions are discussed and certain design rules for chip placement are given.

10:00am **MS-MoM6 Advanced Clean Process by Supercritical Carbon Dioxide**, ***H.-J. Tu,*** *P. Chuang, C.-Y. Wang, Y.-L. Lin, H. Lo, M.-S. Zhou, M.-S. Liang,* Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan, R.O.C.

As device approaching nano-scale, it is more difficult to extend aqueous-based clean processes to future generations due to its high surface tension characteristics. An advanced clean process by supercritical carbon dioxide (SCCO@sub 2@) becomes a potential enabling technology in semiconductor industries for its specific capabilities of low surface tension, chemical inertness, and more friendly ESH (environment, safety, and health) which can overcome future wafer clean challenges. In the present work, we show that using SCCO@sub 2@ can successfully remove residue/polymer for advanced sub 100 nano-meter copper low-k interconnect fabrication. In addition, it appears that the low-k dielectric film is much less damaged by this novel technology than conventional clean process.

10:20am **MS-MoM7 Two-Gas Reactive Sputtering**, *W.D. Sproul, D.J. Christie,* ***D.C. Carter,*** Advanced Energy Industries, Inc.

Reactive sputtering with two reactive gases and one target material presents special problems. Both reactive gases affect the state of the target surface and the plasma conditions, which means that both affect common feedback control signals such as the cathode voltage and optical emission signals. Modeling has shown that the way to control the two-gas reactive sputtering process is to produce individual control signals for each gas. Experiments have confirmed the model. The reactive sputtering of titanium or silicon in a combined oxygen/nitrogen atmosphere is shown. In this study, individual partial pressure signals for each of the oxygen and nitrogen reactive gases were available from a mass spectrometer. A combination where one of the gases is controlled in the partial pressure mode and the other in a flow mode can lead to unstable operating conditions under certain process conditions. The gas operating in flow control can trap the target in a poisoned state, and the target cannot return to the unpoisoned state until both gases are removed. Both target voltage and mass spectrometer data show the existence of a high partial pressure of the flow controlled reactive gas that traps the target in the poisoned mode even when the partial pressure controlled reactive gas is removed from the system. To have a fully stable process when two reactive

gases are used requires that the partial pressure of each gas be controlled individually. When the individual partial pressures are controlled, the target does not get trapped in a poisoned state, and there is complete freedom to adjust the reactive gas partial pressures to achieve the desired film composition.

10:40am **MS-MoM8 Hydrogen Pressure Dependence of Trench Corner Rounding during Hydrogen Annealing**, ***H. Kuribayashi***, *R. Shimizu,* Fuji Electric Corporate Research and Development, Ltd., Japan*; K. Sudoh, H. Iwasaki,* Osaka University, Japan

Hydrogen annealing has become increasingly important for silicon device processes. Especially for trench gate MOSFETs, both trench corner rounding and sidewall surface smoothing are quite essential for the ruggedness and reliability of gate oxide. Though the evolution of crystal shape through surface self-diffusion during heating in vacuum has been extensively investigated, it has not been sufficiently studied in specific ambients, which are applicable to semiconductor processes. At the preceding meeting we studied shape transformation of silicon trenches with sidewall surface of (110) and (-110) during annealing in hydrogen ambient at 1000°C, and showed that the observed shape transformation can be simulated well with Mullin's continuum surface model@footnote 1@ with surface self-diffusion. In this work, to study the roll of hydrogen gas on the Si surface self-diffusion in more detail, we investigated both the hydrogen pressure dependence and the temperature dependence of the trench corner rounding for wider range of pressure (10-760Torr) and temperature (1000-1100°C), respectively. We found a remarkable effect of hydrogen on trench corner rounding. The curvature of a trench corner for a certain annealing time increases linearly with increasing hydrogen pressure. The diffusion coefficient at 1000°C deduced by the Mullin's formula decreased from 2x10@super 5@nm@super 2@/sec at 100Torr to 3x10@super 3@nm@super 2@/sec at 500Torr, which are much smaller than the one in vacuum@footnote 2@ by three to five orders of magnitude. The diffusion coefficients did not follow the Arrhenius relations for 1000-1100°C in the higher-pressure region above 100Torr, suggesting that more than one rate-limiting processes are involved in the temperature range. @FootnoteText@ @footnote 1@W.W.Mullins, J.Appl.Phys.28, 333(1957).@footnote 2@Y.-N. Yang, Elain S. Fu, and Ellen D. Williams, Surf. Sci. 356,101(1996) .

11:00am **MS-MoM9 Development of a Continuous Generation/Supply System of Highly-concentrated Ozone Gas for Low-temperature Oxidation Process**, ***S. Ichimura***, *H. Nonaka,* National Institute of Advanced Industrial Science and Technology (AIST), Japan*; Y. Morikawa, T. Noyori, T. Nishiguchi, M. Kekura,* Meidensha Corporation, Japan

Ozone has various superior characteristics compared to oxygen molecules in ultrathin oxide film formation on silicon. It realizes rapid oxidation rate at low substrate temperature, very thin transition layer in the oxide film, high electrical quality of the oxide film, etc. Those characteristics have been proved using a highly concentrated (HC) ozone generator, which supplies almost 100% ozone gas at pressure lower than 1000 Pa. The generator utilizes vaporization of pure liquid ozone accumulated in an ozone vessel. Since the liquid ozone accumulation is limited to 5 ml because of safety, the generator can supply only about 360 l ozone gas at the pressure. Considering future need in practical low-temperature oxidation process, we have developed a new system which continuously generate/supply HC ozone gas. The system is equipped with 4 ozone-vessels, and each vessel temperature can be controlled separately. During continuous operation, the condition of each ozone vessel changes stepwise with the same time interval along the following mode sequence; 1) cooling the vessel from 120K to 90K, 2) accumulation of liquid ozone by distillation of ozone/oxygen mixture gas at 90K, 3) heating the vessel from 90K to 113K and vaporization of pure liquid ozone, and 4) heating the vessel from 113K to 120 K and evacuation of the vessel. Allocating one of the 4 modes to each of the 4 ozone vessels so as to cover all the modes simultaneously, the system can supply constant flow of HC ozone gas. The maximum flow rate of the gas is 60 sccm, being enough for single wafer processing, and the ozone concentration is over 99 vol.% at the output of the system. The characteristics of the system in the formation of ultrathin oxide on 4 inch silicon wafer is examined, together with the effect in low temperature oxidation of excited state atomic oxygen which can be generated/supplied by photo-dissociation of ozone at sample position. @FootnoteText@@footnote 1@T. Nishiguchi et al. Appl. Phys. Lett. 81, 2190 (2002).

11:20am **MS-MoM10 Profile Control for Deep Silicon Etch by Sidewall Passivation in High Density Plasma**, ***M. Khbeis***, *G. Metze,* Laboratory for Physical Sciences*; K. Powell, D. Thomas, A. Pentland, J. Hutchings,* Trikon Technologies, Ltd.

Deep silicon etching of micron-sized structures is a critical step in high-aspect ratio via fabrication. This paper shows that m=0 Resonant Induction (M0RI) plasma technology coupled with the use of both etch and passivation gases produced deep via holes with unscalloped sidewalls at non-cryogenic temperatures. Process development, operational parameters, and potential applications are discussed. Wafer level packaging of high density, complex systems-on-chip is of great interest to the microelectronics industry for the production of compact devices and electronic components.@footnote 1@ Vertical integration of various unpackaged integrated circuits can be accomplished through die attachment, wafer-to-wafer bonding, thinning, and lastly high-aspect ratio backside interconnects for signal communication. During the fabrication of these 3-D systems there is a need to provide high-aspect ratio backside metal interconnects at a depth of at least 20µm. The fabrication of interconnect via holes dictate that the following etches be performed; oxide mask etch, bulk silicon etch, and buried oxide layer etch. Other potential applications for deep silicon etch include bulk micromachining for MEMS, ground/power plane connections, or re-routing of signal lines for novel packaging. In this paper, development of the deep bulk silicon etch is emphasized. To accommodate subsequent dielectric passivation and metallization steps, via holes were specified to have a profile angle of 89 to 90 degrees with absolutely no sidewall scalloping. Sidewall scalloping will impede metal transport during a high-pressure reflow process. Since deep reactive ion etch (DRIE) processes, such as Bosch, induce scalloping, alternative etch technologies that do not require switching of etchants and passivants are mandatory. @FootnoteText@@footnote 1@ J. Reche E. Korczynski, High-Density Thru-Silicon Interconnects, HDI Expo Proceedings,(2000).

11:40am **MS-MoM11 The Study on Deformation of ArF Photo Resist in Dry Etching**, ***C.-H. Shin***, *G.J. Min, C.J. Kang, J.T. Moon,* Samsung Electronics Co., Ltd., Korea

193nm ArF lithography has been introduced in DRAM industry for sub-90nm patterning. However, it has several issues in the substrate fabrication of sub-90nm patterning. First, the physical thickness of resist has been decreased less than 3000Å, which is critical point for stable pattern transfer. Second, durability of resist in the plasma was reduced due to the increase of Ohnish parameter. Third, resist is subjected to deformation when it is exposed to the plasma due to its soft chemical structure. All these factors limit the application of ArF lithography. Etching was performed in the commercially available dual frequency plasma based on O2, Ar, CO and C4F6 single gas chemistry, respectively. It was found that supply of bias power in the argon gas system led to the severe deformation of ArF photo resist. Novel techniques for the formation of protective layer will be discussed in this paper in order to suppress resist deformation with enhanced etch selectivity.

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