Manufacturing Science and Technology
Room 309 - Session MS-MoA

Challenges in Advanced Materials and New Processes for Semiconductor Manufacturing

Moderator: A. Testoni, Varian Semiconductor Equipment Associates

2:00pm **MS-MoA1 Research and Challenges in Nano Mechanics and Materials***, **K.P. Chong**,* National Science Foundation **INVITED**

Mechanics at the nano-scale is quite different from continuum mechanics. Nanomechanics is basic and essential in all areas of nano science, materials and engineering. Basic principles and experimental tools, multi-scale simulation, self-assembly as well as nanomechanics in information technology, biotechnology, micro/nano electronics [M/NEM] and other issues are presented. Recent workshops, research issues, research projects, as well as opportunities and challenges in nanomechanics are also discussed.

2:40pm **MS-MoA3 Opportunities and Challenges in the Materials Supply Chain for Semiconductor Manufacturing***, **R.J. Richardson**,* Air Products and Chemicals, Inc. **INVITED**

Over 100 gases and chemicals are used to manufacture semiconductor devices. Many of these materials present formidable challenges in synthesis, purification, analysis, container and distribution system compatibility, contamination control, ESH and regulatory issues. As we near the end of the CMOS roadmap, a large number of new materials and processes are being considered to enable the manufacture of ever-smaller device structures. Although the large number of new candidate materials appears to provide a number of new opportunities, they bring a host of challenges. Only a few of the new alternatives will eventually end up in high volume manufacturing, which poses a dilemma for a full service materials supplier beyond the decisions related to the allocation of scarce R&D resources to multiple solutions to the same problem. How these issues (e.g., purity requirements, materials compatibility studies, ESH impacts) are addressed for some of the new materials under consideration for advanced CMOS manufacturing and the various competing trends (e.g., consistency of supply vs. ever-higher purity) facing the materials supplier will be discussed.

3:20pm **MS-MoA5 New Processes and Materials for Environmentally Benign Semiconductor Manufacturing***, **F. Shadman**,* University of Arizona **INVITED**

The environmental issues are beginning to have significant impact on both the development of new processes and the application of new materials. In this presentation, some of the technical challenges and the potential solutions will be discussed. The specific examples will include: surface preparation, new dielectric materials, gaseous emissions particularly of global warming compounds, environmental bottlenecks in chemical mechanical planarization (CMP), and finally, environmental drivers for process integration in patterning and deposition of dielectrics in copper/low-k dielectric systems.

4:00pm **MS-MoA7 Sub-100 nm Copper Wiring Challenges and Solutions***, M. Xi, M. Yang, W.-F. Yau, J. Dukovic, **A. Rosenfeld**, N. Maity,* Applied Materials **INVITED**

With the emergence of sub-100 nm Cu-low k BEOL technology, copper-electroplating faces a new set of challenges. The combination of shrinking dimensions (coupled with an increase in aspect ratio) and increased current density, necessitate innovation in process and hardware development that can provide acceptable process integration results. Furthermore, the ever-shortened development cycle requires proliferation of new innovations into predictable and repeatable production-worthy processes in minimal development and qualification cycle time. The Cu metallization process is performed in two steps. First, thin metallic layers of barrier material (such as TaN or Ta) and Cu seed is deposited into the vias and lines that define the interconnect. Next, Cu electroplating is used to fill the interconnect structures. The function of the barrier material is to prevent Cu diffusion into the surrounding dielectric, while the Cu seed enables the electroplating fill. The key requirement for both barrier & seed layers is conformal step coverage in sub 100nm features. As such, ionized PVD technology is required to achieve the desired step coverage. To address this requirement, a novel magnetron source was developed that enables high metal ionization with a flat target. The flat target design enables low defects and low cost of ownership for the Cu Barrier-Seed process. Moving to 65 nm and below, the PVD films could be substituted by ultra-thin conformal ALD films, particularly for the barrier process. This will enable lower interconnect resistance and further reduce cost of manufacturing, by reducing the cost of consumables for both the barrier deposition and the barrier CMP processes. To address the needs of sub 100nm copper plating, a novel electroplating system featuring a small volume plating bath with individual electrolyte circulation is was developed. Conventional large volume electroplating bath systems is are adequate for 130nm productions needs, but shows limitations in the area of consistent gap fill and defect performance for sub 100nm applications. In addition, a large bath system lacks the flexibility to change chemistry quickly, which slow down the development and optimization of new processes to meet the new requirements. Root cause of the inconsistent gap fill is correlated to organic by-product build up. In one experiment, the total organic content of a large bath system is measured throughout the life of the bath. The result shows that gap fill consistency is compromised when the total organic content is above 550ppm. In contrast, the small volume plating system allows periodic dumping and refilling of the plating bath after processing a small number of wafers, such as 200 wafers. This provides two key advantages. First, incoming wafers are exposed to fresh plating solution. This minimizes the gap fill inconsistency caused by aging and breakdown of the organic additives mentioned above. Second, by dumping and refilling the small bath after a small number of wafers are processed, different chemistry can be introduced and tested efficiently, from one bath to the next. This can provide significant time and chemical savings for process development and optimization. In addition, the individual electrolyte circulation design allows different plating cells within a plating system to process with different chemistries. This design enables sequential processing, or multi-step plating within a single plating system. The advantage of multi-step plating is demonstrated with experimental results showing dramatic reduction in as plated mounding.

4:40pm **MS-MoA9 Nanoporous Organosilicates for On-Chip Applications Using Sacrificial Macromolecular Porogens***, **R.D. Miller**, W. Volksen, H.-C. Kim, E. Connor, J.L. Hedrick, C.J. Hawker, T. Magbitang, V. Lee,* IBM Almaden Research Center **INVITED**

Porous organosilicates have many potential applications, including separation media, catalyst supports, high surface area materials for bio-applications and ultralow-k media for on-chip insulator applications. The latter is driven by the need for low-k insulators to minimize signal delays and crosstalk. We have studied the generation of nanoporous thin film organosilicates using sacrificial macromolecular porogens, a process that requires a tailored interaction between the pore generators and the respective matrix resin. Depending on the porogen structure, the pore generating process can be classified either as nucleation and growth or templating. Each technique produces porous materials, but the film morphologies can be quite process specific. The integration of porous organosilicates for copper interconnects puts a premium on matrix mechanical properties. These can be altered by structural variations and/or process variations. The generation, characterization and integration of porous thin organosilicate films will be discussed.

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