High-k Gate Dielectrics and Devices Topical Conference
Room 317 - Session DI-TuM

High-k Dielectric Growth and Processing

Moderator: R.L. Opila, University of Delaware

8:20am **DI-TuM1 Effects of Transistor Fabrication Process Conditions on Electrical Characteristics of High-k Gate Dielectrics**, ***G. Bersuker***, *P. Zeitzoff, G.A. Brown, J. Gutt, N. Moumen, J. Peterson, J. Barnett,* International Sematech*; B.H. Lee,* International Sematech, Korea*; C.H. Lee, S. Gopalan, N. Chaudhary, Y. Kim, C. Young, P.S. Lysaght, H.-J. Li, M. Gardner, R.W. Murto, H.R. Huff,* International Sematech **INVITED**

Comprehensive evaluation of high-k materials for gate dielectric applications requires fabrication of transistor test structures. The complex fabrication process includes several operations employing highly reactive ions, which may potentially affect electrical performance of the high-k materials. It is, therefore, critical from a materials evaluation standpoint to separate intrinsic properties of high-k dielectrics from process-related effects. The latter is the focus of this investigation. In particular, we concentrate on the charging problem associated with high-k materials, which appears to be one of the major factors affecting threshold voltage and mobility in high-k gate dielectric transistors. Our results demonstrate high sensitivity of the high-k films to the transistor fabrication process conditions. It is shown that electrical properties of gate stacks fabricated with a variety of combinations of ALD and MOCVD Hf-based dielectric compositions can be greatly affected by process-induced charges (PIC). PIC caused by negatively charged ions and/or electron trap inducing species may accumulate in the area of the high-k film exposed to various plasma operations during post gate definition processing (such as poly etch, ash/clean and spacer deposition). These contaminants may diffuse under the gate during subsequent high temperature processing and adversely affect device performance. Significant dependence of the electrical characteristics on the process scheme employed for the transistor fabrication complicates the evaluation of the intrinsic properties of the high-k gate dielectrics.

9:00am **DI-TuM3 Characteristics of High-k Gate Dielectric Formed by Oxidation of Sputtered Hf/Zr/Hf Thin Fims on the Si Substrate**, *H.-D. Kim,* ***Y. Roh***, *N.-E. Lee, C.-W. Yang,* Sungkyunkwan University, Korea

Recently, high-k gate oxide have been extensively investigated to overcome the problems such as large leakage current caused by the direct tunneling through extremely thin SiO@sub 2@. We previously demonstrated that simple oxidation of sputtered Hf thin films on Si results in HfO@sub 2@HfSi@sub x@O@sub y@ stacked high-k gate oxides simultaneously with excellent physical and electrical properties; negligible hysteresis, excellent EOT value (1.2 nm) and low leakage current (2 X 10@super -3@ A/cm@super 2@ at 1.5 V after compensating the flatband voltage). In this work, we further investigated the characteristics of high-k gate dielectric formed by the oxidation of Hf/Zr/Hf film (1.5 nm) deposited on the Si substrate by a sputtering method. The oxidation and annealing were performed at 500~800 °C for 60~120 min under O@sub 2@ ambient and at 500~900 °C for 30~60 min under N@sub 2@ ambient, respectively, in furnace. To form MOS capacitors, Pd gate was thermally evaporated on the HfO@sub 2@ film using a shadow mask with circular dots. We found that the electrical properties of MOS devices with oxidized Hf/Zr/Hf film are further improved as compared to those obtained after oxidizing single Hf film with same thickness (i.e., 1.5 nm) In addition to the negligible hysteresis, we obtained the EOT value of 1.15 nm and the leakage current density of 4.2 X 10@super -3@ A/cm@super 2@ at -3 V. More importantly, the deterioration of high-k gate oxide caused by high-temperature oxidation and/or annealing processes drastically minimized. For example, even after the 900 °C oxidation of Hf/Zr/Hf film, EOT and leakage current density were 1.37 nm and 2.78 X 10@super -6@ A/cm@super 2@ at -3 V, respectively. We speculate that this improvement is due to the minimization of undesirable SiO@sub 2@ formation between High-k oxide and Si. These results, as well as further investigation of physical properties of the samples using XPS, will be presented at the conference.

9:40am **DI-TuM5 Study of ZrO@sub 2@ Initial Stage Deposition on Si(100) During High Vacuum Chemical Vapor Deposition**, ***Z. Song***, *R.D. Geil, D.J. Crunkleton, V.L. Wahlig, B.R. Rogers,* Vanderbilt University

ZrO@sub 2@ is a potential high-k material to replace SiO@sub 2@ gate dielectrics in MOSFET devices. Electrical and structural requirements of the gate dielectric dictate that these layers will be significantly less than 10 nm thick. Studies of the initial stages of ZrO@sub 2@ deposition is needed in order to create an abrupt, low defect interface with silicon. In this work, we used atomic force microscopy (AFM), spectroscopic ellipsometry (SE), X-ray photoelectron spectroscopy (XPS), and transmission electron microscopy (TEM) to study the initial deposition behavior of ZrO@sub 2@ films. Films were deposited at pressures of 10@super -5@ to 10@super -4@ Torr and substrate temperatures of 250 to 450 °C. We observed a transition from 3D growth to 2D growth. These results suggest that a deposition temperature greater than 350 °C is needed to form a uniform film.

10:00am **DI-TuM6 Thin Film Growth and Composition Characterization of Hafnium Oxide Grown on Surface Treated Silicon by Atomic Layer Deposition**, ***R. Inman***, *A. Deshpande, G. Jursich,* American Air Liquide

New materials are needed for future generation of semiconductor devices and hafnium oxide along with silicate and aluminate combinations continue to show promise for meeting stringent demands of the gate dielectric insulator layer in CMOS transistors. In this critical application, film growth needs to be well controlled by process conditions and deposition requires high level of conformality as layer thickness extends below 100 nm dimension and more complex gate geometries are proposed. To best serve these requirements, atomic layer deposition is an ideal method of growing such films. In this work, thin films of hafnium oxide were deposited on Si(100) substrates by means of atomic layer deposition (ALD) technique using tetrakis(diethylamino)hafnium precursor. The resulting composition and purity of these films were determined at different substrate temperatures using x-ray and Fourier Transform Infrared (FTIR) spectroscopies. FTIR studies confirmed that the resulting films are relatively free of carbon contamination and provided a measure of hydroxyl groups in the film. The kinetics of film growth was also investigated by measuring film thickness as a function of substrate temperature and reagent pulsing characteristics. The thickness measurements indicated a relatively mild inverse temperature dependence of film growth in the range of 250 - 350 C. The cycle number dependence of film growth was examined at both high and low cycle number in order to infer the nucleation growth of the film. These results will be presented using Si substrates with different surface treatments.

10:20am **DI-TuM7 The Effect of Hf Content in Liquid Precursor on the Properties of Mist Deposited Ultra-Thin Films of HfSiO@sub 4@**, ***K. Chang***, *K. Shanmugasundaram,* The Pennsylvania State University*; D.-O. Lee, P. Roman, P. Mumbauer,* Primaxx Inc.*; J.R. Ruzyllo,* The Pennsylvania State University

Ultra-thin (<10nm) films of hafnium silicate formed by mist deposition method for gate dielectric application in advanced MOS devices were investigated. Precursors with Hf:Si ratio of 0.103:1, 0.276:1, and 1:1 were prepared to investigate the effect of Hf content on mist deposition process and film characteristics. MOS capacitors were fabricated for electrical characterization using Pt gate electrode. The Hf composition in the HfSiO@sub 4@ film was analyzed with angle-resolved X-ray photoelectron spectroscopy. The 1:1 precursor resulted in 12.6 at.% of Hf in the film and 7.5 at.% of Hf was obtained in the HfSiO@sub 4@ film deposited with 0.103:1 precursor. Deposition rate of HfSiO@sub 4@ linearly increases with the Hf content in the precursor even though the Hf composition in the film didn't scale in the same order. Despite the difference in Hf content of the precursor, an interfacial oxide 2.2nm ~ 3.0nm thick was always detected by transmission electron microscopy. Through electrical characterization, it was determined that the obtained gate stacks feature an equivalent oxide thickness of 0.8nm ~ 1.5nm depending on the process. It is postulated that the lower EOT is caused by Hf diffusion from HfSiO@sub 4@ film during thermal treatment step and lower EOT of the interfacial layer. For lower EOT of the interfacial oxide, higher Hf content in the precursor is needed. Using 1:1 precursor, EOT 1.5nm HfSiO@sub 4@ thin film is deposited with leakage current density of less than 1×10@super -2@ A/cm@super 2@.

10:40am **DI-TuM8 The Effect of Surface Preparation and Post Growth Annealing on the Thickness and Composition of High-k Layers Grown on Silicon**, *T. Conard,* IMEC, Belgium*; R.K. Champaneria, P. Mack,* Thermo Electron, UK*; R.G. Vitchev,* Facultes Universitaires Notre-Dame De La Paix (FUNDP), Belgium*; R.G. White,* ***J. Wolstenholme***, Thermo Electron, UK

The move to high-k materials for gate dielectrics brings with it a new set of parameters that require characterisation. As with silicon dioxide, the thickness of the layer must be measured but, in addition, the thickness of any intermediate layer must be measured also. The chemistry of the intermediate layer is likely to affect the electrical properties of the layer and therefore needs to be understood along with the factors that affect

this chemistry. XPS has an information depth that is similar to the thickness of the layers and, therefore, can be used to characterise them. If the information depth is controlled by varying the photoelectron emission angle (angle resolved XPS or ARXPS) more information becomes available. Thickness of surface and subsurface layers can be measured with accuracy and precision. The chemical state of each component of the material can also be determined and the distribution of chemical states within the layer can be measured. Since no material is removed during the measurements, ARXPS can be regarded as a non-destructive technique. This technique has been used to analyse HfO2 and Al2O3 layers on silicon prepared by ALD or MOCVD. A comparison will be made of the layers grown on relatively thick (up to ~1 nm) silicon oxide with those grown on thin oxide layers and on layers containing nitrided SiO2. It will be shown how XPS and ARXPS can determine the effect of the preparative method on the thickness of the layers and the chemical states of the component materials. The results will be presented in the context of those on the same materials from other techniques.

11:00am **DI-TuM9 Si and Ge Surface Functionalization Characterized by In Situ and Ex Situ Infrared Spectroscopy**, *M.M. Frank,* IBM T.J. Watson Research Center and Rutgers University*; M.-T. Ho, S. Dörmann, C.-L. Hsueh,* Rutgers University*; L.J. Webb, N.S. Lewis,* California Institute of Technology*; S. Rivillon,* Rutgers University*; O. Pluchery,* Université Paris 6, France*;* ***Y.J. Chabal,*** Rutgers University

Chemical functionalization and passivation of semiconductor surfaces is often necessary to foster uniform nucleation and high-quality interface formation in the deposition of ultrathin high-@kappa@ gate dielectrics and organic films. To understand the formation of such monolayers in wet, gaseous, or ultra-high vacuum environments, it is desirable to monitor surface reactions in situ. Utilizing infrared absorption spectroscopy, we have achieved such in situ monitoring with submonolayer sensitivity. We have performed both in situ and ex situ studies to gain mechanistic insight into surface chemical reactions on HF-etched, mostly H-terminated Si and Ge surfaces. Chemical species studied include: Cl, supplied via gas phase and wet chemistry, enabling subsequent activation of the Si substrate through hydroxylation; trimethylaluminum (Al(CH@sub 3@)@sub 3@) and other metal organic precursors, to initiate homogeneous atomic layer deposition or chemical vapor deposition of high-@kappa@ gate dielectrics (Al@sub 2@O@sub 3@ and HfO@sub 2@) onto hydrogen-terminated Si; and alkyl groups from wet chemistry, to passivate the Si. In particular, we shed light on the reactivity of Si-CH@sub 3@ and metal-CH@sub 3@ species formed in reactions with organic high-@kappa@ precursors and in wet chemical passivation. On Ge, we are investigating hydrogen passivation in HF using in situ methods, as well as the oxidation of such passivated surfaces. We compare and contrast the passivation and oxidation mechanisms on Si and Ge substrates.

11:20am **DI-TuM10 Plasma Deposition of RuO@sub2@ on HfO@sub2@ for Gate Electrode Applications**, ***D.B. Terry***, *J.M. Doub, G.N. Parsons,* North Carolina State University

Ruthenium-based metals are potential candidates for gate electrodes in advanced gate stack applications. The detailed structure of the interface between high-k dielectrics and the gate metal will be important to maintain low equivalent oxide thickness, but the effect of metal deposition on the high-k/metal interface structure is not known. We have deposited RuO@sub2@ metal from Tris-tetramethyl-heptadianato Ru (Ru TMHD) introduced downstream from a remote N@sub2@O plasma at 365 and 500°C, and examined the deposited film and interface structure using Auger and X-ray photoelectron spectroscopies. The growth rate at 500°C is approximately twice that at 365°, and films show some evidence for N and C incorporation, consistent with the 250°C decomposition temperature of the Ru TMHD. Based on AES results, the O/Ru ratio is larger for the films deposited at higher temperature. Because of the difference between the oxidizing and reducing environments in CVD processing, we expect that metallic oxides such as RuO@sub2@ will result in different metal/dielectric interface structure than for elemental metal/dielectric interfaces. To examine the role of deposition chemistry on interface structure, several thicknesses of RuO@sub2@ have been deposited by plasma CVD on HfO@sub2@ formed in our lab by atomic layer deposition. The effect of HfO@sub2@ surface structure, and the trends in RuO@sub2@ composition with film thickness determined using AES and XPS will be presented and discussed.

11:40am **DI-TuM11 Novel Ultra-thin TiAlO@sub x@ Alloy Oxide for New Generation of Gate Dielectric**, ***W. Fan***, Northwestern University*; S. Saha, B. Kabius, J.M. Miller, J.A. Carlisle, O. Auciello,* Argonne National Laboratory*; S.Y. Li, V.P. Dravid, R.P.H. Chang,* Northwestern University*; C. Lopes, E.A. Irene,* University of North Carolina, Chapel Hill

A novel TiAlO@sub x@ alloy oxide has been developed and studied as an alternative gate oxide material for CMOS devices (patent pending). Ultra-thin TiAl (3:1) films with physical thickness 3-20 nm were grown on n-Si (100) by sputter deposition. In-situ oxidation was then performed by using both molecular oxygen (P=1.0x10@super -3@ Torr) and atomic oxygen sources (P=1.0x10@super -4@ Torr). The formed TiAlO@sub x@ exhibits amorphous structure on Si, as revealed by XRD and TEM analyses. In-situ XPS study shows that a full oxidation of TiAl can be achieved at 500@super o@C using both oxygen sources. However, the TiAlO@sub x@ layer formed through atomic oxygen annealing presented a leakage current 150 times lower than the one with molecular oxygen annealing. Since both Ti and Al have more negative oxide formation energies than Si, the presence of Ti and Al at the interface with Si significantly reduces the formation of interfacial SiO@sub x@. It has been confirmed by XPS depth profile, ellipsometry and cross-sectional TEM, which revealed ~1 nm SiO@sub x@ layer formed at the oxide/semiconductor interface with 500@super o@C oxidation. The amorphous TiAlO@sub x@ layer with equivalent oxide thickness (EOT) of 1.7 nm and negligible hysteresis was obtained via atomic oxygen exposure at 500@super o@C, exhibiting high permittivity (~30) and low leakage current density (1.2x10@super -2@ A/cm@super 2@). After post deposition annealing with top gate electrode in place, the leakage was further improved and reached 5.4x10@super -5@ A/cm@super 2@. Furthermore, extended study shows that a full transition of TiAl to TiAlO@sub x@ can be accomplished at room temperature by exposure to atomic oxygen beam. Interfacial SiO@sub x@ formation, therefore, was completely eliminated and TiAlO@sub x@ layer with EOT less than 1 nm was achieved on Si. @FootnoteText@*This work was supported by the U.S. Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.@.

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