## Tuesday Afternoon, November 4, 2003

#### High-k Gate Dielectrics and Devices Topical Conference Room 317 - Session DI-TuA

#### High-k Dielectric Characterization

Moderator: E.L. Garfunkel, Rutgers University

2:40pm DI-TuA3 Invited Paper, E. Cartier, IBM T.J. Watson Research Center INVITED

3:20pm DI-TuA5 Enhanced Tunneling in Symmetric Stacked Gate Dielectrics with Ultra-thin HfO@sub 2@ Layers (0.5-10. nm) Sandwiched between Thicker SiO@sub 2@ Layers (1.5 nm), C.L. Hinkle, C. Fulton, G. Lucovsky, R.J. Nemanich, North Carolina State University

A novel method for obtaining the tunneling mass, m@sub eff@, and conduction band offset energy with respect to Si, E@sub B@, for high-k gate dielectrics is presented. It is based on a quantum mechanical WKBapproximation that explains large bias dependent increases in tunneling in symmetric stacked devices with ultra-thin HfO@sub 2@ layers (~0.5 nm) sandwiched between thicker SiO@sub 2@ layers (~1.0-1.5 nm) as compared with reference devices with homogenous SiO@sub 2@ dielectrics. J-V traces for substrate injection indicate a marked departure from the approximately exponential bias dependence of homogenous dielectrics for V@sub ox@ = V@sub g@ - V@sub fb@ >1 V. This correlates with differences between the tunneling attenuation factors, @alpha@@sub i@t@sub i@ = 4@pi@t@sub i@(2m@sub effi@E@sub Bi@)@super 0.5@/h, in the constituent layers, i, where t@sub i@ is the i@super th@ layer thickness. For V@sub ox@ >1 eV, small decreases in @alpha@t(SiO@sub 2@) compared to larger decreases in @alpha@t(HfO@sub 2@) result in a marked increase in their ratio. For V@sub ox@ > 1.5 V, there is minimal attenuation in the HfO@sub 2@ layer, so that the tunneling current is determined predominantly by the SiO@sub 2@ layer. At V@sub ox@ = 3V, the relative current with respect to the reference Si device is >1000. By analyzing these data, and increasing the thickness of the HfO@sub 2@ layer beyond 2 nm to determine the thickness at which relative tunneling begins to decrease due to increased attenuation in that component of the stack, values of m@sub eff@ = 0.15±0.05 m@sub o@ and E@sub B@ = 1.4±0.2 eV are obtained for HfO@sub 2@.

#### 3:40pm DI-TuA6 Observation of Bulk HfO@sub 2@ Defects by Spectroscopic Ellipsometry, H. Takeuchi, D. Ha, T.-J. King, University of California at Berkeley

HfO@sub 2@ (hafnium oxide) is a promising candidate to replace SiO@sub 2@-based films as the gate dielectric in ultra-scaled MOSFETs, due to its thermal stability in contact with Si, compatibility with a conventional CMOS process flow, and moderately high dielectric constant (20-25). The electrical characteristics of HfO@sub 2@ films, such as equivalent SiO@sub 2@ thickness (EOT), leakage current density, hysteresis in capacitance vs. voltage curves, fixed charge density and resultant field-effect carrier mobilities, have been extensively investigated. However, the physical mechanism for deviation from ideal behavior is not yet well understood. In particular, not much is known about bulk defects inside HfO@sub 2@ and their impact on electrical characteristics and the thermal stability of HfO@sub 2@. In this study, we report a bulk defect in HfO@sub 2@ which can be detected as an optical absorption peak by spectroscopic ellipsometry (SE). 12.5nm-thick HfO@sub 2@ films were formed by oxidation of pure Hf films in a cold-wall rapid thermal annealing (RTA) reactor. Absorption coefficients near the absorption edge were extracted by the data inversion method, in which the optical constants for short wavelength were calculated using the thickness obtained from long wavelength data. The obtained optical bandgap of 5.7eV matches very well with theoretical calculation and VUV measurement reported by other groups, and a shift due to crystallization was also detected. In addition, an extra absorption peak was observed in 4.5~5.0eV range. The energy difference between this absorption peak and the bandgap corresponds well to the trap energy extracted from measurement of the temperature dependence of Poole-Frenkel current. Hence, the peak is associated with electron transition from the valance band to the trap energy level inside the bandgap. This peak reduces with oxidation annealing time, indicating that the defects can be attributed to oxygen vacancies in the HfO@sub 2@ film.

4:00pm DI-TuA7 Chemically Abrupt Interfaces between Lanthanum Aluminate and Silicon for Alternative Gate Dielectric Applications, *L.F. Edge*, *D.G. Schlom*, Pennsylvania State University; *S.A. Chambers*, Pacific Northwest National Laboratory; *C.L. Hinkle*, *G. Lucovsky*, North Carolina State University

LaAlO@sub 3@ is one of the most promising alternative gate dielectrics for the replacement of SiO@sub 2@ in silicon MOSFETs. Single crystalline LaAlO@sub 3@ is known to have a dielectric constant of 24 and an optical bandgap of 5.6 eV. The band offsets between LaAlO@sub 3@ and Si have been predicted to be in the range 2.1 to 3.5 eV for electrons and 1.0 to 1.9 eV for holes. It will be shown that LaAlO@sub 3@ is stable in contact with silicon under standard MOSFET processing conditions. Epitaxial Si has been grown by MBE on single crystals of LaAlO@sub 3@ and annealed at 1026C, which is a standard implant activation anneal for MOSFETs, and the interface remained stable and free of SiO@sub 2@. A major challenge in the growth of alternative gate dielectrics on Si is the formation of unwanted SiO@sub 2@ at the interface. One technique to prevent the formation of SiO@sub 2@ is to grow in a low temperature and excess oxidant regime. We have investigated the oxidation kinetics of Al and La, both individually and together (codeposition), to determine the minimum oxygen partial pressure required to achieve fully oxidized LaAlO@sub 3@. Using these optimized conditions, amorphous LaAlO@sub3@ films as thin as 1.0 nm have been grown on silicon by MBE. AES and XPS analyses indicate that the films are fully oxidized and show no SiO@sub 2@ at the interface, even after prolonged exposure of the films to air.

4:20pm DI-TuA8 Medium Energy Ion Scattering Studies of the Structure and Composition of Epitaxial SrTiO@sub 3@ Films on Silicon, *L.V. Goncharova*, *D.G. Starodub*, *E.L. Garfunkel*, *T. Gustafsson*, Rutgers University; *D.G. Schlom*, Pennsylvania State University

Thin crystalline oxide films on silicon show a wide range of new electronic, optical, and magnetic properties with potential impact on novel devices. Precision control of the composition, stoichiometry and structure of such films and the ability to characterize the films and their interfaces are therefore of central importance. We have used high-resolution medium energy (~ 100 keV) ion scattering (MEIS) to investigate the composition and structure as a function of depth of thin (40-250 Å) crystalline SrTiO@sub 3@ films on Si (100). As ion beams are penetrating, and the ion-solid interaction is well understood, this technique allows us to get quantitative information both about the film/vacuum and about the film/substrate interface structure. Different channeling and blocking geometries have been utilized to distinguish epitaxial/amorphous regions, to characterize the chemical composition of the SrTiO@sub 3@/Si interface and also to give information about structural parameters. Thin SrTiO@sub 3@ films were grown epitaxially on Si(001) at the low temperatures in an excess of oxygen.@footnote 1@ Our MEIS results show that films grown by this method have A-site (SrO) termination. We further show that submonolayer amounts of strontium silicide, used in the initial stages of growth, are fully eliminated from the interface after growth is completed and that instead Ti has diffused into the interface region. The SrTiO@sub 3@/Si interface was confirmed to be crystalline; however the geometrical structure deviates significantly both from the 'bulk' epitaxial film and from the substrate. Possible structural models for the transition region and mechanisms of titanium incorporation in the interface region will be discussed. @FootnoteText@ @footnote 1@ J. Lettieri, J.H. Haeni, and D.G. Schlom, J.Vac.Sci.Technol. A 20 (2002) 1332.

4:40pm DI-TuA9 In-situ and Ex-situ Characterization of Barium Strontium Titanate Thin Films on Thermal SiO@sub 2@/Si Substrates, N.A. Suvorova, C.M. Lopez, University of North Carolina, Chapel Hill; A.A. Suvorova, M. Saunders, University of Western Australia; E.A. Irene, University of North Carolina, Chapel Hill

Alternative materials with high dielectric constant (k) are in demand for replacement of SiO2 in MOSFET devices. Barium strontium titanate (BST) is one of possible candidate for DRAM applications. The most important requirement for the incorporation of an alternative gate dielectric is to maintain a high quality interface with Si comparable to that of SiO2 /Si. Similar to other high k materials for BST this is a major problem due to interface reaction with Si. One potential solution is the use of a thermal SiO2 ultra thin underlayer, which helps to minimize the reaction between high k dielectric and Si as well as maintain the high interface quality. However this solution degrades the k values of the two film gate stack. The present study is aimed toward optimizing the SiO2 underlayer thickness in order to maintain the interface quality yet minimize the effect on k. The results from this optimization study are presented with emphasis on the

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key process parameters that improve the dielectric film stack. For in-situ growth characterization of BST film grown on thermally oxidized Si substrates spectroscopic ellipsometry has been used. Studies of material properties have been complemented with analytical electron microscopy. Electrical characterization has been employed for ex-situ studies of Pt/BST/SiO2/Si structures. From conductance-voltage analysis, the interface trap density Dit was observed to significantly decrease for the capacitors grown on oxidized Si substrates and annealed in forming gas.

## 5:00pm DI-TuA10 Band Offsets at Ba- SrTiO@sub 3@ / Si Interfaces, F. Amy, A. Wan, A. Kahn, Princeton University

The continuous drive toward faster electronics and scaling down of MOSFET device dimensions requires alternatives to SiO@sub 2@ for gate dielectrics. High-k dielectrics have therefore received considerable attention from industry and the scientific community. Crystalline perovstike oxides such as SrTiO@sub 3@ and BaTiO@sub 3@ are of special interest and offer several advantages. First, they can be MBE-grown latticematched to Si (or Ge) substrates with very low interface state density.@footnote 1@ Second, they can serve as a buffer layer for the growth of semiconductors, opening possibilities for integrating Si electronics and III-V optoelectronics. However, several issues concerning these materials remain to be fully addressed, among which band offsets with Si and other semiconductors. In this work, we use a SrTiO@sub 3@(100 Å)/BaSrO(11 Å)/Si structure grown by MBE, and X-ray and UV photoemission spectroscopy to study core levels and valence band respectively. Depending on surface preparation, including ex-situ UV ozone, O@sub 2@ or UHV annealing, the valence band maximum position shifts by more than 2 eV, whereas very little if any shift is observed on core levels. These findings indicate that surface composition and morphology are of paramount importance in the UPS determination of electronic structure, and may explain discrepancies between results reported in the literature. Our investigation of clean and stoichiometric SrTiO@sub 3@ surface indicates that its conduction band minimum is located 0.4 eV (± 0.4) below the one of silicon. An in-depth investigation of the role of surface preparation is being pursued, and results on BaTiO@sub 3@/SrTiO@sub 3@/Si samples will be reported. @FootnoteText@ @footnote 1@ . R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. 293, 468 (2001)

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