Monday Afternoon, November 3, 2003

High-k Gate Dielectrics and Devices Topical Conference
Room 317 - Session DI-MoA

High-k Dielectric Stability

Moderator: Y.J. Chabal, Agere Systems

2:00pm **DI-MoA1 Etching and Thermal Stability of Zirconium and Hafnium Oxide High-k Dielectrics***, **J.P. Chang**,* University of California, Los Angeles **INVITED**

The aggressive down-scaling of the silicon based metal-oxide-semiconductor field effect transistor (MOSFET) replies strongly on the materials and the resultant electrical properties associated with the dielectric material employed to isolate the transistor gate from the silicon. Currently, the major challenges in integrating high-k materials include a thorough understanding of the thermal stability of these materials on silicon and an effective etching chemistry in patterning these materials. In this talk, I will discuss current research progress in atomic layer controlled deposition of high-k dielectric films on silicon with tailored electronic, chemical, interfacial, thermal, and mechanical properties, followed by discussions on plasma patterning of the high-k materials. Specifically, research work on ZrO@sub 2@ and HfO@sub 2@ thin films and their thermal stability, dielectric function, and integration on silicon surfaces will be presented. The talk will focus on linking the molecular coordination and film morphology to the electronic properties of the high-k dielectrics, and elucidating the reaction pathways leading to the deposition of thermally stable, stoichiometric, amorphous, smooth, uniform, and highly conformal high-k dielectrics. Plasma enhanced etching of metal oxides in halogen based chemistries will be presented, including the effect of ion energy and ion type on etching rate and etching selectivity. I will also highlight some new research directions that aim at enabling the predictive engineering of a superior high-k/silicon interface and its associated device performance through ab initio calculations.

2:40pm **DI-MoA3 Structure and Stability of Alternative High-K Gate Dielectrics***, **S. Stemmer**,* University of California, Santa Barbara **INVITED**

This talk will present an overview of extrinsic and intrinsic stability issues of high-k dielectrics, such as ZrO@sub 2@, HfO@sub 2@, Y@sub 2@O@sub 3@, their alloys with SiO@sub 2@ or Al@sub 2@O@sub 3@, and their interfaces with electrodes and Si. While thermodynamics predicts that all high-k gate dielectrics currently under investigation are stable in contact with Si, interfacial reactions have been reported. We show that gate oxide stoichiometry and processing conditions, such as oxygen excess or reducing conditions, can explain reactions and are consistent with predictions from thermodynamics. Intrinsic stability issues include phase separation of silicates and aluminates, and will be discussed in the context of equilibrium as well as metastable phase diagrams, respectively. A combination of experimental methods is needed to experimentally analyze the stability of these ultrathin layers. We have used electron energy-loss spectroscopy (EELS), atomic resolution Z-contrast imaging, high-resolution transmission electron microscopy, small angle x-ray scattering (SAXS) and x-ray absorption spectroscopy fine structure analysis (XANES) to dielectric layers after high temperature anneals necessary for CMOS device processing. For example, phase separated microstructures of Hf-silicate films with different compositions show different morphologies and kinetics, due to mechanisms of microstructural evolution by nucleation and growth, and spinodal decomposition, respectively, consistent with the predictions from metastable phase diagrams. SAXS is used to study the kinetics of phase separation. Oxygen deficiency can lead to silicide reactions, whereas oxygen excess in the films is responsible for interfacial silicate reactions in rare earth oxide films on Si. This research was performed in collaboration with J.-P. Maria, A. Kingon, G. Parsons, P. Lysaght, P. C. McIntyre, S. Ramanathan, and T.P. Ma.

3:20pm **DI-MoA5 Hafnium Silicate High-K Dielectric Etch with High Selectivity to Si at Low Wafer Temperatures***, S. Ramalingam,* Lam Research Corporation*; **C.B. Labelle**,* Advanced Micro Devices*; S.D. Lee, G.P. Kota, C. Lee, V. Vahedi,* Lam Research Corporation

Advanced microprocessors require the use of increasingly thin gate oxide materials to achieve the highest performance. To date, these materials have consisted primarily of SiO2 and nitridized SiO2, but the leakage current behavior of these materials becomes undesirable as they are successively thinned (=12Å). A potential solution to this problem is replacement of SiO2 by an insulator with a higher dielectric constant (high k). Keeping with current integration schemes, gate etching would then require etching through the polysilicon and high-k materials, stopping on the underlying silicon. However, high-k materials have proven very challenging to etch, specifically due to the low volatility of etch products, which typically require an aggressive approach to the etch, most notably including high temperatures. Key etch issues include selectivity to polysilicon/bulk silicon and masking material, redeposition of high k materials on the poly gate sidewalls, and altering of the poly gate profile and/or CD. A Lam 2300 SeriesTM silicon etch reactor has been used to etch photoresist-masked polysilicon gate wafers with HfSiOx gate dielectric. A BCl3-based process has been developed that provides excellent selectivity to polysilicon, no high k redeposition, and <10Å silicon recess. Selectivity to Si is attained at low ion energy and through passivation of the surface by formation of Si-B bonds. A key advantage of this process over those currently in practice is that wafer temperatures higher than those in typical gate etch processes are not necessary. Key etch results will be presented, including analysis of the impact of a boron-based etch process on gate doping.

3:40pm **DI-MoA6 Post Deposition Stability of High-k Dielectrics to Air Exposure and its Implications to Interface Reactivity***, **T. Gougousi**, D. Niu, R.W. Ashcraft, G.N. Parsons,* North Carolina State University

Post-deposition stability of the gate oxide is an important issue for advanced gate stacks. For this study, group III and IV high-k dielectrics films are deposited on Si by PECVD or by metal sputtering and ex-situ oxidation in N@sub 2@O. After deposition the dielectrics are permitted to react with ambient H@sub 2@O and CO@sub 2@ for extended periods and their stability is monitored as a function of time using FTIR. We find that group III (Y and La) based-films are generally susceptible to reactions with H@sub 2@O and CO@sub 2@ forming hydride and carbonate species. For PVD La films, the oxidation temperature affects the film stability significantly. Films oxidized at 600°C show signs of reaction within minutes of air exposure while films oxidized at 900°C are stable for exposures up to two weeks. Y@sub 2@O@sub 3@ CVD films deposited at 400°C also show high reactivity with H@sub 2@O. Post deposition inert anneals at 900°C in N@sub 2@ improves the film stability significantly. In-situ capping of the Y@sub 2@O@sub 3@ films with 500Å of a-Si reduces greatly the amount of OH detected in the films. Group IV (Hf and Zr) based film exhibit superior stability as compared to the group III films, however. Carbonate formation is verified for both HfO@sub 2@ and ZrO@sub 2@ films. OH is practically undetectable in the films even after ambient exposure for six months. The effect of the OH incorporation on the interface stability will be discussed, and examples of OH promoted reactions between the dielectric film and the Si substrate or polysilicon gate metal will be presented.

4:00pm **DI-MoA7 Growth, Characterization and Thermal Stability of High-K Gate Stacks***, **E.L. Garfunkel**, T. Gustafsson, D.G. Starodub, S. Sayan, L.V. Goncharova, D. Vanderbilt, X. Zhao, R.A. Bartynski,* Rutgers University*; T. Nishimura,* Murai Project, Japan*; Y.J. Chabal,* Rutgers University **INVITED**

We describe recent results using medium energy ion scattering (MEIS), soft x-ray photoemission (SXPS), inverse photoemission (IPES), electron microscopy (TEM), infrared spectroscopy (FTIR), electrical methods and first-principles calculations to examine high-K gate dielectrics and their interfaces with silicon and metal layers. MEIS has proven extremely helpful in presenting accurate elemental depth profiles of high-K films on Si, Ge and GaAs, especially related to the problem of interface composition. Our isotopic labeling results give new insight on oxygen incorporation and diffusion in high-K films. In selecting an alternative (to SiO2) gate insulators, many parameters in addition to dielectric constant and thermal stability must be considered, including the barrier heights for tunneling. Our SXPS and IPES experimental results are complemented by first-principles density functional calculations to study the properties of the different crystalline phases of HfO2 and ZrO2. It is found that the band gap, barrier height and dielectric response of these two materials are phase dependent. The densities of states are calculated and compared to various experimental measurements. The thickness, layered structure, and crystal phase of the as-deposited and annealed films have been studied by diffraction (XRD), x-ray adsorption (XAS), MEIS and TEM. Critical electrical and materials changes occur during post-processing at elevated temperature. We discuss these changes, including the decomposition of the films in reducing environments in the 900-1100Â°C range. Finally, FTIR results on initial surface reactivity and ALD/CVD film growth are presented. The authors would like to acknowledge productive interactions with colleagues at Agere, IBM, NCSU and Stanford. We also acknowledge the SRC/Sematech FEP Center and the NSF for financial support.

4:40pm **DI-MoA9 Hafnium Germanosilicate Thin Films for Gate and Capacitor Dielectric Applications: Thermal Stability Studies***,* ***S. Addepalli,*** *P. Sivasubramani, P. Zhao, M.J. Kim, M. El-Bouanani, B.E. Gnade, R.M. Wallace,* University of North Texas

The use of SiO@sub 2@-GeO@sub 2@ mixtures in gate and capacitor dielectric applications is hampered by the inherent thermodynamic instability of germanium oxide. Studies to date have confirmed that germanium oxide is readily converted to elemental germanium.@footnote 1,2@ In sharp contrast, germanium oxide is known to form stable compounds with transition metal oxides such as hafnium oxide (hafnium germanate, HfGeO@sub 4@).@footnote 3@ Thus, the incorporation of hafnium in SiO@sub 2@-GeO@sub 2@ may be expected to enhance the thermal stability of germanium oxide via Hf-O-Ge bond formation. In addition, the introduction of transition metal would simultaneously enhance the capacitance of dielectric thereby permitting a thicker dielectric, which reduces leakage current.@footnote 4@ In this study, the thermal stability and electrical properties of PVD-grown hafnium germanosilicate (HfSiGeO) films on Si(100) substrate were investigated. XPS, RBS, HR-TEM, C-V and I-V results for germanosilicate films after deposition and subsequent annealing treatments will be presented. Our results indicate that the thermal stability of the hafnium germanosilicate films is drastically affected not only by the presence or formation of elemental germanium during annealing, but also by the germanium content in the film. This work is supported by DARPA through SPAWAR Grant No. N66001-00-1-8928, and the Texas Advanced Technology Program. @FootnoteText@ @footnote 1@ W. S. Liu, J .S. Chen, M.-A. Nicolet, V. Arbet-Engels, K. L. Wang, J. Appl. Phys. 72, 4444 (1992), and, Appl. Phys. Lett. 62, 3321 (1993).@footnote 2@ W. S. Liu, M.-A. Nicolet, H.-H. Park, B.-H. Koak, J.-W. Lee, J. Appl. Phys. 78, 2631 (1995). @footnote 3@ P. M. Lambert, Inorg. Chem. 37, 1352 (1998).@footnote 4@ G. D. Wilk, R. M. Wallace and J. M. Anthony, J. Appl. Phys. 89, 5243 (2001).

Author Index

Bold page numbers indicate presenter

— A —
Addepalli, S.: DI-MoA9, **2**
Ashcraft, R.W.: DI-MoA6, 1
— B —
Bartynski, R.A.: DI-MoA7, 1
— C —
Chabal, Y.J.: DI-MoA7, 1
Chang, J.P.: DI-MoA1, **1**
— E —
El-Bouanani, M.: DI-MoA9, 2
— G —
Garfunkel, E.L.: DI-MoA7, **1**
Gnade, B.E.: DI-MoA9, 2
Goncharova, L.V.: DI-MoA7, 1
Gougousi, T.: DI-MoA6, **1**
Gustafsson, T.: DI-MoA7, 1
— K —
Kim, M.J.: DI-MoA9, 2
Kota, G.P.: DI-MoA5, 1
— L —
Labelle, C.B.: DI-MoA5, **1**
Lee, C.: DI-MoA5, 1
Lee, S.D.: DI-MoA5, 1
— N —
Nishimura, T.: DI-MoA7, 1
Niu, D.: DI-MoA6, 1
— P —
Parsons, G.N.: DI-MoA6, 1
— R —
Ramalingam, S.: DI-MoA5, 1
— S —
Sayan, S.: DI-MoA7, 1
Sivasubramani, P.: DI-MoA9, 2
Starodub, D.G.: DI-MoA7, 1
Stemmer, S.: DI-MoA3, **1**
— V —
Vahedi, V.: DI-MoA5, 1
Vanderbilt, D.: DI-MoA7, 1
— W —
Wallace, R.M.: DI-MoA9, 2
— Z —
Zhao, P.: DI-MoA9, 2
Zhao, X.: DI-MoA7, 1