

Thursday Afternoon, November 7, 2002

Plasma Science

Room: C-103 - Session PS-ThA

Dielectric Etch II

Moderator: A.P. Mahorowala, IBM T. J. Watson Research Center

2:00pm **PS-ThA1 Etching Reaction Mechanism of Organic Low-k Dielectric Employing High-Density Plasmas and Multi-Beams.** *M. Hori, H. Nagai*, Nagoya University, Japan, *M. Hiramatsu*, Meijo University, Japan, *T. Goto*, Nagoya University, Japan

An organic film, FLARE, is one of the most prospective candidates for interlayer insulating films with lower dielectric constant (low-k). N_2/H_2 and N_2/NH_3 gas plasmas have been used for etching organic low-k film without degrading the film quality and etch profile. The organic low-k film etching has been studied in ultrahigh frequency (UHF) plasma and inductively coupled plasma (ICP) employing N_2/H_2 and N_2/NH_3 gases. The absolute densities of H and N radicals were measured using the vacuum ultraviolet absorption spectroscopy (VUVAS) employing micro-plasma as a light source. N and H radical densities were estimated on the order of $10^{11} - 10^{12} \text{ cm}^{-3}$ and $10^{12} - 10^{13} \text{ cm}^{-3}$, respectively. The behavior of etch rate corresponded to that of H radical density. Therefore, H radicals were found to be important species for organic low-k film etching, while N radicals never etched without ion bombardments. To investigate the roles of radicals and ions from view point of fundamental reactions, the organic low-k film etching reaction was investigated using radical and ion beams. H and N radicals ($\approx 10^{10} \text{ cm}^{-3}$) were injected with changing the density under the irradiation of each ion (Ar^+ , N_2^+ , NH_4^+ , H_3^+) with an energy of 500 eV. The etch rate of organic low-k film was linearly increased with increasing H radical density, while suppressed drastically by N radical injection. The etched subsurface reactions of radicals were investigated by in-situ X-ray photoelectron spectroscopy (XPS) and fourier transform-infrared attenuated total reflection (FT-IR ATR). The etching reaction mechanism is discussed on the basis of results in plasma and multi-beam etching.

2:20pm **PS-ThA2 Modeling Dual Inlaid Feature Construction.** *P.J. Stout, S. Rauf, T. Sparks, D. Zhang, P.L.G. Ventzek*, Motorola

A reactor/feature physics based modeling suite has been applied to dual inlaid (DI) via first trench last (VFTL) feature construction. The reactor model is HPEM (developed at the University of Illinois) and the feature model is Papaya (developed at Motorola). Papaya, a 2D/3D Monte Carlo based feature scale model, includes physical effects of transport to surface, specular and diffusive reflection from surface, adsorption, surface diffusion, deposition, sputtering, etching, and crystal structure. Papaya is coupled to the reactor model through "atomic sources". The atomic sources are the identity, flux rate, angular distribution, and energy distribution of specie incident on the feature surface. The atomic sources are used by the feature model to predict feature evolution. The DI feature is used in inlaid copper interconnect construction to define metal lines and their connection to the metal layer below. The advantage of the DI feature is only one metallization step (barrier/seed/plating/CMP) is required to deposit metal into both the metal lines and the via connections to the metal layer below. The DI feature is constructed through a combination of etch, fill, and mask steps. Discussed will be the 3D feature modeling of fluorocarbon plasma etching of vias and trenches in SiO_2 to construct a VFTL DI feature. The significant feature effects have been simulated for the interaction of trench etch and etched via profile and the via protect fill material. Effects of feature geometry, via protect material level, and polymerization thickness on the final 3D DI feature profile will be discussed.

2:40pm **PS-ThA3 Profile Evolution During Fluorocarbon Plasma Etching of Low-k Porous Silica**¹. *A. Sankaran, M.J. Kushner*, University of Illinois at Urbana-Champaign

To achieve shorter RC-delay times in integrated circuits low-k dielectric materials are being investigated for interconnect wiring. Porous silica is a promising candidate. Profile evolution and maintenance of critical dimensions during plasma etching of porous silica are problematic due to the exposure of open pores. To investigate these issues, reaction mechanisms for fluorocarbon plasma etching of porous silicon-dioxide have been developed and incorporated into the Monte-Carlo Feature Profile Model (MCFPM) which was modified to address these two-phase systems. To focus on issues related to the morphology of porous materials, the porous silica in the model was treated as stoichiometric SiO_2 . Pores are randomly distributed in the SiO_2 to have a specified average pore radius and

volume fraction (porosity). Fluxes to the substrate were obtained from the Hybrid Plasma Equipment Model for inductively coupled plasmas sustained in CHF_3 , C_2F_6 and C_4F_8 . The surface reaction mechanisms for these chemistries were validated by comparison to experiments.² Etch rates and tapering of high aspect ratio features were investigated as a function of bias voltage and diluents (e.g., Ar). We found that etch rates for porous silica materials are generally higher than for SiO_2 even when accounting for the smaller mass density, though etch rates do not necessarily scale linearly pore size or porosity. Scaling parameters (e.g., more tapering with larger polymerizing fluxes) observed for solid SiO_2 are generally applicable to the porous materials. Removal of polymer from exposed pores was also investigated using O_2 plasmas.

¹Work supported by Semiconductor Research Corp. and National Science Foundation.

²Oehrlein et al. JVST A 17, 26 (1999); 18, 2742 (2000)

3:00pm **PS-ThA4 The Effect of Aspect Ratio on the Etching Properties of Porous Low-k Material in Fluorocarbon Plasma.** *S.H. Moon, S.-W. Hwang, G.-R. Lee, J.-H. Min*, Seoul National University, Korea

As the critical dimension of integrated circuit devices rapidly shrinks to sub $0.1\mu\text{m}$ range, micro-structures such as trench, contact and via holes have high aspect ratios and consequently the issue of the aspect-ratio-dependent-etching (ARDE) becomes important. In ARDE study, information about the surface properties of the sidewall and the bottom inside the features is important, but there are few studies about this, especially in low-k interlayer dielectric etching, because the direct analysis of the surface in real features is difficult. In this study, we used a Faraday cage, which allowed us to control the ion incident angle on the substrate, and investigated in macroscopic scale the change in the roughness and chemical composition of porous low-k silsesquioxane with the aspect ratio of trench-shaped structure after etching in CF_4 and CHF_3 plasmas. For the etching experiments, we placed trench structures made of porous silsesquioxane inside the Faraday cage, and the samples were processed at 4mTorr, 600W source power, and -100V bias voltage in TCP etcher. The sidewall height of the samples was fixed at 1cm and the bottom width was varied between 1mm and 1cm such that the aspect ratio of the trench structure was varied between 10 and 1. Etch rates of the bottom and the sidewall of the samples for different aspect ratios were correlated with their surface properties observed by AFM, AES, and FT-IR.

3:20pm **PS-ThA5 Etching of Porous Low-K Dielectric Films in Fluorocarbon Plasmas.** *S.A. Rasgon, B.E. Goodlin, H.H. Sawin*, Massachusetts Institute of Technology

To further reduce interconnect delay and enable higher device speeds (especially as the critical dimensions are lowered below $0.13\mu\text{m}$), it becomes advantageous to reduce the dielectric constant of the interlevel dielectric material between the metal lines. Porous low-k materials are potential candidates to meet this objective. While current research has focused on the material characterization of porous low-k films, little attention has been paid to the etching characteristics, of critical importance for process integration. Our research focuses on the etching characteristics and kinetics of leading candidate porous low-k dielectric films in fluorocarbon chemistries. Etching characteristics of these films are simultaneously compared with OSG, SiO_2 , $SiC(N)$, and photoresist films to reveal similarities and differences in etching behavior, and selectivity toward mask and stop layers. Ellipsometric results on porous low-k films indicate a possible competition between diffusion of etching precursors into the porous matrix, and ion-enhanced etching. Specifically, at low DC bias voltages, we note what appears to be a mixed fluorocarbon/porous-low k layer, possibly several hundred Å deep. As DC bias is increased, the mixed layer thins, and disappears around 300 V DC bias. This mixed layer is not present on OSG or SiO_2 samples etched at the same conditions. XPS studies will confirm these results. Understanding these etching behaviors may provide valuable insight into solving the problems of damage to the dielectric constant of porous low-k films, and reverse - selectivity during etching of the stop layer.

3:40pm **PS-ThA6 Plasma Etching Chemistry and Kinetics for Low-k and Porous Low-k Dielectric Films.** *W. Jin*, Massachusetts Institute of Technology

To further reduce interconnect delay and enable higher device speeds, especially as the critical dimensions are lowered below $0.13\mu\text{m}$, the interlevel metal insulator material with dielectric constant as low as 2.0 is desired. Porous materials, which lower the dielectric constant as a result of mixing air with the solid phase, are potential candidates to meet the low dielectric constant objective. Current research is focused on the material characterization, but little attention has been paid to its etching

characteristics, although they are critical for process integration. In this research, we have measured etching rates of both porous low-k and low-k (OSG) as functions of ion bombardment energy, ion impinging angle with various fluorocarbon plasma beams, which are necessary for profile evolution modeling of porous low-k etching in inductively coupled plasma. In this work, ions and neutrals are extracted directly from plasma to the main chamber evacuated by a cryo-pump. Surface reaction is studied by measuring etching rate with an ex-situ spectroscopic ellipsometer. At the same time, ion and neutral composition of the plasma is determined with mass spectrometer. And surface composition is analyzed by an X-ray photoelectron spectroscopy. The possible reasons attributing to the difference of the etching behavior between porous low-k and low-k dielectric films has been studied.

4:00pm **PS-ThA7 In Situ Real Time Monitoring of Evaporation Induced Self-Assembly and Patterned Etching of Low-k Mesoporous SiO₂ in Fluorocarbon Plasmas**, *H. Gerung, C.J. Brinker, S. Han* University of New Mexico

We have investigated in situ and in real time the sol condensation and the plasma-assisted patterning of mesoporous low-k SiO₂ films, using attenuated total reflection Fourier transform infrared spectroscopy. The porous SiO₂ films are prepared by evaporation induced self-assembly (EISA). The evaporation of ethanol in the sol induces self-assembly of surfactants to form an ordered cubic-phase template. Around this template, tetraethylorthosilicate (TEOS) condenses to create a silica network. The template is subsequently removed by calcination, resulting in a cubic phase mesoporous SiO₂ film. To better understand the condensation sequence, we have monitored the dichroic ratio of Si-O-Si IR absorbance during EISA and examined the propagation of Si-O-Si bond formation for varying film thicknesses. Thus formed porous SiO₂ films, stacked with a patterned photoresist, are etched in an inductively coupled plasma reactor, using CHF₃ and Ar. During etching, the integrated IR absorbance by Si-O-Si asymmetric stretching modes near 1080 cm⁻¹ decreases while that of C-F_x (x = 1, 2, or 3) stretching modes near 1300 cm⁻¹ continues to increase. The rate of decrease in integrated Si-O-Si absorbance translates to the SiO₂ removal rate. When corrected for the exponentially decaying evanescent electric field, the removal rate helps monitor the evolution of the etch profile in real time. We attribute the increasing integrated absorbance to the formation of C-F_x species along the sidewall of patterned SiO₂ trenches. The stretching vibrational modes of carbon-carbon double bonds (C=C) are not observed near 1700 cm⁻¹. The absence of C=C absorbance with the presence of C-F_x absorbance indicates that the sidewall passivation maintains a steady state thickness. We intend to exploit the SiO₂ removal rate and the observed nature of sidewall passivation to predict the etch profile.

4:20pm **PS-ThA8 The Control of the Etching of SiOCH Films using C₄F₈/Ar/N₂ Plasma**, *T. Tatsumi*, Sony Corporation, Japan, *K. Urata*, Sony Computer Entertainment, Japan, *K. Nagahata*, Sony Corporation, Japan, *S. Iseda*, Sony Computer Entertainment, Japan, *Y. Morita*, Sony Corporation, Japan

The relationship between the etch rates, C-F polymer thickness and the incident fluxes in dual-frequency (60/2MHz) RIE was evaluated by using various in-situ measurements tools, such as IRLAS and OES. To vary the amount of incident CF_x species, the C₄F₈ partial pressures in the C₄F₈/Ar/N₂ (or O₂) was increased under a gas pressure of 75 mTorr and a V_{pp} of 2000 V. The C-F polymer thickness increased when the incident CF_x fluxes were relatively higher than the removal ability of the C-F polymer; that mostly depends on the O and N fluxes (including the O outflux from etched SiOCH). SiOCH films have some methyl groups in the Si-O network and their densities are lower than SiO₂. Comparing to SiO₂ etching, the outflux of O decreased while additional C from the etched surface of SiOCH was supplied to the C-F polymer layer. The difference in outfluxes between SiO₂ and SiOCH drastically changed the process window for the selective etching. We found that the optimum etching condition could be obtained below the "critical point" P_c, where the total C flux became equivalent to O and N total fluxes. We have to carefully control the partial pressure and dissociation degree of C₄F₈ according to the density, composition and aspect ratio of the SiOCH sample and thus find the P_c at which the maximum etch rate can be obtained. This is because the process window is very narrow and slight change in radical fluxes can induce phenomena such as residues and etch stop that cause serious problems with etching performance.

¹T. Tatsumi et al., Proceedings of 22nd Symposium on Dry Process (2000) 37.

4:40pm **PS-ThA9 SiO₂ Etch Lag in SiO₂/SiLK™/SiO₂ Stack Structures**, *A. Hasegawa, K. Ohira, T. Mizutani*, Fujitsu Limited, Japan, *K. Higuchi*, Fujitsu Vlsi Limited, Japan, *M. Okamoto, M. Nakaishi, K. Nakagawa*, Fujitsu Limited, Japan

The etching of stack structure using hard-mask became indispensability by the adoption of the dual damascene process and organic low dielectric

constant (k) material for Cu wiring. In this study, SiO₂ etch lag effect depending on existence of SiLK™ layer in stack structure is investigated. SiLK™ is low-k organic dielectrics considered as perspective candidates for the use in microelectronic industry. The sample used in this experiment consists of SiN/upper SiO₂/SiLK™/lower SiO₂ stacked structure. SiN was used for hard-mask to etch SiO₂. Upper SiO₂ was used for cover layer to protect SiLK™ damage during ashing and/or planarization by chemical mechanical polishing. After SiN trench etch, SiN/upper SiO₂/SiLK™ were etched using hole patterned photoresist mask. Photoresist mask was removed during SiLK™ etch. Then, trench pattern of upper SiO₂ and via pattern of lower SiO₂ were etched at the same time using the patterned SiN/upper SiO₂/SiLK™ layers. The etching of the upper and lower SiO₂ were performed in commercial UHF plasma reactors using a C₃F₈/Ar/O₂ chemistry. The lower SiO₂ etch depth was measured from cross-sectional-scanning-electron-microscopy (SEM) photographs. The etch rate of dense via was 284nm/min. On the other hand, in the isolated via, the etch rate was only 91nm/min. However, in the case of using the stack sample, which was replaced SiLK™ with SiN, etch rate of dense and isolated via were equivalent at 282nm/min. It was found that existence of SiLK™ decreases the SiO₂ etch rate of a particular via pattern remarkably.

5:00pm **PS-ThA10 Etch Process Development of Porous Low-k Dielectrics for Dual Damascene Copper Interconnects**, *K.D. Brennan* Texas Instruments, *J.M. Jacobs*, Philips, *P.J. Wolf*, Intel

Advances in plasma etch technology are necessary to integrate low-k dielectrics and low-resistance metal leads to reduce interconnect RC time delay in order to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). International SEMATECH (ISMT) is currently implementing dual damascene copper interconnects built with porous low-k dielectrics as a means to meet future interconnect requirements. Development and optimization of an etch process for JSR LKD 5109, a porous methyl-silsesquioxane (pMSQ) based dielectric with a k-value of 2.2 is presented. Two level metal interconnects are fabricated, using a dual hard mask approach. The advantages and limitations of this approach for the etch process are discussed.

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