Monday Morning, November 4, 2002

Plasma Science
Room: C-105 - Session PS-MoM

Conductor Etch I
Moderator: S. Han, University of New Mexico

8:20am **PS-MoM1 The Evolution of Plasma Etching in Integrated Circuit Manufacturing**, ***J.W. Coburn***, University of California, Berkeley **INVITED**

Anisotropic plasma etching methods were introduced into semiconductor manufacturing in the late 1970s. The notion of using reactive gas glow discharges to etch solid materials had been described much earlier but it was not until the mid 1970s that the anisotropic etching capabilities of plasma etching were recognized. At this time, it was understood that the requirements for anisotropic etching were both energetic ion bombardment of the surface being etched and an exothermic chemical reaction between the gas phase reactants and the surface that form a volatile reaction product. Early plasma etching systems were primarily capacitively coupled, single frequency diodes with either planar or cylindrical geometry. In order to achieve the desired etch rates, relatively high energy (0.5 to 1 keV) ion bombardment of the surface being etched was required. However this bombardment tended to reduce etch selectivities and increase wafer damage. Furthermore, the plasma potential in capacitively coupled systems can exceed 100 volts, resulting in high energy ion bombardment and sputtering of grounded surfaces; a possible source of wafer contamination. These issues were addressed by separating the plasma generation from the wafer bias. During the early 1980s, single frequency and dual frequency triodes were popular. Later in the 1980s, inductively coupled and wave-generated plasma sources were introduced. These sources allowed the generation of high density plasmas (10^{11} to 10^{13} electrons/cm^3) which, when combined with a relatively low power capacitively coupled chuck, allowed high etch rates to be achieved with relatively low ion energies (50 - 200 eV). Today, each wafer is exposed to a plasma etching environment between 10 and 20 times during its manufacture and without the highly anisotropic etching provided by this critical process, high density IC manufacturing would not be possible.

9:00am **PS-MoM3 Resist Transformation under High Density Plasma Exposure**, ***E. Pargon***, *J. Foucher, J. Detter, L. Vallier, G. Cunge, O. Joubert*, CNRS/LTM, France, *Th. Lill*, Applied Materials

We are now entering in the development of sub 0.1 µm Integrated Circuits device fabrication where a very accurate control and understanding of plasma processes is essential to address the road map requirements. In particular, plasma processes involved in gate stack processes need special attention since several steps such as resist trimming, hard mask opening and silicon etching impact the final gate dimension. In any of these processes, the etching behaviour of photoresist exposed to the plasma plays a key role. In this study, we have performed chemical topography analyses using XPS to explore the chemical nature and thickness of the reactive layers formed on the resist patterns. XPS analyses show that the resist transformation during the resist trimming process is well correlated with the trim rate measured in HBr/O_2 and $HBr/Cl_2/O_2$ /CF_4 chemistry. In particular, a decrease in trim rate obtained when increasing the bias power is well correlated with a thicker perturbed layer formed on the resist sidewalls. A good correlation between reactive layer thickness on the sidewalls and decrease in trim rate is also observed with CF_4 addition. CF_4 based plasmas used for hard mask opening generate reactive layers as thick as 10 nm on the resist sidewalls (through the formation of a CFx-based layer). This layer is suspected to generate a loss of CD control during hard mask patterning. Deep transformations of the resist during silicon gate etching are also observed. XPS studies show that the resist mask strongly loads chlorine species as compared to an oxide hard mask and that thick passivation layers are formed on the resist sidewalls using $HBr/Cl_2/O_2$ and $HBr/Cl_2/O_2/CF_4$ chemistries. Correlations between resist behaviour and process control (mainly CD control) can be established

9:20am **PS-MoM4 A Novel Gate-Electrode Fabricating Technique using a Sequential UHF-ECR Plasma Process**, ***M. Mori***, Hitachi, Ltd.,Japan, *T. Tsutsumi*, Hitachi High-Technologies Corp.,Japan, *N. Itabashi*, *M. Izawa*, Hitachi, Ltd.,Japan

For fabricating beyond 90 nm-node devices, ArF lithography will be increasingly used. This process demands that the gate electrode must be trimmed more than 50 nm after lithography and critical dimension (CD) shift variation must be suppressed within 3-5 nm across the wafer. However, gate-electrode trimming of more than 50 nm using only ArF trimming is difficult, because the resist is too thin or bent in followed hard-mask etching. Therefore, we have developed a sequential gate process consisting ArF/polySi trimming that uses a UHF-ECR plasma. This plasma has capability to precisely CD-shift control, because of its moderate ion-current flux (ICF) at low pressure and its by-product uniformity control.[1] In polySi trimming, we evaluated the vertical undercut process. By using this process, we can measure gate-length with a CD SEM after wet etching. For vertical undercut process, we used multi-step etching, consisting a polySi main etching step with a thin side-wall protection film, followed by a highly selective trimming step. The amount of trimming could be controlled by the time of trimming step, and 86.5±1.5 nm trimming was obtained without punching through in a 2.5-nm gate-oxide layer. Regarding ArF trimming, it was confirmed that O_2 containing gas chemistry provided good hard-mask selectivity and good linearity of time control. Trimming - rate variation across the wafer was within 2.7 nm/min. To suppress resist bending in hard-mask etching, the vertical/horizontal etching rate ratio was controlled in ArF trimming, and CHF_3 based gas chemistry was used for the hard-mask etching. This good linearity of CD control with time in ArF/polySi trimming will be caused by UHF-ECR plasma that has more moderate ICF and less interaction with the reactor wall.

[1] M. Mori, et al., (2000), Proceeding of Solid State Devices and Materials, p. 192.

9:40am **PS-MoM5 Impact of Chemistry and Mask Nature on Critical Dimension Control of Gate Etch Processes**, ***X. Detter***, STMicroelectronics, France, *G. Cunge, E. Pargon, L. Vallier, O. Joubert*, CNRS/LTM, France, *R. Palla, I. Thomas-Boutherin*, STMicroelectronics, France

During a CMOS gate etch process, requirements in terms of Critical Dimension (CD) bias and microloading are more and more severe. Since gate etch processes are composed of several steps (resist trimming, BARC and probably hard mask opening, poly-silicon main etch step, soft landing step (to preserve the gate oxide) and over-etch step), a good understanding of the mechanisms influencing the CD deviation is necessary for each of them. During a classical poly-silicon gate etch process, passivation layer deposition on the gate sidewalls is known to be one source of CD microloading and the main source of CD bias for isolated patterns. However, as the aspect ratio is increasing, the profile evolution is more complicated and may be influenced by loading and shadowing effects as well as charging effects. Indeed, the passivation layer formation results from deposition of inhibitors and etching by radicals which are both strongly influenced by the nature of the mask and total aspect ratio of the structure. In this talk, we present a study of profile evolution during the poly-silicon etch steps with a resist and an oxide hard mask. Aspect ratio dependent etching and passivation layer deposition mechanisms are investigated for chemistries used in today's gate etch processes : $HBr/Cl_2/O_2$ and $HBr/Cl_2/O_2/CF_4$. Loading and shadowing effects induced by the mask are more precisely investigated (in a range of aspect ratio varying from less than 0.1 to more than 3 and a minimal space between lines of 60 nm). A correlation with X-ray Photoelectron Spectroscopy analysis of passivation layers composition and emission spectroscopy of by-products present in the gas phase is also performed. Finally, the limits of the current processes and potential strategies for future gate etch processes are discussed.

10:00am **PS-MoM6 Deposition of Silicon Oxychloride Films on Chamber Walls during Cl_2/O_2 Plasma Etching of Si**, ***S.J. Ullal***, *H. Singh, V. Vahedi*, Lam Research Corporation, *E.S. Aydil*, University of California, Santa Barbara

Chlorine plasma etching of silicon is widely used in gate etching and shallow trench isolation. During etching, the silicon chloride etch products react with oxygen present in the plasma to deposit a glassy silicon oxychloride film on the chamber walls. The chemical nature and deposition rate of the silicon oxychloride films deposited on the chamber walls during Cl_2/O_2 plasma etching of Si were investigated using multiple total internal reflection Fourier transform infrared (MTIR-FTIR) spectroscopy. The differences in the infrared spectra of films deposited under different etching conditions were quantified through the Si-O and OSi-Cl absorption band intensities and positions to determine the growth rate and composition of these films. The changes in the film's deposition rate and composition with rf bias power and O_2 flow rate gave insight into the deposition mechanism. Based on our experimental observations, we propose that the silicon oxychloride film is deposited through oxidation of $SiCl_x$ ($0 \le x \le 4$) molecules adsorbed on the reactor walls and suggest a kinetic expression for the film deposition rate. This kinetic expression may also be used judiciously for describing the silicon oxychloride deposition on the sidewalls of etched features in gate etching and shallow trench isolation.

10:20am **PS-MoM7 HBr Outgassing and Condensation from Silicon and Polysilicon Wafers after Plasma Etching**, ***H. Singh***, *D. Outka, J.D. Daugherty*, Lam Research Corporation

HBr gas is commonly used in dry etching of poly-silicon gate structures and in shallow trench etching since HBr-rich etch chemistry provides good profile control and high selectivity to gate oxide. As a result, the surface of wafers in many silicon etch processes are bromine terminated at the end of plasma etching. Subsequently, HBr outgasses from etched wafers upon exposure to atmosphere. HBr also condenses on the etched wafer and neighboring wafers in the form of HBr-hydrate and bromine-hydrate. HBr and bromine hydrates crystals are stable at ambient conditions. The timescale for HBr outgassing and condensation varies from few seconds to days, depending on the etch and ambient conditions (e.g. humidity). HBr outgassing and condensation also occurs on bare silicon wafers commonly used to condition plasma etchers before etching production wafers. The re-use of these bare silicon wafers results in micro-masking of the wafer by the HBr-hydrate crystals, resulting in formation of silicon pillars on the wafer. The micro-masking of the wafer results in formation of so-called "black silicon" rendering the wafer unusable. Various methods investigated to minimize the outgassing and condensation of HBr on wafers, including the heating of the wafer in vacuum, heating the wafer after exposure to atmosphere, and treating the wafer with oxygen plasmas, show limited success in removing bromine from the wafer surface. Separation of unetched and etched wafers on the etcher is the most effective method of eliminating micro-masking of unetched wafers. For bare silicon wafers, post treatment of the wafer with fluorine plasma is an effective way to remove the bromine from the wafer. A phenomenological model explaining the processes involved is presented, elucidating the role of chemisorbed and physisorbed bromine on the wafer.

10:40am **PS-MoM8 Energetic Neutral Fluxes Towards Surfaces in a MERIE Like Reactor**, ***W. Sabisch***, *M. Kratzer*, Infineon Technologies AG, Germany, *R.P. Brinkmann*, Ruhr University Bochum, Germany

In VLSI microelectronics fabrication Magnetically Enhanced Reactive Ion Etch (MERIE) reactors are established for many dry etch processes. One example is the etch of high aspect ratio capacitor trenches.[1] For feature scale profile evolution the angularly and energetically resolved distributions of the surfaces incident particles (ions and neutrals) as well as the fluxes of ions and neutrals play an essential role. Butterbaugh et al.[2] showed that the etch yield for the selective SiO_2 / Si etch is strongly influenced by the ratio of neutral to ion fluxes. The focus of this work is set on the calculation of the neutral to ion fluxes ratio. Therefore the MERIE reactor's boundary sheath is simulated by the TCAD simulation tool Hybrid Plasma Sheath Model (HPSM).[3,4] HPSM consists of a self-consistent coupling of a fluid dynamical part to a Monte-Carlo part. Sheath and presheath region are described in one unified model. Energetic neutrals impinging the surface can be monitored in addition to the positive ion species. Presented are simulations with parameters typical for a trench etch with pressures in the range of about 100 mTorr, rf voltages of a few 100 Vs, magnetic fields of about 100 Gauss and plasma powers of about 1000 W. The simulations show that the flux of the energetic neutrals compared to the flux of the ions is not neglectable and that the neutral flux gives an important contribution to the energy budget of the surface impinging particles.

[1] J. Bondur, R. Bucknall, F. Redeker, and J. Su: Proc. of the SPIE 1992, vol. 1803, pp. 45ff

[2] J.W. Butterbaugh, D.C. Gray, and H.H. Sawin: JVST B, vol. 34, 1991, pp. 1461ff

[3] M. Kratzer and R.P. Brinkmann: The IEEE Int. Conf. on Plasma Science 2000, 3D03

[4] M. Kratzer, R.P. Brinkmann, W. Sabisch, and H. Schmidt: JAP, vol. 90 (5), 2001, pp. 2169 ff.

11:00am **PS-MoM9 ICP Etching of Poly-crystalline Si-Ge as a Gate Material**, *K.M. Tan*, ***W.J. Yoo***, *W.K. Choi, Y.H. Wu, J.H. Chen, D. Chan*, National University of Singapore

In recently years, silicon germanium ($Si_{1-x}Ge_x$) is receiving significant attention as a candidate gate material to replace polycrystalline silicon, since Si-Ge can have advantages over poly-Si in achieving small threshold voltage and high trans-conductance required in sub 100 nm CMOS devices. In this work, we wish to demonstrate etching properties of the $Si_{1-x}Ge_x$ films using an inductively coupled plasma. The polycrystalline $Si_{1-x}Ge_x$ films were deposited by sputtering at 250°C and annealed at 900°C subsequently. The amount of Ge in the $Si_{1-x}Ge_x$ films varied from 10% to 60% by changing the sputtering target. According to preliminary results obtained using ICP of CF_4+H_2, the etching rates were strongly dependent on the amount of Ge in the $Si_{1-x}Ge_x$ films. The maximum etching rate was obtained at the chamber pressure of 20mTorr: 2.2 µ/min at 60% Ge and of 0.9 µ/min at 10% Ge when an inductive RF power of 1000W was applied. The etching rates were increased almost linearly as a function of %Ge. We were able to obtain anisotropic etching profiles over the entire experimental range of %Ge, despite that photoresist profiles prior to the ICP etching were not anisotropic. To control critical dimension of gate structures precisely and to obtain high selectivity with respect to thin oxide under-layer, we propose etching mechanisms of $Si_{1-x}Ge_x$ gates in ICP using Cl_2, HBr, and O_2, and also reveal their sidewall passivation properties.

11:20am **PS-MoM10 Endpoint Strategies for Recess Etch Processes in DRAM and eDRAM Applications**, *J.P. Merceron*, Ecole Polytechnique, France, ***V.C. Venugopal***, *A.J. Perry, A.J. Miller*, Lam Research Corporation

Developing a robust and reliable strategy to determine the end point of recess etch processes for DRAM and eDRAM applications presents some unique challenges. These processes involve etching the poly-Si back-filled into trenches in a Si substrate. The tight depth control required necessitates accounting for incoming material variations, mask erosion, and variations in the densities of incoming patterns. In addition, if an optical diagnostic tool such as an interferometer is used, the high aspect ratio structures and low open area lead to low signal levels, low fringe contrast and signal noise. Incoming nitride mask thickness could vary depending on the planarization process used (either CMP or etch) and the device being fabricated. Target depths are usually specified with respect to the bottom of the nitride layer. The starting recess depth (after planarization) is usually not known either. These uncertainties necessitate measurement of the starting nitride thickness as well as the initial recess depth to achieve the required accuracy. We have developed a robust endpoint strategy based on a broadband (UV-VIS-NIR) reflectometer, adapted to provide a high signal-to-noise ratio (SNR), to achieve the desired degree of control for recess etch processes. The broadband reflectance spectrum carries sufficient information to be able to determine the starting parameters of interest. The evolving recess structure causes a discernible modulation of the reflected light from the wafer, especially at short wavelengths (typically <300nm). A robust fringe counting method which accounts for mask erosion and etch rate variations but is insensitive to signal noise is then used to determine the change in depth of the recess relative to its initial value.

11:40am **PS-MoM11 Numerical Model of a Cl_2-BCl_3 Metal Etch Reactor**, ***G.I. Font***, *W.L. Morgan*, Kinema Research

Plasmas containing Chlorine (Cl2) and Boron trichloride (BCl3) are used in the patterning of interconnects during integrated circuit manufacturing. Optimization of the plasma uniformity in the reactor is important for the purpose of accurate pattern transfer across the entire wafer. Optimization, however, requires understanding of the influence of the reactor variables (power, pressure, and geometry) on the plasma chemistry. Simulation can aid in providing understanding of metal etch reactors by providing insight into the relative importance of chemical path ways and their dependence on reactor external variables. We have developed a chemical model for an Ar, BCL3, Cl2 discharge. Comparisons with experimental measurements inside a commercial reactor demonstrate good agreement with plasma density and electron temperature. The model also captures the plasma density distribution across the reactor and the dissociation characteristics with respect to pressure. Results below 10 mTorr suggest that parent negative ions may play an important role in the discharge.

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