Plasma Science
Room: C-105 - Session PS+MM-WeA

Feature Profile Evolution /Plasma Processing for MEMS
Moderator: A. Kornblit, Bell Labs, Lucent Technologies

2:00pm **PS+MM-WeA1 Plasma Molding Over Trenches and Resulting Ion/Fast-neutral Distribution Functions**, ***D. Economou***, *D. Kim**, University of Houston

Plasma molding over surface topography finds applications in MEMS microfabrication, neutral beam sources, plasma extraction through grids, and plasma contact with internal reactor parts (e.g., wafer chuck edge). The flux, energy and angular distributions of ions incident on the substrate are of primary importance in these applications. These quantities depend critically on the shape of the meniscus (plasma-sheath boundary) formed over the surface topography. When the sheath thickness is comparable to or smaller than the feature size, the sheath tends to "mold" over the surface topography. A two-dimensional fluid/Monte Carlo simulation model was developed to study plasma "molding" over surface topography. The radio frequency (RF) sheath potential evolution, and ion density and flux profiles over the surface were predicted with a self consistent fluid simulation. The trajectories of ions and energetic neutrals (resulting by ion neutralization on surfaces or charge exchange collisions in the gas phase) were then followed with a Monte Carlo simulation. Ion flow and energy and angular distributions of ions and energetic neutrals bombarding the walls of a trench will be reported. Emphasis will be placed on high aspect ratio features of interest to MEMS and neutral beam sources. Simulation results will be compared with experimental data, taken at Sandia National Labs, on ion flux and ion energy and angular distributions at the bottom of trenches. Work supported by the National Science Foundation and Sandia National Laboratories.

2:20pm **PS+MM-WeA2 Physically Based Modelling of High-Density-Plasma-CVD on the Feature Scale**, ***G. Schulze-Icking***, *A. Kersch*, Infineon Technologies AG, Germany, *A. Knorr*, Infineon Technologies, *A. Hausmann*, *J. Radecker*, Infineon Technologies Dresden GmbH & Co. OHG

Due to its low thermal budget and its highly directional deposition HDP-CVD of SiO2 has become an important process in IC fabrication. In order to study (and ultimately improve) the HDP-CVD process we have developed a physically based model for feature scale simulations. This model has been implemented into our custom Topography Simulator "Topsi" and extensive studies of the HDP-CVD process have been performed. In this presentation we give a survey of our simulation results and compare them to experiments. The model we propose retains the characteristics of a complex reactor scale model published by Meeks et al.[1] and extends it to the feature scale. A key aspect of both models is a "structural passivation" of the surface due to the chemisorption of gas phase precursors. In contrast to conventional CVD (at much higher temperatures) in HDP-CVD this passivation is removed by cations striking the surface. Accordingly ions not only sputter surface material but also are responsible for its directional deposition. The final topography therefore is the result of simultaneous neutral deposition/passivation, ion induced activation, and sputtering. It is well known[2] that the sputtering yield crucially depends on the ion energy and the angle of incidence. This probably also applies to ion induced surface activation, but very little is known about its energy and angular dependence. We therefore have performed deposition experiments and compared the final topography to simulations performed using our new model. With the derived set of parameters we are now able to predict the surface evolution as a function of process conditions. This is a major improvement over a more empirical model proposed by Conti et al.[3]

[1] E.Meeks et al.; J.Vac.Sci.Techn. A, 16, pp 544 (1998)
[2] C.Abrams et al.; J.Vac.Sci.Techn. A, 16, pp 3006 (1998)
[3] R.Conti et al.; DUMIC Conference (1999).

2:40pm **PS+MM-WeA3 Micro- and Nano-Fabrication Technology for High Aspect Ratio Micro-Electromechanical Systems (MEMS)**, ***S.W. Pang***, The University of Michigan **INVITED**

For many applications in micro-electromechanical systems (MEMS), having high aspect ratio sensors or actuators can improve performance, increase sensitivity, and lower power consumption. Micro- and nano-fabrication technology can be used to generate these high aspect ratio MEMS. Etch rate, profile, selectivity, and uniformity could vary as aspect ratio becomes higher since plasma etching characteristics depend on aspect ratio of microstructures. These variations could affect MEMS performance. In this talk, key issues to provide precise control in MEMS fabrication by plasma processing will be discussed. High aspect ratio MEMS including micromirrors for optical switching arrays, submicrometer resonators for accelerometers, sharp tips for emitters or scanning probes, and microheaters for micro-gas chromatography systems will be reviewed.

3:20pm **PS+MM-WeA5 Critical Tasks in the High Aspect Ratio Silicon Dry Etching for MEMS**, ***I.W. Rangelow***, University of Kassel, Germany **INVITED**

Microscopically uniform anisotropic etching of semiconductor layers is a critical step in ME(O)MS and ULSI circuit fabrication. The non-ideal etched feature limits density, yield and reliability of these devices. Artefacts such as RIE-lag, notching, sidewall bowing, micro-trenching, and mask facetting are typically accompaniment effects occurring during the etching high aspect ratio features in silicon. Because etch rates and the shape of etched features depend on circuit layouts-design, considerable effort have to be spent in the near feature to understood all common single and simultaneous phenomena during the high aspect ratio dry etching. The development of effective manufacturing processes requires a fundamental understanding of the factors, which determine etched feature shape. Gas reactivity, pressure (affecting ion bowing in the sheath due to scattering with neutrals), ion, electrons and reactant transport to the surface, and product transport away from the surface, have been identified as the key factors that control the microscopic etching uniformity in high aspect ratio etching. The choice of these can cause numerous secondary aspect ratio-dependent effects. The modelling of the most significant effects as RIE-lag, notching, bowing, facetting, micro-trenching, profile shape dependence etc. will be discussed.

4:00pm **PS+MM-WeA7 Deep Silicon Etch Profile Control for Micro-Sensor Applications**, ***R.J. Shul***, *M.G. Blain, S.G. Rich, S.A. Zmuda, C.G. Willison, R.P. Manginell*, Sandia National Laboratories

The ability to etch deep, high-aspect ratio, anisotropic, Si features has opened up new areas of application for microelectromechanical systems (MEMS) devices, as well as revolutionized the conception and implementation of "mixed technology" integration. For example, a fully integrated microsystem could include sensors, actuators, electronics, fluidics, and optics in a variety of material systems on a single chip or in a single package. Fabrication of such structures often requires profile control, multi-level etched features, and the ability to form freestanding membrane structures. For example, Si deep reactive ion etch (DRIE) has been used to fabricate a gas chromatographic (GC) separator as part of a micro-chemical analysis system (µChemLab™) used for the detection of trace concentrations of gas phase analytes. Maintaining uniform, controlled flow dynamics to optimize device performance requires well-controlled etch profiles and smooth etch morphologies. We will report on the use of the DRIE platform to fabricate anisotropic GC columns 100 µm wide, 400 µm deep with 25 µm walls. To improve the separation sensitivity of the GC columns, a new GC design that incorporates 50 µm diameter posts on 80 µm pitch located within 500 µm deep GC columns has recently been fabricated. A new DRIE process was developed to etch these features using parameter ramping, varying reactive gas flow, pressure, and ion energy. The profiles were very anisotropic with smooth features. The use of parameter ramping as well as multi-level masking processes to meet the challenges of advanced micro-sensor designs will be discussed. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-ACO4-94AL85000.
.

4:20pm **PS+MM-WeA8 Profile Control as a Function of Process Parameters in Deep Anisotropic Etching of Silicon**, ***M.L. Steen***, *T.J. Dalton*, IBM T.J. Watson Research Center

Deep etching of silicon is integral to the fabrication of microcomponents for microelectromechanical systems (MEMs). New commercially-available etching tools from several manufacturers are capable of deep silicon etching beyond 300 µmm. These systems offer the time multiplexed deep etching (TMDE) technique developed and licensed by Robert Bosch Gmbh, which uses alternating etching and deposition cycles for anisotropic etching of deep silicon structures. During the deposition step, sidewalls are passivated by a polymer deposited from a C_4F_8 discharge. During the subsequent etching cycle flowing only SF_6, both the polymer and silicon are preferentially etched from the base of the trench by ion bombardment. Accurate control of the depth and anisotropy of etched structures is

* PSTD Coburn-Winters Student Award Finalist

achieved by a fine balance between deposition and subsequent removal of the passivating layer. Processes are well controlled and many types of MEMS devices, such as pressure sensors and accelerometers, are produced using this technology. We are interested in expanding the number and scope of applications using deep silicon etching. Many of these applications have additional demands on surface morphology including minimization of the scalloping observed on vertical sidewalls during TMDE and the roughness of surfaces exposed to the discharge. Moreover, mask undercut and bowing of the etch profiles must be reduced to tailor the slope of etch profiles. Our goal is to understand the evolution of these traits as a function of operating conditions. Toward this goal, a number of process variables were explored using a commercial inductively-coupled plasma etcher. We report a significant increase in the silicon etching rate, minimization of mask undercut, and substantial reduction in bowing. These improvements demonstrate enhanced process performance and flexibility to meet a broad range of needs in deep silicon etching.

4:40pm **PS+MM-WeA9 Mechanisms Involved in the Silicon Cryogenic Etching Process**, ***M. Boufnichel***, GREMI / ST Microelectronics, France, *P. Lefaucheux, R. Dussart,* GREMI, France, *P. Ranson*, GREMI-Universite d'Orleans-CNRS, France

In this study, we investigated the etching and passivation mechanisms involved in the deep cryogenic etching of silicon trenches. More precisely, we studied the dependence of sticking coefficient of oxygen and fluorine as regards to wafer temperature. We showed that fluorine radicals sticking coefficient does not strongly depend on wafer temperature at the contrary to oxygen radicals. XPS measurements allowed us to obtain further informations concerning the nature and behaviour of the passivation layer deposited on trench sides during the cryogenic silicon etching with a SF_6/O_2 mixture. XPS measurements pointed at the fact that the passivation layer formed during the cryogenic etching of silicon is not mainly composed of SiO_2 species. Furthermore, a new method has been employed to determine the effective angular dispersion of ions (EIAD) involved in the etching of silicon and its impact on trench etching evolution. A comparison of the performances of RF and LF bias generators has also been performed so as to highlight the impact of bias-frequency on profile characteristics. A complete study of the etching mechanisms would not have been possible without parallel measurements of physical plasma parameters using Langmuir probe and actinometry with Optical Emission Spectroscopy (OES). The parallel between the etching experiments and diagnostics measurements shows for example that local bowing seems to depend on ion local surface bombardment and passivating mechanisms. Finally, we are able to etch deep anisotropic trenches (100 microns deep and 2 microns in aperture) at a high etch rate, high selectivity (SiO_2 mask) and high anisotropy. We performed to reduce or eliminate defects such as local bowing, undercut and notching for different application: etching of HARTs (High Aspect Ratio Trenches), LARTs (Low Aspect Ratio Trenches), vias, SOI (Silicon On Insulator) layers.

5:00pm **PS+MM-WeA10 3-Dimensional Feature Profile Evolution Using Level Set Methods**, ***H. Hwang***, *T.R. Govindan, M. Meyyappan*, NASA Ames Research Center

Modeling feature profile evolution due to etching of semiconductor materials is typically done in two dimensions. However, these 2-D simulations make assumptions about geometries, such as semi-infinite trenches, that are unrealistic. Since a semi-infinite trench will "collect" higher amounts of fluxes than a finite one, the calculated ion and neutral fluxes to the surfaces in 2-D will not account for the shadowing of the opening due to the finite size. These larger fluxes will then lead to a larger overall etch rate, compared with calculations done in 3-D. Furthermore, any asymmetries (due to ion angular distribution functions, for example) can only be captured in 2-D. Inherently 3-D situations, such as striation patterns of the trenches, cannot be studied without the third spatial dimension. We will present results using an etching 3-D simulation which uses level set methods to advance the moving front. This code is an extension of SPELS, the Simulation of Profile Evolution using Level Sets, to calculate etch rates of silicon in chlorine discharges. We will show animations of the evolving trench for different geometries as well as for different process conditions. We will make comparisons of cross sections of the 3-D profiles to calculations from 2-D simulations and demonstrate the effects of a finite trench versus a semi-infinite trench on etch rates.

Authors Index

Bold page numbers indicate the presenter

— B —

Blain, M.G.: PS+MM-WeA7, 1
Boufnichel, M.: PS+MM-WeA9, **2**

— D —

Dalton, T.J.: PS+MM-WeA8, 2
Dussart, R.: PS+MM-WeA9, 2

— E —

Economou, D.: PS+MM-WeA1, **1**

— G —

Govindan, T.R.: PS+MM-WeA10, 2

— H —

Hausmann, A.: PS+MM-WeA2, 1
Hwang, H.: PS+MM-WeA10, **2**

— K —

Kersch, A.: PS+MM-WeA2, 1
Kim, D.: PS+MM-WeA1, 1
Knorr, A.: PS+MM-WeA2, 1

— L —

Lefaucheux, P.: PS+MM-WeA9, 2

— M —

Manginell, R.P.: PS+MM-WeA7, 1
Meyyappan, M.: PS+MM-WeA10, 2

— P —

Pang, S.W.: PS+MM-WeA3, **1**

— R —

Radecker, J.: PS+MM-WeA2, 1
Rangelow, I.W.: PS+MM-WeA5, **1**
Ranson, P.: PS+MM-WeA9, 2
Rich, S.G.: PS+MM-WeA7, 1

— S —

Schulze-Icking, G.: PS+MM-WeA2, **1**
Shul, R.J.: PS+MM-WeA7, **1**
Steen, M.L.: PS+MM-WeA8, **2**

— W —

Willison, C.G.: PS+MM-WeA7, 1

— Z —

Zmuda, S.A.: PS+MM-WeA7, 1