Tuesday Morning, November 5, 2002

Electronic Materials and Devices
Room: C-107 - Session EL+SC-TuM

Heterojunctions
Moderator: R.S. Goldman, University of Michigan

8:20am **EL+SC-TuM1 Epitaxial Growth and Characterization of CdS Layers Grown on InP (001) using Molecular Beam Epitaxy from Atomic Sulfur Beam and Thermally Evaporated Cd**, ***J.W. Choi***, *M.-A. Hasan, A. Bhupathiraju*, University of North Carolina at Charlotte

Recent progress in epi-ready InP(E_g=1.35 eV) wafer growth has prompted new applications of heterojunction devices and quantum structures based on closely lattice matched epitaxial films on InP. Cadmium sulfide (CdS), a direct bandgap material (E_g=2.5 eV), has a small lattice mismatch to InP (0.63%) that can facilitate optoelectronic integration on InP. In this work, growth of CdS on InP (001) substrates is investigated using modified molecular beam epitaxy (MBE). Two growth methods are investigated. In the first method, epitaxial growth is conducted by atomic sulfur (S) beam from an RF atomic source with H_2S as the source gas while Cd is supplied from a cracker cell. The RF source is operated at 13.56 MHz and produces an intense monoatomic sulfur beam (λ= 930.5 nm emission peak measured by plasma spectroscopy). In the second method, deposition is performed using CdS sublimation from a solid CdS using a conventional Knudsen cell. Rinsing by methanol is used to clean the epi-ready InP (001) substrates. Final substrate cleaning is achieved by thermal desorption (530-550°C) in vacuum. RHEED shows InP (001) 2x1 surface after thermal cleaning. In both methods, in-situ RHEED measurement indicates epitaxial growth of zincblende CdS; Auger electron spectroscopy (AES) shows stoichiometric CdS within the AES resolution limit. AES depth profiles also indicate an abrupt InP/CdS interface for all temperatures investigated. The growth rate of CdS is primarily governed by Cd flux as indicated by the activation energy measured from the flux-dependence of the growth rate. Atomic force microscopy (AFM) shows measurable dependence of surface roughness on growth method. For growth using an RF atomic source, average surface roughnesses of 1-2 nm is measured for all growth temperatures, layer thicknesses, and flux ratios with no evidence of island formation; higher roughness values (10-20nm) were typically measured for growth from solid CdS.

8:40am **EL+SC-TuM2 Structure of InAs/InP Interfaces Formed During Metalorganic Vapor-Phase Epitaxy**, ***D.C. Law***, *Y. Sun, C.H. Li*, University of California, Los Angeles, *S.B. Visbeck*, Siemens & Shell Solar Gmbh, *G. Chen, R.F. Hicks*, University of California, Los Angeles

We have studied the initial stages of heterojunction formation during the metalorganic vapor-phase epitaxy of indium arsenide on indium phosphide. Exposing an InP (001) film to 10 mTorr of tertiarybutylarsine below 500 °C results in the deposition of a thin InAs layer from 1.5 to 5.0 atomic layers thick (2.3 to 7.5 Å). The surface of this epilayer remains atomically smooth independent of arsenic exposure time. However, in an overpressure of tertiarybutylarsine at or above 500 °C, the arsenic atoms diffuse into the bulk, creating strained InAsP films. These films form three-dimensional island structures to relieve the built-up strain. The arsenic transport into InP can be described by a constant-source diffusion model with the arsenic number density given by: $N_{As} = 0.5\ N_f \mathrm{erfc}\ (x/2\sqrt{(D_{eff}t)})$. The activation energy and pre-exponential factor for arsenic diffusion into indium phosphide are: $D_o = 2.3\pm1.0 \times 10^{-7}$ cm^2/s and $E_d = 1.7\pm0.2$ eV.

9:40am **EL+SC-TuM5 Device Quality III-V Compound Semiconductor Epitaxy on Si Via SiGe Interlayers**, ***S.A. Ringel***, *C.L. Andre, A. Khan, M. Gonzalez, M.K. Hudait*, Ohio State University, *E.A. Fitzgerald*, Massachusetts Institute of Technology, *J.A. Carlin, M.T. Currie, C.W. Leitz, T.A. Langdo*, AmberWave Systems Corporation **INVITED**

Integration of III-V compounds with Si using direct epitaxial approaches has been an area of intense interest for years. Achieving this would enable a complement of electronic and optoelectronic capabilities that would generate new circuit functions with higher speed, and potentially simpler architecture. There is also substantial interest in III-V/Si integration where the primary purpose for Si is as an alternative substrate for III-V solar cells, which are conventionally grown on Ge or GaAs substrates. Compared to Si, these substrates are expensive, brittle and heavy, which are issues for this application. For both of these directions, the materials issues of how to integrate III-V compounds with Si without degrading electronic properties due to the mismatch in structural, thermal and chemical properties so that high performance devices can be achieved are the same. Here we show that growth of compositionally graded SiGe interlayers to accommodate lattice strain between a Si wafer and III-V epitaxial structures, coupled with monolayer-scale control over the formation of the initial III-V/IV interface to eliminate anti-phase domain disorder and block interface diffusion, together yield high quality AlGaAs/GaAs and InGaP/GaAs layers, heterostructures and minority carrier devices. Time resolved photoluminescence measurements of III-V double heterostructures reveal record high minority carrier lifetimes for GaAs on Si in excess of 10 nanoseconds, which is attributed to the simultaneous elimination of anti-phase domains and reduction of residual threading dislocation densities to below 1×10^6 cm^{-2}. SIMS and capacitance-voltage measurements show that autodoping is effectively eliminated for GaAs grown on Ge/SiGe/Si, with no additional background impurities detected in the GaAs layers grown on these substrates. Solar cells are used as examples of minority carrier devices to show that high performance comparable to similar devices grown on conventional substrates has been achieved, with record voltage output for III-V cells grown on Si.

10:20am **EL+SC-TuM7 Interdiffusion, Alloying, and Defect Formation at GaN-Sapphire Interfaces**, ***X.L. Sun***, *S.T. Bradley, G.H. Jessen, L.J. Brillson*, The Ohio State University

The chemical and electronic structure at GaN/sapphire interfaces has a major influence on the electronic quality of epitaxial GaN films. In particular, degenerate doping usually occur near hydride vapor phase epitaxy (HVPE) grown GaN/sapphire interfaces that can affect lateral transport in overgrown devices. Near the interface, impurity diffusion, alloying, and related defect formation can occur at the high (1150°C) growth temperatures that is important to understand and control. We have used Auger electron (AES) and cathodoluminescence (CLS) spectroscopies in a UHV scanning electron microscope (SEM) to probe the chemical and electronic features at the HVPE GaN/sapphire interface in cross section in a nanometer scale. Specimens were cleaved and Ar sputtered in UHV to prepare clean interfaces with well-defined AES, CLS, and secondary electron images. AES images reveal dramatic evidence for diffusion of O from sapphire typically decreasing exponentially ~ 1 μm into GaN from 60% to the detection limit of < 1% surface coverage. The AES O intensity line profile mirrors corresponding SIMS O depth profiles and a donor level CLS emission vs. depth normal to the interface found in similar samples. Conversely, N with plateau concentrations of ~5 % extend ~ 2 μm into the sapphire and correspond spatially to a 3.8 eV defect emission attributed to Al-N-O complexes. While Ga exhibits no strong diffusion, interface Al decreases from 10% to < 1% over ~1 μm into the GaN and support evidence for AlGaN alloy formation, based on ~3.6 eV CLS emission above the GaN band gap at the buried interface. Depending on surface pretreatment and growth conditions, such interfaces can be abrupt to < 200 nm or can exhibit interdiffusion on a micron scale. These results illustrate a new approach to probe chemical and electronic interactions at semiconductor heterojunctions and reveal that both interdiffusion and alloying can occur and lead to extrinsic electronic effects.

10:40am **EL+SC-TuM8 Growth and Characterization of Heterjunction Diode Made of AlN on Si(111)**, ***K. Sundaresan***, *M. Jenkins, M.-A. Hasan*, University of North Carolina, *M. Sardela Jr.*, University of Illinois

Single crystalline hexagonal AlN(001) was grown on Si(111) using surface-reconstruction induced epitaxy. The Si(111)7x7 surface, generated under thermal etching under UHV, was first passivated by deposition of ~0.3 monolayer (ML) of Al at 650-700 °C. Each Al atom bonds to 3 Si atoms on the surface, which give rise to the well-known Si(111)root3xroot3 surface. The well ordered, Al-passivated Si(111)root3xroot3 surface was then used as a template to initiate epitaxial growth of AlN on Si. The growth was conducted by using an atomic N flux from a RF atomic source and thermal Al evaporation. X-ray diffraction showed single crystalline hexagonal AlN(001) with a full width at half maximum (FWHM), measured from the layer peak, equal to that of the Si substrate indicating highly oriented AlN layer. Epitaxial growth was achieved over a wide range of Al/N flux ratio and growth temperatures extending from 350 to 850 °C. AlN/Si heterojunction diode, fabricated using this method showed a breakdown voltage in excess of 350 V and a leakage current below 100 nA indicating high quality interface.

11:00am **EL+SC-TuM9 Observation of a Long-range Strain Field under SiO_2/Si Interface by using Multi-wave X-ray Diffraction**, ***W. Yashiro***, National Institute of Advanced Industrial Science and Technology (AIST), Japan, *K. Sumitani, T. Takahashi,* The University of Tokyo, Japan, *Y. Yoda,* Japan Synchrotoron Radiation Research Institute (JASRI), *K. Takahashi, T. Hattori,* Musashi Institute of Technology, Japan

In order to further improve the speed of VLSI circuits, new materials and device structures are being proposed in recent year. In particular there has been considerable interest in strained Si because it can lead to high-performance metal-semiconductor (MOS) devices. Transmission electron microscopy (TEM) is a technique to investigate local strains, e.g. around a dislocation at a phase boundary. In contrast with TEM, x-ray diffraction is powerful to investigate long-range ordered structures in crystals. In the present paper, we propose a new method that is sensitive to very small and long-range strains near surfaces of crystals by using multi-wave x-ray diffraction technique. To date, the Bragg reflection of x-ray diffraction is used to investigate such long-range strain fields. Recently Emoto et al. have indicated using the Bragg reflection that there exist very small strain fields on the side of the Si substrates if even ultra-thin layers are formed on them.[1] Our method is also a method using the Bragg reflection, but with the important distinction that we use a phenomenon, intensity modulation of the CTR scattering under a Bragg condition. This makes it possible to determine total displacements due to small lattice distortions, rather than local lattice spacing. The method was applied to a Si(001) wafer whose surface is covered with an oxide layer about 5 nm thick formed by microwave-excited high density Kr/O_2 plasma oxidation. We found that the total displacement of -0.18 Å in the direction normal to the surface exists under the interface between the oxide layer and the substrate.

[1]Emoto et al. Surf. Sci. 493 (2001) 221-226.

11:20am **EL+SC-TuM10 Measurement of Fermi Level Pinning Kinetics at Si-SiO_2 Interfaces: Implications for CMOS Transistor Manufacture**, ***K. Dev***, *M.Y.L. Jung, R. Gunawan, R.D. Braatz, E.G. Seebauer*, University of Illinois

Excessive transient enhanced diffusion (TED) of boron in silicon has been a major inhibitor to forming ultrashallow junctions for CMOS device applications. Current technology for junction formation relies on ion implantation into Si through SiO_2 to introduce dopants into the substrate, followed by rapid thermal annealing. We have investigated a previously unknown effect in this process sequence: charge build-up at the Si-SiO_2 interface and the resulting Fermi level pinning that can occur just after implant. Fundamentally, the charge build-up occurs in response to the ion-induced formation of dangling bonds that introduce energy states into the Si surface bandgap. The present work uses the optical technique of photoreflectance to demonstrate experimentally that these effects indeed exist and to measure their evolution kinetics. Photoreflectance is one of a class of modulation spectroscopies in which a semiconductor is periodically perturbed, and the resulting change in dielectric constant is detected by reflectance. The presence of a photoreflectance spectrum demonstrates unequivocally the existence of Fermi level pinning. The spectral amplitude scales linearly with the magnitude of built-in surface potential. Thus, we can deduce the pinning kinetics from the variation in amplitude. Our data demonstrate the existence of substantial pinning just after implant with 500 eV ions. Healing begins to occur in the vicinity of 400°C - within the temperature stabilization step in which interstitial clusters form. TED simulations using electrostatic boundary conditions derived from the photoreflectance experiments show that pinning deepens the pn junction significantly by transforming the Si-SiO_2 interface into a reflector of charged bulk interstitials.

11:40am **EL+SC-TuM11 Effects of Interface Properties on Degradation and Reliability of CMOS Devices with RPECVD Stacked Oxide/Nitride and Oxynitride Dielectrics**, *G. Lucovsky,* ***Y. Lee***, North Carolina State University, *Y. Wu,* Advanced Micro Devices, *C. Bae, J.G. Hong*, North Carolina State University

The effects of interface properties on device degradation and reliability of sub-2nm stacked oxide/nitride and oxynitride gate dielectrics prepared by the remote plasma enhanced CVD (RPECVD) technique under constant voltage stress (CVS) are investigated. Time evolutions of the transient SILC effect and threshold voltage (Vt) changes have been demonstrated to illustrate the breakdown behaviors and charge trapping during stress. More negative Vt shifts were observed for both P- and N-MOS devices, indicating the increases of hole trapping at the Si/SiO_2 interface. The p-channel transistors with stacked gate dielectrics received interface N_2/He nitridation and effectively suppress positive off-state leakage current, resulting in less device degradation as compared to the transistors without interface nitridation. This improvement is attributed to approximately one monolayer of N at the Si/SiO_2 interface which suppresses hole trapping. In addition, the influence of remote-plasma-assisted oxidation (RPAO) thickness on oxynitride device degradation and reliability is also studied. It is found that the devices with 0.6 nm RPAO exhibit improved C-V characteristics, lower post-breakdown current and higher TDDB reliability compared to the devices with 0.8 nm RPAO. The generation of interface states and the correlation between carrier conduction mechanism and TDDB are also discussed.

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