Thursday Morning, November 7, 2002

Dielectrics
Room: C-107 - Session DI+EL-ThM

Issues for Gate Dielectrics
Moderator: D.P. Norton, University of Florida

8:20am **DI+EL-ThM1 Epitaxial Oxides on Silicon for Alternative Gate Dielectrics and More**, ***D.G. Schlom***, Penn State University **INVITED**

The epitaxial growth of oxides on silicon presents opportunities to harness the full spectrum of electronic, optical, and magnetic behavior available in oxides, while simultaneously exploiting the properties of the underlying semiconductor. One key application for epitaxial oxides on silicon, which will be the focus of this talk, is to produce a viable gate dielectric alternative to SiO_2 for silicon MOSFETs with higher dielectric constant (K). As a first step in the identification of such an alternative gate dielectric, we used tabulated thermodynamic data to comprehensively assess the thermodynamic stability of binary oxides and nitrides in contact with silicon at temperatures from 300 to 1600 K. Sufficient data exist to conclude that the vast majority of binary oxides and nitrides are thermodynamically unstable in contact with silicon. The dielectrics that remain are candidate materials for alternative gate dielectrics. Of these remaining candidates, the oxides have significantly higher K than the nitrides. We then extended this thermodynamic approach to multicomponent oxides comprised of candidate binary oxides. The result is 13 silicon-compatible gate dielectric materials with $K > 20$, of which at least six have an optical bandgap ≥ 5 eV. Having identified promising candidate materials with high K, high optical bandgap, and the likelihood for thermodynamic stability in contact with silicon, we have been using MBE to epitaxially integrate the candidate materials having the best lattice match with silicon. High-resolution cross-sectional TEM analysis of the epitaxial interface between silicon and epitaxial oxides will be shown. Some of these interfaces were formed by growing silicon on the dielectric; others were formed by growing the dielectric on silicon. Achieving the former interface is easier as it involves the deposition of a single component material (Si) in a vacuum environment. In contrast, the latter involves multiple components, and as one of these components is oxygen, the possibility of oxidizing the silicon surface and not only losing the epitaxial template, but also forming an undesired SiO_2 layer. Over the last two decades, three strategies have been used to grow epitaxial oxides on silicon: (1) to grow with no excess oxidant, (2) to grow with excess oxidant at high substrate temperatures, and (3) to grow with excess oxidant at low substrate temperatures. The overarching goal of all three strategies is to avoid the formation of an amorphous SiO_2 layer that would result in the loss of the substrate's crystalline template before the oxide has a chance to nucleate on it. Most reports of the epitaxial growth of oxides on silicon fall into the high temperature / excess oxidant regime. Although successful for the nucleation of an epitaxial oxide layer, these growth conditions typically lead to the growth of an SiO_2 layer at the silicon interface. To avoid this layer, whose replacement is the purpose of the alternative gate dielectric, we have studied the last of the three regimes-the low temperature / excess oxidant regime. In this regime the oxidation of silicon by the oxidant is limited by kinetics. However, kinetic barriers to the oxidation of the constituents of the desired oxide at these low temperatures can also occur. We have performed in situ oxidation studies to assess the low temperature oxidation of various elements. Examples illustrating oxides that can be grown epitaxially on silicon in the low temperature / excess oxidant regime will be presented, as well as epitaxial oxide / silicon heterostructures that make use of the integration of the overlying epitaxial oxide layers and the underlying silicon.

9:00am **DI+EL-ThM3 Electrical and Material Properties of 10 nm Thick Hf-Doped Tantalum Oxide High k Dielectrics**, ***J. Lu***, *J.Y. Tweg, Y. Kuo*, Texas A&M University, *P.C. Liu*, AMD, *B.W. Schueler*, Physical Electronics

A high k gate dielectric material that replaces the nm thick SiO_2 is necessary for sub 100 nm ULSICs for many practical reasons.[1] Metal oxides such as Ta_2O_5, HfO_2, ZrO_2 and Al_2O_3, are promising candidates and have been intensively investigated. However, they suffer from problems such as the high leakage current and high interface states. It was reported that by adding a third element into the metal oxide, some of the dielectric properties could be improved.[2,3] In this paper, we studied the Hf-doped Ta_2O_5 thin films deposited by reactive magnetron sputtering. Electrical properties of the 10 nm thick films, such as the k value and leakage current, were measured. Compositions, microstructures, and interfacial properties of the film were probed with ESCA, TEM and SIMS. Compared with the undoped film, the doping process reduced the leakage current, improved the k value, and lowered the fixed charge density. Influences of the post-deposition annealing process parameters, such as temperature and time, to high k properties were also studied. We are going to present these experimental results and to compare them with literature reports. This project is supported by the Texas Higher Education Coordination Board ATP program (project # 0005120003-1999).

[1]International Technology Roadmap for Semiconductors, 1999 edition, SIA.
[2]Y. Kuo, J. Y. Tewg, J. P. Donnelly, and J. Lu, ECS Procs. Intl. Semi. Technol. Conf., 2001-17, 324, 2001.
[3]Y. Kuo, J. Y. Tewg, and J. P. Donnelly, ECS Meeting Abstract, 2001-1, No. 232, 2001.

9:20am **DI+EL-ThM4 The Effect of N_2 Annealing on $Al_xZr_yO_z$ Oxide**, ***J. Pétry***, *O. Richard, W. Vandervorst, T. Conard*, IMEC, Belgium, *J. Chen, V. Cosnier*, International Sematech c/o IMEC, Belgium

In the path to the introduction of high-k dielectric into IC components, a large number of challenges have to be solved. One of these concerns the stability of high-k oxides to high temperature annealing. Indeed annealing will most likely be necessary to improve the electrical characteristics of the high-k layer itself and the high-k stack will be submitted to annealing in further processing. In this study, we investigated the effect of annealing of ALCVD AlZrO layers in N_2 from 700 to 900C by XPS, TOFSIMS, TEM and FTIR. The effect of the Si surface preparation (HF-last, 0.5 nm RTO, Al_2O_3) on the modification of high-k oxide and interfacial layer upon annealing was also analyzed. We first studied the compositional changes of the mixed oxide upon annealing. For all temperature and surface preparation considered, we observed a segregation of the mixed oxide with the Al oxide at the surface. We also observed an increase of the Si concentration in the high-k film itself, with a diffusion profile towards the surface of the film. On the other hand, the modification of the interfacial layer is strongly dependent on the system considered. In the case of mixed oxide grown on 0.5 nm RTO, no changes are observed between the as-deposited layer and the layer annealed at 700C. At 800C, radical change appears: the initial RTO layer seems to be converted to a mixed layer composed of the initial SiO_2 and AlO coming from the mixed oxide, without forming an Al-silicate layer. This remains for annealing at 900C. When grown on 1.5 nm Al_2O_3 on 0.5 nm RTO, the only difference from the previous system is the observation of an Al-silicate fraction in the interfacial layer for the as-deposited and 700C annealed samples, which disappears at higher temperatures. Finally, when grown on HF-dipped Si, we observe a slight increase of the interfacial thickness after annealing at 700C and no further changes for higher annealing temperature.

9:40am **DI+EL-ThM5 Pulsed Plasma Enhanced MOCVD of High k Y_2O_3 Layers for Gate Dielectric Applications**, ***C. Durand***, *B. Pelissier, C. Vallee, M. Bonvalot, L. Vallier, O. Joubert*, CNRS/LTM, France, *C. Dubourdieu*, CNRS/LMGP, France

CMOS transistor scaling is rapidly reaching its limits with traditional SiO@sub2@ gate oxide due to increasing tunneling currents. Rare earth oxides, as high k materials to replace SiO@sub2@, have shown promising results. Here, we focus on the elaboration of Y@sub2@O@sub3@ thin films by an innovative technique, namely pulsed injection Plasma Enhanced Metal Organic Chemical Vapor Deposition (PE-MOCVD). In this technique, dissolved Y(thd)@sub3@ precursors are sequentially injected into an evaporator, which allows perfect reproducibility of the amount of precursors delivered to the plasma chamber and then onto the SiO@sub2@ (8 @Ao@)/Si substrate heated at 350@degree@C. An Ar/O@sub2@ plasma is applied to favor precursor decomposition and surface reactivity. Preliminary experiments have shown that no Y@sub2@O@sub3@ film is deposited on substrates heated at 350@degree@C by pulsed MOCVD only, whereas stoichiometric layers (typ. 5 nm thick) are obtained with the plasma. The plasma induces a lower deposition temperature compared to MOCVD. Based on X-rays Photoelectron Spectroscopy (XPS) and infrared spectroscopy studies of the initial stages of the thin film formation, it seems that metallic yttrium atoms react with SiO@sub2@ to form silicate compounds. The thickness of the initial SiO@sub2@ layer gradually changes leading to silicate layer formation. The SiO@sub2@ underlayer can be fully consumed. Y@sub2@Osub3@ thin films have been annealed at a temperature of 600@degree@C under several atmospheres. Subsequent XPS analyses indicate that carbon contamination can be reduced by half, independent of the annealing atmosphere Ar or O@sub2@, thereby suggesting densification of the layer. Further experiments are under way to determine optimum annealing conditions leading to fully oxidized Y@sub2@O@sub3@ layers without carbon atoms. Simultaneously, the behavior of the silicate interface during this annealing treatment will be carefully analyzed.

10:00am **DI+EL-ThM6 Plasma Enhanced MOCVD of Hafnium Oxide and Hafnium Silicate Thin Films**, *V. Rangarajan*, ***H. Bhandari***, *T.M. Klein*, University of Alabama

Hafnium oxide films were deposited by Metal Organic Chemical Vapor Deposition (MOCVD) on Si using hafnium t-butoxide as the metal organic precursor. X-ray diffraction data show a monoclinic crystal structure when films were deposited at 400°C. Films were subjected to ex-situ furnace anneal and compared with as deposited films using XPS that showed a significant interfacial silicon dioxide growth. Hafnium silicate films were deposited by both thermal and plasma enhanced MOCVD using SiH_4 as the Si precursor. Plasma excitation improved Si incorporation resulting as much as 21.5 at.% Si. The films were subjected to furnace anneals up to 1100°C in oxygen and XPS analysis was done to confirm the silicate formation, composition and stability. Surface and bulk film morphology was studied using AFM and XRD respectively. Thermally grown Hf silicates had a measured 1.1 nm rms roughness, while plasma deposited films had 5.2 nm rms roughness. Both thermal and plasma deposited Hf silicates are amorphous as deposited, however thermal films exhibit crystallinity after a 30 min 1100°C furnace anneal in oxygen while plasma deposited films remained amorphous after the same treatment. Reflection FTIR measurements were performed and results show no evidence of bulk carbon incorporation. In-situ anneals in Ar ambient were done on thin films of HfO_2 and silicates and their change in chemical state was studied using XPS.

10:20am **DI+EL-ThM7 UHV-CVD of Al_2O_3 for Gate Dielectric Applications**, ***B.R. Rogers***, *Z. Song, R.D. Geil, V. Pawar, D.W. Crunkleton, R.A. Weller*, Vanderbilt University

Successful replacement of silicon dioxide-based MOSFET gate dielectrics by a high-permittivity (high-k) dielectric is a critical step in the continued drive to build the smaller, faster, lower-power, more-integrated circuits that society is demanding. Our goal toward this effort is to develop a thermodynamically and microstructurally stable, amorphous material system, having no interfacial silicon dioxide formation. In this presentation I will briefly discuss the need for an alternative gate dielectric and a "wish list" of characteristics for this material. I will then discuss our work on developing alumina/zirconia alloys as a potential gate dielectric. We have begun this effort by studying the deposition of alumina films in an ultra-high-vacuum chemical vapor deposition (UHV-CVD) system. I will present our findings to date in relation to the CVD process. In addition I will discuss the characterization of these films using spectroscopic ellipsometry and time-of-flight medium energy backscattering (ToF-MEBS), a characterization capability unique to Vanderbilt University.[1]

[1] This work is supported by the National Science Foundation grant # CTS-0092792.

10:40am **DI+EL-ThM8 Hafnium Oxide As an Alternative Gate Dielectric in MOSCAP and MOSFET Application**, ***Y. Lin***, *R. Puthenkovilakam, J.P. Chang*, University of California, Los Angeles

HfO_2 is investigated in this study to replace SiO_2 as the gate dielectric material in metal-oxide-semiconductor devices. HfO_2 films were deposited on P-type Si (100) wafers by an atomic layer chemical vapor deposition (AL-CVD) process using hafnium (IV) t-butoxide $Hf(OC_4H_9)_4$ as the precursor and oxygen as the oxidant. The two chemistries were introduced sequentially into the reactor with purging and evacuation in between. The deposited films were stoichiometric and uniform based on X-ray photoemission spectroscopic and ellipsometry. The X-ray diffraction analysis indicated the deposited film was amorphous, however, it showed an interfacial layer formation at on the silicon substrate based on the chemical etching resistance experiment. This interfacial layer will be examined by the high-resolution transmission electron and medium energy ion scattering analysis. The step coverage will also be examined by depositing HfO_2 on 200 nm features with an aspect ratio of 4. The thermal stability of HfO_2 thin film on silicon was examined by Synchrotron radiation x-ray photoemission spectroscopy. The HfO_2 thin films were thermally stable up to 950° C in vacuum. In-situ Infrared analysis and ellipsometer measurement are underway to enhance our ability to understand the surface reactions. Isotope labeling of oxygen will be perform to study the effect of the oxidation/annealing processes on film composition. The dielectric constant of HfO_2 was 18 from the C-V measurement, which was slightly lower than the bulk HfO_2 . In the C-V measurement a small hysteresis and the interface state density was approximately $5.22x10^{11}$ cm^{-2} eV^{-1} are observed. The leakage current is 2~3 order magnitude lower than SiO_2 at the same equivalent oxide thickness. NMOS transistors will be fabricating to exam the applicability of HfO_2 for MOSFET application.

11:00am **DI+EL-ThM9 Hafnium Silicate and Nitrided Hafnium Silicate as Gate Dielectric Candidates for SiGe-based CMOS Technology**, ***S. Addepalli***, *P. Sivasubramani, H. Zhang, M. El-Bouanani, M.J. Kim, B.E. Gnade, R.M. Wallace*, University of North Texas

Strained epitaxial Si_xGe_{1-x} layers on Si have attracted considerable technological interest due to the enhancement in hole mobility, as well as ease of integration with existing Si CMOS technology. One of the major drawbacks, however, is the inability to produce a high-quality gate oxide in direct contact with Si_xGe_{1-x}, while maintaining the integrity of the oxide-Si_xGe_{1-x} interface. The introduction of a stable high-κ dielectric provides the prospect of simultaneously enhancing the capacitance of the gate stack and reducing leakage current for high performance SiGe devices. We have investigated hafnium silicate and nitrided hafnium silicate as viable candidates for SiGe-based CMOS technology. Hafnium silicide and nitrided hafnium silicide films were sputter deposited directly on Si_xGe_{1-x}. These films were subsequently converted to hafnium silicate and nitrided hafnium silicate respectively by employing a room temperature UV-ozone assisted oxidation approach in order to preserve the pseudomorphic nature of the Si_xGe_{1-x} layers. The bonding and composition of these films were characterized by X-ray photoelectron spectroscopy (XPS), Fourier Transform Infrared Spectroscopy (FTIR), and Rutherford Backscattering Spectrometry (RBS). The deposition and post-deposition processing parameters were optimized using XPS, High-resolution transmission electron microscopy (HRTEM), and FTIR. The electrical performance of the films was evaluated from capacitance-voltage (C-V) and current-voltage (I-V) measurements. The effects of various post-deposition annealing treatments on the electrical performance of the films were also studied. This work is supported by DARPA through SPAWAR Grant No. N66001-00-1-8928, and the Texas Advanced Technology Program.

11:20am **DI+EL-ThM10 XPS Study of Chemical Phase Separation in Amorphous Zr Silicate High-k Dielectrics**, ***G.B. Rayner***, *D.H. Kang, G. Lucovsky*, North Carolina State University

X-ray photoelectron spectroscopy (XPS) was used to investigate chemical phase separation in pseudo-binary Zr silicate alloys, $(ZrO_2)_x(SiO_2)_{1-x}$, deposited at 300C on Si substrates as a function of alloy composition, film thickness and subsequent annealing temperature. Based on previous infrared (IR) and x-ray diffraction (XRD) studies, it been shown that a chemical phase separation in (a) ZrO_2 and (b) SiO_2 with up to about 5 atomic percent ZrO_2 occurs in Zr silicate alloys when annealed at 900C in a non-oxidizing ambient such as Ar.. This separation is not accompanied by crystallization for silicate alloys with x~ 0.25, but crystallization of the ZrO_2 phase occurs for x> ~ 0.5. For Zr silicate films ~30 nm thick and x < ~0.6 the XPS O1s core level peak shapes are essentially unchanged for annealing temperatures to 500C. However, for annealing at 900C, the O1s core level peak splits into a distinct doublet with binding energies independent of alloy composition for $0.35 < x < 0.6$. The peak at low binding energy, assigned to O^{2-} ions in the ZrO_2 phase, scales approximately linearly with composition. These results indicate a transition from silicate bonding, characterized by Si-O-Zr alloy bonds, into bonding characteristic of the end-member oxide phases, SiO_2 and ZrO_2. The XPS results presented here provide additional insights into local bonding that are complementary to what has been revealed previously in IR studies, as well as confirming the chemical phase separation that occurs for annealing temperatures > 900C in inert ambients. Included also are the results of a parallel study on the effect of chemical phase separation on the electrical performance of metal oxide semiconductor capacitors.

11:40am **DI+EL-ThM11 Electrical Properties of SiO_2 Films Grown by Si(100) Reactions with Oxygen, Wet-oxygen and Wet-hydrogen**, ***Y. Liu***, *J. Hebb*, Axcelis Technologies, Inc.

The oxidation of Si(100) by oxygen (O_2), wet-oxygen (H_2O+O_2) and wet-hydrogen (H_2O+H_2) is of great importance for silicon oxide (SiO_2) dielectric film formation in the advanced CMOS devices. At the atmospheric pressure and high temperatures (>1100°C), 20 to 100 Å SiO_2 films have been grown on Si(100) wafers (dia.=200 mm) using a hot-wall rapid thermal processor (Summit 200, Axcelis) enhanced with a small volume (3-liter) quartz reactor for rapid gas switching. Wet-oxygen and wet-hydrogen with controlled compositions are produced using a hydrogen-rich and an oxygen-rich catalytic water vapor generator (WVG), respectively, and are monitored in real-time with a residual gas analyzer (RGA). Kinetic equations for Si(100) reactions with oxygen and water vapor are used to control oxidation temperature, oxidant fractional pressure and time to achieve desired oxide thickness. To grow a thermal oxide film, a Si(100) wafer is rapidly heated to a desired temperature in nitrogen or hydrogen. Rapid gas sequencing is carried out to expose the wafer to oxygen, wet-oxygen or wet-hydrogen for oxidation, and back to nitrogen or hydrogen for annealing and cooling. Critical electrical properties of the thermal oxide films grown under various conditions are measured and

compared systematically using a powerful and non-contact Corona Oxide Characterization of Semiconductor (COCOS) tool (FAaST, SDI). These properties include equivalent oxide thickness (EOT), oxide capacitance, flat band voltage, effective oxide charge, interface trapped charge, interface trap density, and interface trap density spectrum. Gate oxide integrity (GOI) of these films is quantified by leakage current versus voltage (I-V) and stress-induced leakage current (SILC) measurements. Correlation between growth conditions and oxide qualities will be made.

Authors Index

Bold page numbers indicate the presenter