Wednesday Afternoon, November 6, 2002

Applied Surface Science
Room: C-106 - Session AS-WeA

High-k Dielectric Characterization
Moderator: B.R. Rogers, Vanderbilt University

2:00pm **AS-WeA1 Ultra-high Resolution AES Depth Profiling using a Masked Specimen Holder**, ***K. Satori***, *H. Kobayashi*, SONY Corporation, Japan, *K. Kimura, K. Nakajima*, Kyoto University, Japan

Auger electron spectroscopy (AES) using an instrument with coaxial geometry for an electron column and a cylindrical mirror analyzer (CMA) has the advantages of high sensitivity and accurate mapping capability. However, the analytical depth when using a coaxial CMA is larger than when using a hemispherical analyzer because the angle of the Auger electrons detected by a coaxial CMA ranges widely at any given tilt angle. This is a serious problem when we wish to evaluate ultra-thin films such as gate dielectrics. Some studies have been conducted using ion sputtering with low kinetic energy, to obtain high depth resolution. However, these studies have highlighted that one of the most important factors concerning depth resolution is the analytical depth. We designed angled and masked specimen holders to obtain a more shallow analytical depth using the coaxial CMA. We optimized the holder angle by calculating the distribution of the angle of the Auger electrons and the actual AES measurement to increase the intensity of the Auger electrons emitted at high angle from the surface normal. Next, we designed an electron shadow mask on a specimen holder to prevent the analyzer detecting the Auger electrons at low angle from the surface normal. Using the holder that we designed, the surface-sensitivity becomes three times higher than that of conventional methods. In addition, to improve depth resolution, we designed a new mask shape and obtained a low incident angle for the ion beam. Using the holder, the depth resolution was improved sufficiently to evaluate ultra-thin silicon oxynitride films (thickness 2.5nm). The shape of the AES depth profile was in good agreement with that obtained by means of high-resolution Rutherford backscattering spectroscopy. Our method is easy to use but useful for obtaining a shallow analytical depth and high depth resolution.

2:20pm **AS-WeA2 Sputtering Artifacts in Depth Profile Analysis of HfO_2 and $HfSi_xO_y$**, ***C.F.H. Gondran***, *J.A. Bennett, M.R. Beebe*, International SEMATECH

As electrical device sizes continue to shrink, thinner transistor gate oxides are required. Soon the required gate oxide thickness will be too thin to be obtained using SiO_2. Thicker gate oxides can be used to obtain the desired equivalent silicon dioxide thickness if the material used has a higher dielectric constant. HfO_2, ZrO_2 and their silicates are among the most promising candidates for alternative high-dielectric-constant gate materials. With these new materials, come a host of new challenges for both device processing and materials characterization. Preferential sputtering and other affects seen in the Auger and SIMS depth profiles of HfO_2 and $HfSi_xO_y$ result in the appearance of Hf deep into the Si Substrate. In mixed oxides the relative size of this artifact varies with the composition posing a challenge for quantitative analysis. The sputtering artifacts in HfO_2 and $HfSi_xO_y$ are characterized and practical approaches for analysis are discussed.

2:40pm **AS-WeA3 Challenges for the Characterization and Integration of High-k Gate Dielectrics**, ***R.M. Wallace***, University of North Texas **INVITED**

The integration of new high-k gate dielectric materials into advanced planar CMOS technology presents several significant challenges.[1] Moreover, the introduction of these materials is expected to occur at an unprecedented pace to meet industry technology forecasts[2] and will therefore mandate a rapid correlation of physical characterization with electrical performance. Although recent research has dwelled on the search for a material that yields a suitable (higher) dielectric constant, a more important problem is the actual integration of any new dielectric material in existing CMOS flows in a cost-effective manner. These integration issues include etching, control of phase segregation, dopant penetration, gate electrode compatibility, and many others that will influence the resultant electrical properties. This talk will examine several of these integration issues and the associated surface and thin film characterization challenges that must be addressed for successful high-k gate dielectric integration.

[1]For a review, see: G.D.Wilk, R.M.Wallace and J.M.Anthony, J. Appl. Phys. 89 (2001) 5243.
[2]See the International Technology Roadmap for Semiconductors at http://public.itrs.net/.

3:20pm **AS-WeA5 Quantitative Depth Profiling of Hafnium Films by Electron Spectroscopies**, ***P. Mrozek***, *H. Krasinski, D. Sarigiannis, B. Kraus*, Micron Technology Inc.

Surface analysis was performed by AES/XPS on hafnium oxide and hafnium oxy - nitride films grown on silicon. Depth profiles, using elastic peak intensities, aided estimates for inelastic mean free path ratios. Subsequent AES and XPS quantitative analysis was performed using matrix correction factors that incorporated these ratios. Linear least squares analysis was used to deconvolute the different chemical states from elastic peaks and to identify phases within multilayers. Auger parameter, based on hafnium high energy Auger transitions M4N6,7N6,7 and the deep 3d5/2 core level, was used to verify the presence of oxide and silicide layers that were detected by these hafnium chemical state profiles. The results were compared with those obtained from the usual AES quantitative analysis approach to demonstrate the value of supplemental elastic peak measurements.

3:40pm **AS-WeA6 Binding Energy Shifts in Soft X-ray Photoelectron Spectroscopy of HfO_2/SiO_2/Si High-k Gate-dielectric Structures**, ***M.D. Ulrich***, *J.G. Hong, J.E. Rowe, G. Lucovsky*, North Carolina State University, *T.E. Madey*, Rutgers, The State University of New Jersey

We have observed binding energy shifts for thin films of $(HfO_2)_x(SiO_2)_{1-x}$ on Si(111) substrates deposited as alternative high-k gate dielectrics in the film thickness range, 6-15 Å. Thin films of HfO_2 and $(HfO_2)_x(SiO_2)_{1-x}$ on Si(111) substrates were prepared by remote plasma enhanced chemical vapor deposition (RPECVD). This process results in a 6-10 Å layer of SiO_2 between the deposited dielectric and substrate. Samples were analyzed using high-resolution soft X-ray photoelectron spectroscopy (SXPS) with synchrotron radiation. Photoemission measurements were performed at the National Synchrotron Light Source (NSLS) located at Brookhaven National Laboratories using beamline U4A which has a total instrumental resolution of better than 0.1 eV. The Si $2p_{3/2}$ [SiO_2] binding energy from SiO_2 films on silicon substrates decreases with decreasing (5-30 Å) film thickness due to core hole screening. This shift is well described with an image charge model of core hole screening.[1] According to this model, an overlayer above the SiO_2 layer should further increase Si $2p_{3/2}$ [SiO_2] core hole screening causing an additional decrease in binding energy. For the HfO_2 samples, SiO_2 thickness was determined to be ~10 Å. The Si $2p_{3/2}$ [SiO_2] binding energy was 0.3 eV lower than that of a SiO_2 film of similar thickness without the HfO_2 overlayer. The Si $2p_{3/2}$ single-component SXPS spectra indicate that interfacial silicate exists between the SiO_2 and HfO_2 with a signal strength less than one third that of the SiO_2 peak. The result of the Si $2p_{3/2}$ [SiO_2] binding energy matches the image charge model well.

[1] J. W. Keister, J. E. Rowe, J. J. Kolodziej, H. Niimi, H.-S. Tao, T. E. Madey, and G. Lucovsky, J. Vac. Sci. Technol. A 17, 1250 (1999).

4:00pm **AS-WeA7 Chlorine and Oxygen Transport in ALD Grown ZrO_2 and HfO_2 Films on Silicon**, ***S. Ferrari***, *G. Scarel, C. Wiemer, S. Spiga, M. Fanciulli*, Lab. MDM - INFM, Italy

ZrO_2 and HfO_2 have received a lot of attention as possible candidates to replace SiO_2 as insulating layers in CMOS structures. Oxygen diffusivity in those materials may affect a number of properties. Among them, oxygen stoichiometry in the oxide, interfacial silicon oxide formation/reduction are critical parameters that need to be controlled in order to succesfully build high-k based devices with the desired properties. The growth of ZrO_2 and HfO_2 films by means of Atomic Layer Deposition (ALD) from $ZrCl_4$ And $HfCl_2$ percursors is known to cause significant incorporation of chlorine. Chlorine may have detrimental effects on the electrical properties of the films, by introducing positive charge in the film and possibly localized states in the band gap. In this paper we study oxygen and chlorine diffusion by means of Time of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) in ZrO_2 and HfO_2 films as a function of annealing temperature in different environment gasses such as N_2 and O_2 . Preliminary results show that in oxygen deficient environment chlorine desorption in inhibited, demonstrating that chlorine can out-diffuse by exchange with the oxygen. HfO_2 shows a limited oxygen and chlorine mobility as compared to ZrO_2.

4:20pm **AS-WeA8 A Study of the Microstructure and Electrical Properties of the Reoxidized HfO_2 upon Annealing Methods**, ***D. Lee***, *H.-E. Seo, D.-H. Ko, M.-H. Cho*, Yonsei University, Korea, *C.-W. Yang*, Sungkyunkwan University, Korea

Hafnium oxide has been known as gate dielectric material to replace SiO_2 in MOS devices. First of all, for preparation of reoxidized HfO_2, Hf films were deposited on p-type Si(100) substrate by DC magnetron sputtering system. Next, Hf films were reoxidized by RTA(Rapid Thermal Annealing) and

vertical furnace. They were analyzed by AFM, XRD, XPS, AES and HR-TEM. For ~50nm thick as-deposited Hf film, the HfO_2 layer was observed about ~5nm at the surface by HR-TEM. The HfO_2 layer increased to be ~15nm at 600°C in N_2 ambient. Especially, HfO_2 grains were shown not only at the surface of the Hf film but also at the silicide(Hf_5Si_4) grain boundaries. These grains of silicides on the Si substrate were not observed at the sample that annealed at 800°C for 30min in N_2 ambient, due to decompositing into HfO_2 and Si. And then the Si reacted with the oxygen that diffused from surface and accumulated on the interface of Si-substrate. For ~10nm thick as-deposited Hf films, it was observed that the HfO_2 films locally crystallized in the whole films and the interfacial layer between HfO_2 and Si substrate was about 8Å. After annealing by furnace as increasing anneal time and temperature in N_2 or O_2 ambient, also, the thickness of interfacial layer was increased to that of as-deposited film. As a result of measuring C-V and I-V, it was calculated that the value of CET was 51.5Å at -3V and dielectric constant was about 15.5 at 800°C for 5min in N_2 ambient. The leakage current of HfO_2 film decreased as the anneal temperature increased or time increased at constant temperature.

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