Electronics
Room 130 - Session EL-MoM

Ferroelectric
Moderator: Y. Liang, Pacific Northwest National Laboratory

9:40am **EL-MoM1 Quantitative Analysis of Piezoresponse Force Microscopy: Electrostatic vs. Electromechanic Interactions**, *S.V. Kalinin, **D.A. Bonnell**,* University of Pennsylvania

One of the critical aspects of the behavior of ferroelectric materials, both in the context of nano domains and for thin films, is the inter relation between atomic polarization and compensation charge. Piezoresponse force microscopy (PFM) has provided insight on domain structure and polarization reversal processes on the nanometer level. However, the imaging mechanism in PFM is complex in that both electrostatic and electromechanic interactions can contribute to image contrast. Here we analyze the electrostatic and electromechanical contrast in PFM using analytical solutions for the electrostatic sphere-dielectric plane problem coupled to Hertzian contact for the piezoelectric indentation problem. With this analysis local piezo electric properties can be quantified from traditional PFM and we suggest a novel variant that reduces the effects of system resonances to the contrast. The latter allows the measurement excitation and the domain switching bias to be decoupled. We use this approach on BaTiO@sub 3@ (100) to examine compensation charge and switching behavior.

10:20am **EL-MoM3 Template Sol-Gel Synthesis and Characterization of BaTiO@sub 3@ Nanostructures**, ***B.A. Hernandez**, K.C. Chang, E.R. Fisher, P.K. Dorhout,* Colorado State University

Barium titanate in both its cubic and tetragonal form has shown relevance in many applications. A high dielectric constant, ferroelectric behavior, and electro-optical properties make this material a candidate for many applications in the microelectronics industry (e.g. capacitors and DRAMs). Recently, thin films and submicron size particles of BaTiO@sub 3@ have been studied and have shown that dielectric and ferroelectric properties change as a function of grain size and density of the particles. To explain these effects, Landau-Devonshire theory has been applied to both thin film and particle geometry. As far as we know, no one has studied size effects in high aspect ratio BaTiO@sub 3@ nanostructure materials. Thus we have developed a synthetic strategy to produce high aspect ratio nanostructures via a sol-gel template method. A chelate sol-gel solution was made using Ba(OAc)@sub 2@ and Ti(Opr@super i@)@sub 4@. Whattman Anodisc Membranes with a 200 nm pore size were dipped into the solution, allowed to air dry, and then calcined to the appropriate temperature for the tetragonal or cubic phase. SEM analysis shows that the structures can be thought of as fibers with a 200 nm diameter and 50μm length. Powder X-ray diffraction, Raman Spectroscopy, and Differential Scanning Calorimetry of the structures confirmed the production of cubic and tetragonal phases when fired at 700°C and 900°C respectively. Dielectric behavior and polarization data also will be presented.

10:40am **EL-MoM4 Low-temperature Process of (Y@sub 0.95@,Bi@sub 0.05@)MnO@sub 3@ Ferroelectric Thin Film and its Structural and Electrical Properties**, ***T.J. Choi**, Y.S. Kim, J. Lee,* Sung Kyun Kwan University, Korea

(Y@sub 0.95@,Bi@sub 0.05@)MnO@sub 3@ (YBM) on Pt and Y@sub 2@O@sub 3@ buffered Si (100) have been prepared by pulsed laser deposition. Addition of Bi in YMnO@sub 3@ enhanced crystallization of YMnO@sub 3@ thin films. The c-axis oriented YBM films have been obtained on Pt and Y@sub 2@O@sub 3@/Si at 700 °C, which is lower deposition temperature than that of typical YMnO@sub 3@ films. The processing conditions of depositing oxygen partial pressure and cooling atmosphere have affected crystallization behavior and electrical properties of YBM films. At low oxygen partial pressures, (111), (112) and c-axis oriented polycrystalline nature were observed. As the oxygen pressure increased, YBM films intended to grow with c-axis preferred orientation. YBM deposited in oxygen pressure of 100 mTorr was strongly oriented along the c-axis at the substrate temperature of 700 °C. YBM grown on Y@sub 2@O@sub 3@/Si had a hysteresis curve with a clockwise direction, which indicates that the C-V hysteresis curve is caused by ferroelectric polarization switching. The memory window was about 2 V at a sweep voltage of 8 V.

11:00am **EL-MoM5 Effects of Bi/Sr Stoichiometric Ratio on Electrical Properties of Pt/SrBi@sub 2@Nb@sub 2@O@sub 9@/Si Ferroelectric Gate Structure**, ***Y.T. Kim**, S.I. Kim,* Korea Institute of Science and Technology, Korea*; I.H. Choi, H.S. Choi,* Korea University, Korea*; C.W. Lee,* Kookmin University, Korea

In comparison with high dielectric constant (k) isotropic ferroelectric materials such as Pb(Zr,Ti)O@sub 3@ (PZT), and PLZT for the storage capacitor, Bi-layered perovskite materials have relatively low k and some advantages such as excellent fatigue resistance, low leakage current. Especially, for MFSFETs, SrBi@sub 2@Nb@sub 2@O@sub 9@ (SBN) seems to be a promising candidate among the Bi-layered perovskite family because it has relatively lower k than SBT.@footnote 1@ It is well known that the lower k, the higher electric field is applied to the ferroelectric thin film.@footnote 2@ The high electric field causes greater memory window, which becomes now an issue for the application of MFSFETs as cell devices in the non destructive readout ferroelectric random access memory (NDRO-FRAM) with low voltage operation. In this work, in order to control the Bi/Sr stoichiometric ratio, we used SrNb@sub 2@O@sub 7@ and Bi@sub 2@O@sub 3@ targets with different powers of rf magnetrons. As a result, we have found that electrical properties are strongly sensitive to the Bi content. The capacitance-voltage (C-V) characteristics and memory windows of Pt/SBN/Si gate were investigated with various Bi/Sr content ratios. The memory window of the Pt/SBN/Si gate with the Bi/Sr ratio of 3.1 becomes 1.8 V at applied voltage of 3 V, which is the greatest memory window so far. However, the memory window gradually increases with increasing the Bi/Sr ratio in the SBN thin films, but when the Bi/Sr ratio becomes over than 3.1 the electrical properties such as memory window and breakdown voltage becomes to be degraded. The SBN thin film with Bi/Sr ratio of 3.1 has the (008) preferred orientation after annealing at 600°C for 1hr in O@sub 2@ ambient, which is relatively lower recrystallization temperature than that of other Bi-layered perovskite family. Particularly, in order to improve the memory window, it has been used to insert buffer insulators such as CeO@sub 2@, Y@sub 2@O@sub 3@, and YMnO@sub 3@,2). However, in this work, we can obtain the greatest memory window without a buffer insulator. @FootnoteText@ @footnote 1@ Y. T. Kim and D. S. Shin, Appl. Phys. Lett. 71, 3507 (1997) @footnote 2@ H. N. Lee, Y. T. Kim and Y. K. Park, Appl. Phys. Lett. 74, 3887 (1999)

11:20am **EL-MoM6 Recent Progress of Ferroelectric Memory Materials and FET-type FeRAMs**, ***H. Ishiwara**,* Tokyo Institute of Technology, Japan **INVITED**

A new class of ferroelectric materials was synthesized by adding sol-gel solution of a dielectric material to that of conventional ferroelectric materials such as PbZr@sub 1-X@Ti@sub X@O@sub 3@, SrBi@sub 2@Ta@sub 2@O@sub 9@, and Bi@sub 4@Ti@sub 3@O@sub 12@. It was found that the crystallization temperature of the new materials was decreased by 150°C to 200°C compared to the original materials and that the surface of the crystallized film was extremely flat. It was also found that the ferroelectric properties were almost the same as or even better than the original ones. Thus, a 13-nm-thick Bi@sub 4@Ti@sub 3@O@sub 12@-based film with a saturation polarization voltage of 0.5 V was obtained. Concerning the FET-type FeRAMs (ferroelectric random access memories), improvement of the data retention characteristics is most important. To improve the retention time, the buffer layer material, which was necessary to insert between the ferroelectric gate film and a Si substrate for preventing interdiffusion of the constituent elements, was optimized, as well as the structure of the ferroelectric-gate FET was carefully designed. As a result, MFIS (metal-ferroelectric-insulator-semiconductor) diodes with excellent characteristics were fabricated by combination of a Si@sub 3@N@sub 4@ buffer layer and a c-axis-oriented Bi@sub 4@Ti@sub 3@O@sub 12@ film. In order to further improve the retention characteristics, a prototype of the 1T2C cell was also fabricated, in which two ferroelectric capacitors with the same area were connected to the gate terminal of an MOSFET so that the depolarization field was not generated. In this cell, nondestructive readout operation up to 10@super 4@ times and the excellent data retention up to 17 hours were realized.

Manufacturing Science and Technology
Room 131 - Session MS-MoM

Metrology and Inspection for Manufacturing

Moderator: C.R. Brundle, Applied Materials

9:40am **MS-MoM1 Optical Digital Profiling for Production Applications**, ***K. Barry***, *J. Kretzschmar, N. Jakatdar,* Timbre Technologies, Inc. **INVITED**

As the industry drives down feature sizes, the need for more advanced characterization techniques becomes imperative. Gate lengths are quickly approaching the sub-one hundred-nanometer regime. Traditional techniques are not keeping pace with the precision and accuracy needs of the IC industry. Additionally, with the onset of 300mm wafer production, it will be imperative for tools to be able to measure critical parameters and adjust processing conditions on a wafer-by-wafer basis. The industry is experiencing a paradigm shift in critical dimension metrology. Optical Digital Profilometry (ODP), developed by Timbre Technologies Inc. (Fremont, Calif.), is an optical, nondestructive, in-line profile measurement methodology utilizing Maxwell's principles to generate digital cross-sectional representations of IC features. One advantage is that ODP has been proven extendible beyond the 70nm node by utilizing spectroscopic ellipsometry to measure physical structures with precision an order of magnitude better than currently available CD-SEMs. Another advantage lies in Optical Digital Profilometry's ability to generate digital cross-sectional information in real time enabling advanced process control (APC) of IC manufacturing lines. In this paper we present results from monitoring production wafers via ODP of shallow trench isolation (STI) structures at the post-etch, post-clean step, also referred to as final inspect (FI). These results show ODP to be a viable method for in-line CD, depth, and profile metrology, with sub-nm repeatability and excellent correlation to XSEM and CD-SEM.

10:20am **MS-MoM3 Critical Dimension and Profile Measurement by Optical Scatterometry for Sub-0.15 µm Advanced Gate and Shallow Trench Isolation Structures**, ***D. Mui***, *H. Sasano, J. Yamatino, M.S. Barnes, K. Fairbarn,* Applied Materials

The use of a non-destructive optical scatterometry (OS) technique for measuring critical dimensions (CD) and cross-sectional profiles in advanced gate and shallow trench isolation (STI) structures with sub-0.15 µm feature size has been evaluated. Conventional scanning electron microscopy (SEM) technique was used as the reference for comparison. 8" Si wafers with various feature sizes and profiles were used in this study. A bias between optical-CD (OCD) and SEM-CD measured on the same feature was observed. Measurements on different OS tools from different vendors showed consistently smaller CDs than those measured on a SEM tool. This CD bias was observed to be profile dependent ranging from 2 to 20 nm in our study. Good correlation between the two CD metrologies was obtained for a given wafer when a constant bias was added to the OCD data set. For profile comparison, various profiles including - bowed, tapered, notched, and vertical, were etched and measured. In general, good correlation was obtained between the non-destructive OS and destructive SEM techniques.

10:40am **MS-MoM4 Wafer Inspection with HDI Surface Reflectance Analyzer**, ***A. Surdutovich***, *G. Conti, H.T. Nguyen, H. Hao,* Applied Materials*; G.H. Vurens,* HDI Instrumentation

Scanning Reflectance Analysis (SRA) is being widely used in the hard disk industry for metrology of thin film disks. The technique has been evaluated for wafer inspection. This technique provides a means to generate high resolution maps of thickness variation and empirical chemistry variation of films on a wafer in less than one minute. Low k CVD films have been measured with HDI SRA and an application has been developed for mapping out separately chemical and thickness variations across the whole wafer area. Detection of organic contamination on Cu seed film has also been investigated.

11:00am **MS-MoM5 Using SQUIDs for Failure Analysis in the Semiconductor Industry**, *T. Venkatesan, L.A. Knauss,* ***A. Schwartz***, Neocera, Inc. **INVITED**

With the arrival of flip-chip packaging and multi-level metallization on dies, present tools and techniques are having increasing difficulty in meeting failure analysis needs. Recently a magnetic field imaging system has been demonstrated to localize shorts in buried layers of both packages and dies. This system uses a SQUID (Superconducting Quantum Interference Device), which is a very sensitive magnetic sensor that can image magnetic fields generated by magnetic materials or currents (such as those in an integrated circuit or package). These currents (as low as microamperes) can be detected even when they are buried deep within a package or assembly. Since magnetic fields are not affected by most materials used in circuit technology, magnetic field imaging can be applied to several vertical layers enabling problem detection in a multi-layer stack involving the die, solder bumps, package, BGA and board. The current density distribution in the sample can then be calculated from the magnetic field image providing a map of current flow in the assembled device. This can be helpful for design verification and short localization, including determining which layer of the structure contains the defect. To image these devices, the SQUID must be cooled to temperatures around 77K while the sample is at room temperature. In order to image these parts non-invasively, the system has been designed to keep the SQUID cold and in vacuum while the sample is at room temperature in air. The design of this system as well as the application to failure analysis will be presented. Peak localization of defects to ± 5 microns has been demonstrated in the best case with sub-10 microns being typical.

11:40am **MS-MoM7 Development of a 300 mm Wafer Defect Analysis Tool Integrating High Resolution Auger Spectroscopy and Ultrahigh Resolution Immersion Lens SEM Microscopy**, ***W.K. Ford***, *M. Jaehnig, P. Hudson,* Intel Corporation*; T. Dingle, K. Troost, L. Christman, J. Jackman, M. Verheijen,* FEI Company*; P. Belcher,* Thermo VG Scientific

The challenge of defect analysis and material characterization in a Si semiconductor fab becomes increasingly difficult with each process generation. Scaling steadily decreases the size of circuit features, permitting smaller and smaller particle defects to impact the yield of the device. Simultaneously, nanometer-scale thin films are commonly being used as gate dielectrics, metal adhesion and barrier layers, and interfacial treatments. These two trends produce challenges to process development and manufacturing that can be addressed using surface analytical tools such as the Auger microscope. This paper describes the development of an advanced Auger microscope believed suitable for 0.13 µm, 0.10 µm, and 0.07 µm process generations. It is in this range that the large excitation volume of the electron beam even at the lowest practical primary beam energy renders as ambiguous the commonly used x-ray analysis (EDS) methods, and that ultra sensitive mass spectroscopy (TOFSIMS) fails to have suitable lateral spatial resolution. The Auger microscope described herein has been developed using an immersion mode objective lens for ultimate imaging capability, providing simple, rapid transition between ultra high resolution SEM imaging and Auger spectroscopy. It is based on a UHV 300 mm wafer-capable platform using industry standard interfaces and incorporates a new, highly effective stage technology, which provides for the required stage navigation accuracy and speed, versatile sample positioning including high angle tilting, and full integration with standard CAD software interfaces. A high sensitivity Auger detector is used that provides the high spectral energy resolution often required for chemical analysis. These capabilities will be demonstrated using a full range of examples derived from Si process development and manufacturing.

Manufacturing Science and Technology
Room 131 - Session MS-MoA

Manufacturing Technologies for the Information Industry
Moderator: M. Surendra, IBM T.J. Watson Research Center

2:00pm **MS-MoA1 Silicon on Insulator for 100 nm Generation System on Chip*, G. Shahidi,*** IBM Microelectronics Division **INVITED**

SOI CMOS has become a mainstream CMOS technology. In this paper, we will first give a brief overview of the key attributes and challenges of SOI CMOS. As we scale CMOS into 100 nm and beyond, SOI opens novel opportunities, where bulk CMOS is approaching its limits. We will review the extendibility of benefits of SOI (performance gain and floating body effects at 100 nm and beyond). SOI opens some very exciting opportunities in RF CMOS, low power, and other elements needed for system on chip. SOI CMOS is the technology to use when high performance, low power, and capability to easily integrate other needed elements for SOC, at CMOS generations beyond 100 nm.

2:40pm **MS-MoA3 Integrated Circuit Challenges for sub-100nm Generations*, M. Bohr,*** Intel Corp. **INVITED**

This talk will cover the challenges faced as transistors and interconnects are scaled to sub-100nm dimensions and review some of the device and material options being investigated to meet these challenges.

3:20pm **MS-MoA5 The Future for Storage Technology and Manufacturing*, M. Re,*** Read Rite Corp. **INVITED**

4:00pm **MS-MoA7 An Overview of Manufacturing Processes of Some Passive and Active Components for Fiberoptic Communication Networks*, N.A. O'Brien, S.P. Sapers,*** JDS Uniphase Corporation **INVITED**

The wide proliferation of the Internet in the mid 1990s has led to an exponential growth in bandwidth demand. The fiberoptic communications industry was faced with the option of installing more fiber and increasing the bit rate from 10 Gbit/sec in the existing communication systems by, time division multiplexing (TDM). In TDM systems, multiple signals of one wavelength are transmitted through a single fiber but are distinguished from each other by specific time intervals. That option was not economically viable. Wavelength division multiplexing (WDM) emerged as the new technology that increases the capacity of existing fiber by sending multiple (multiplexing) wavelengths down one fiber. The total bandwidth per fiber is the sum of the bit rate of each wavelength. Systems have been built with up to 128 wavelengths per fiber. There are several competing technologies that are employed for multiplexing and demultiplexing such as thin film interference filters, fiber Bragg gratings, and arrayed waveguide gratings. While WDM has kept up with the increase in bandwidth demand, fiberoptic communication systems still rely on optical-to-electrical conversion for switching purposes. This leads to inflexibility of the systems, increased maintenance, and high costs. There exists a great need to have an all-optical network. Recent developments in micro-electro mechanical systems (MEMS) provide a great promise towards making that a reality. MEMS are nanodevices. They are often likened to integrated circuits (ICs) due to similarities in size and manufacturing methods, except ICs route electrons and MEMS can route photons. WDM filter technology has matured and has become yesterdayâ€™s news, while MEMS applications remain in development stages but near commercialization. This presentation is structured to talk about WDM filter technologies and MEMS in the context of passive and active devices respectively, with emphasis on the manufacturing processes.

4:40pm **MS-MoA9 Scientific Challenges in Harnessing Molecules for Electronic Devices*, D.L. Allara,*** Pennsylvania State University **INVITED**

Recent work has shown that molecules are capable of functioning as electronic components such as resistors, diodes and switches. These fundamental properties, in principle, can lead to new generations of devices and computing machines. However, many fundamental challenges lie ahead as the implementation of these technologies begins. These challenges include issues of chemical assembly, lithographic scales and electrical contacts. These and other aspects will be presented and discussed from a broad point of view with an emphasis on the underpinning science that is needed to help enable process development.

Manufacturing Science and Technology
Room 134/135 - Session MS-MoP

Aspects of Manufacturing Science and Technology Poster Session

MS-MoP1 Investigations on Post Cu CMP Cleaning of Colloidal Silica Slurry, *T.-C. Wang, T.E. Hsieh, S.-Y. Chiu,* National Chiao Tung University, Taiwan, R.O.C.*;* ***Y.-L. Wang,*** Taiwan Semiconductor Manufacturing Company*; J.J. Chang,* National Chiao Tung University, Taiwan, R.O.C.*; Y.-N. Shieh,* Chang Chun Petrochemical Co., Ltd., Taiwan

Chemical mechanical polishing (CMP) is the only way to achieve the global planarization in copper damascene process. In addition to complex consumables and process controls, one of the key issues in mass manufacturing using CMP technology is post-CMP cleaning. In this study, novel clean solutions for efficient removal of colloidal silica from polished copper line were proposed. There were three kinds of formulated post Cu CMP cleaning solutions carried out including PVA, Dextrose and D-sorbitiol aqueous solution. Cleaning with these chemistries was able to change the character of the colloidal silica abrasive surface and eliminate the strong tendency of the absorption of colloidal silica on copper line. From the SEM images of polished copper surface, abrasive-free Cu surface could be obtained. Besides, the surface-scan for defect analysis performed a different level for Cu CMP post-clean efficiency. In addition, the electrical analyses for polished pattern wafers cleaning were evaluated to verify the performance of these formulated clean solutions.

MS-MoP2 In-Situ EIS Approaches to the Copper CMP Slurry Characterization, ***S.-Y. Chiu,*** National Chiao Tung University, Taiwan, R. O. C., R.O.C.*; J.-W. Hsu, Y.L. Tasi,* National Tsing Hua University, Taiwan, R. O. C.*; Y.-L. Wang,* Institute of Materials Science and Engineering, Taiwan, R. O. C.*; M.-S. Tsai,* National Nano Device Laboratories, Taiwan, R. O. C.*; H.C. Shih,* National Tsing Hua University, Taiwan, R. O. C., TAIWAN*; M.-S. Feng,* National Chiao Tung University, Taiwan, R. O. C., R.O.C.

In the chemical-mechanical polishing study, slurry chemistry in chemical-mechanical polishing of Cu thin film has been evaluated in various slurries. Various types of oxidizer and inhibitor were changed in the concentration and slurry pH were investigated. In nitric acid based slurry, with both H+ and NO3- present, it provides a corrosion environment for copper. With citric acid present in slurry system, it plays a role of formation a native passivation film on the surface. The polishing rate of copper increases as the concentration of HNO3 increases or citric acid decreased. In H2O2 based slurry, H2O2 both dissolute of copper and form a cupreous oxide passivation surface. H2O2 is a strong oxidizer, it provides a potential to copper to be oxidized, maybe cupric ion or cuperous oxide simultaneously. For small amount of H2O2 adding in acidic region, it increase the dissolution the copper that increase the polishing rate of copper. With more H2O2 in slurry, the oxide film formation rate increases and the dissolution rate of copper decreases, as a result the CMP removal rate of copper film decreases. With Benzotriazole(BTA) present in HNO3 based slurry, BTA passivated the copper surface from HNO3. And the copper removal is conducted by the abrasive polishing off the BTA from the copper surface then etching the copper surface by HNO3. In this study, we wish to investigate the concentration of oxidizer and inhibitor effect in acidic slurry system on the polishing mechanism of copper CMP. Electrochemical impedance-spectroscopy (EIS) measurements were applied in order to obtain a better fundamental understanding of the electrochemical reaction and the physical model of copper in the CMP process.

MS-MoP4 Line Type SAC with Oxide Spacer(LSOS) Adopting Flowfill Oxide for 0.10µm Design Rule and Beyond, ***S.C. Park,*** *S.D. Lee, S.T. Ahn, J.C. Ku, D.S. Kim, J.W. Kim, H.K. Yoon,* Hynix Semiconductor, Inc., Korea

In this study, we used Flowfill oxide in the Line-type SAC with Oxide Spacer(LSOS) process, a storage node contact formation technology for DRAM devices. During our LSOS process, a bit-line sidewall was formed after SAC etching, which substantially reduced the aspect ratio of ILD gap-fill process.@footnote 1@ However, for 0.10µm design rule and beyond, even when the LSOS process was applied, small voids were created because conventional High Density Plasma(HDP) oxide was not able to fill the gap between bit-lines. Therefore, we selected Flowfill oxide as a novel InterLayer Dielectric(ILD) material instead of HDP oxide. The key attribute of Flowfill oxide is a unique chemistry of SiH@sub 4@ and H@sub 2@O@sub 2@, which generates a liquid-like intermediate compound that fills very narrow gaps and provides excellent planarity.@footnote 2@ In this experiment, to deposit the Flowfill oxide, TRYKON Planar 200 system was used. A higher Si@sub 3@N@sub 4@ selectivity was obtained when Flowfill oxide was used during the SAC etching, compared to HDP oxide. To find the exact cause of such a high selectivity with Flowfill oxide, X-ray Photoelectron Spectroscopy(XPS) was used to analyze partially etched Flowfill oxide and HDP oxide sample. The XPS analysis showed that a thicker fluorocarbon film was formed on Flowfill oxide and the carbon concentration of the fluorocarbon film was higher on Flowfill oxide. The difference of fluorocarbon film can be due to the presence of hydrogen in Flowfill oxide. In addition, we found that even though Flowfill oxide was annealed for the purpose of densification, nano-pores were created at the bottom of the gap between bit-lines. These nano-pores resulted in a partial stoppage of the SAC etching process, so we had to remove the remaining layer during the sidewall etching. Furthermore, we were able to check the practicality of the LSOS process with Flowfill oxide by fabricating a 256Mb density test vehicle having 0.10µm design rule. @FootnoteText@ @footnote 1@ K.H. Yoon, S.C. Park, et. al.,Symp. on VLSI Tech. Dig., 2001, in press. @footnote 2@ M. Matsuura, et. al., IEDM Tech. Dig., 1994, P.117

MS-MoP5 Application of Plasma V@sub dc@ Bias Diagnostics Cathode For Device Charging Damage Optimization, ***S. Ma,*** Applied Materials*; K. Horioka,* Applied Materials, Japan*; R. Lindley, K. Doan, S. Kats, M. Dahimene, Y. Xia, H. Shan,* Applied Materials

It is highly desirable to investigate the potential plasma damage issues as early as in the stage of plasma process chamber development without processing the real device wafers. Therefore a diagnostic tool is required to give reliable relationship to real device plasma damage and fast feedback on any process or hardware change. In this paper, a V@sub dc@ bias diagnostic cathode is used to measure the plasma induced self bias uniformity across the wafer and the correlation to device charging damage. A Magnetically Enhanced Reactive Ion Etching (MERIE) chamber is used to install this diagnostic cathode. Multiple probe pins are buried within the electrostatic chuck surface with only the top surface tips exposed to plasma. Wafer surface DC bias voltage during plasma process can be directly measured from these probes simultaneously with built-in circuitry. Real-time analysis of V@sub dc@ bias is thus feasible by multi-channel recording of bias evolution. The maximum bias difference (@delta@V@sub dc@ = V@sub dc(max)@ - V@sub dc(min)@) between the maximum and the minimum value of simultaneously measured V@sub dc@ across the cathode surface can be used to correlate to the potential driving voltage on the wafer to generate device damaging current during plasma process. Compared to real antenna MOS capacitor device damage data under similar process conditions, when @delta@V@sub dc@is less than a threshold around 12V then plasma induced charging damage is not a concern. This method also shows successful examples of different process recipes and hardware optimization to meet industrial device plasma damage spec.

Manufacturing Science and Technology
Room 131 - Session MS-TuM

Process Integration and Factory Productivity
Moderator: S.S. Shankar, Intel Corporation

8:20am **MS-TuM1 Reduction in Loadlock Vent Time and Particles through Use of Fast Vent Diffuser**, *C. Adcock,* Mykrolis Corporation (Formerly the Microelectronics Division of Millipore Corporation)*; H. Dang,* Texas Instruments Inc.*; J. Gratz, M. Randolph,* ***J. Snow****, C. Tsourides,* Mykrolis Corporation*; R. Wheeler,* Millipore Corporation

Improvements to semiconductor manufacturing equipment effectiveness can be directly impacted by enhancements in tool throughput and/or product yield. One area for these improvements is system loadlocks. Reducing loadlock vent-up time from vacuum to atmospheric pressure increases tool throughput. Additionally, reducing particle adders in the loadlock increases product yield. Traditionally, a soft vent procedure has been used in an attempt to balance loadlock vent-up time with reduced particle generation. While some particle control is achieved, vent-up times are often in excess of ten minutes - not an optimal solution. Gas diffuser technology has been developed and integrated with filtration technology to enable faster vent-up of loadlocks while simultaneously decreasing particle adders on the wafer. This is accomplished using a "specially formulated" sintered porous metal membrane, which provides laminar flow across the entire diffuser surface. Vent gas volume is maximized while gas velocity at the loadlock entrance is minimized. Results from two independent evaluations with diffusers will be presented. First, tests conducted at an equipment manufacturer will demonstrate an 80% reduction in vent time with no adverse effect on particle performance. Second, on-tool performance at a semiconductor manufacturing facility will highlight the reduction in wafer particle adders.

8:40am **MS-TuM2 Cleaning Procedures in Wafer Processing: Analytical Challenges for Root Cause Determination of Particle Problems**, ***C.C. Wang,*** *Y.S. Uritsky, C.R. Brundle,* Applied Materials, Inc.

Common dry clean procedures used in the wafer processing industry are: substrate pre-clean of individual wafer prior to deposition (gentle Ar@super +@ sputter), and hardware clean after many processed wafers to remove the sputtered material build-up (harsh NF@sub 3@ usually). Particle failures can result from both procedures, however, and are a severe industry problem. In the Ar@super +@ pre-clean a gradual build-up of by-products of cleaning occurs on chamber surfaces. These can chemically react with the hardware material, releasing composite particles through stress (proven by detailed particle morphology observation). In the NF@sub 3@ case, the fluorine radicals, intended for removing deposits by forming volatile products, often attack hardware itself producing particles. In both cases particle analysis is critically needed to determine exactly what piece of hardware is being attacked and by what mechanism for the purpose of hardware and process improvements. The sophistication of the analytical work required for finding root cause is high. In this paper we describe how careful SEM/EDX work, supported by FIB and Raman/Photoluminescence, identified root cause in both NF@sub 3@ and Ar@super +@ clean particle failures. In the NF@sub 3@ case the critical issue was to establish, without any doubt, that generated particles scavenged by an oxide monitor wafer, contained no oxygen and only Al and F. In the Ar@super +@ pre-clean case it was demonstrated that particles consisted of thin, plate-like bi-layers of sputtered substrate material (SiON in this case) and amorphous Al@sub 2@O@sub 3@ from the surface of the plasma degraded ceramic dome. In both cases modeling the EDX spectra using STRATAGEM@footnote 1@ software for multi-layer thin film structures (and here applied to particles) was important in reaching definitive conclusions, which were then used in the successful defect reduction actions. @FootnoteText@ @footnote 1@ STRATAGEM is a registered trademark of SAMx.

9:00am **MS-TuM3 High Productivity Plasma Etch Reactors: Hardware and Chemistry Concepts**, ***D. Podlesnik,*** Applied Materials **INVITED**

9:40am **MS-TuM5 Data Driven Manufacturing**, ***C.J. Spanos,*** University of California, Berkeley **INVITED**

Manufacturing has evolved through several stages: From handmade parts, to interchangeable components, from scientific management and statistical process control to numerical control, and finally to intelligent machine tools and flexible production facilities. While it took over 200 years for traditional manufacturing to mature, semiconductor manufacturing advanced through all these stages in four short decades. More so than in other types of manufacturing, today's semiconductor manufacturing is "data driven" in many levels of abstraction. Much like traditional manufacturing, there is tremendous data infrastructure at the factory level, monitoring parts movement, recipes, consumables, etc. Unlike traditional manufacturing, however, there is also data driving the production at the process or tool level. Examples here include the sophisticated control and diagnosis databases that often describe individual process steps of critical nature, such as plasma etching, photolithography and Chemical-Mechanical Planarization. An additional example of unusual datasets in semiconductor manufacturing has to do with the large amount of wafer or work-piece data, collected to monitor tooling, to predict yield, to drive control applications, and to also drive the evolution of semiconductor manufacturing technology. This talk will examine this hierarchy of data in semiconductor manufacturing, and it will specifically focus on the interactions between the various levels. Examples will be given regarding critical deep sub-micron patterning steps of the semiconductor manufacturing sequence.

10:40am **MS-TuM8 Gate Module Integration with High k Dielectrics**, ***S.W. Butler,*** Texas Instruments **INVITED**

Due to silicon dioxide being unable to meet future gate dielectric thickness and leakage requirements, silicon dioxide as a gate dielectric is being replaced with a higher k material, such as a metal silicate. Switching from silicon dioxide to a higher k dielectric involves more than just changing the dielectric. Although the goal is to minimize changes to a traditional CMOS flow, this paper will discuss the reality of the types of changes that must be made for the transistor to achieve improved performance and meet the SIA Roadmap requirements. Temperature changes are the most common type of change considered. However, there are more subtle process and flow changes which can be quite insidious and their impact must be understood. Contamination concerns may also drive process changes, but are more likely to cause procedural or manufacturing system changes. Such changes may be considered more expensive by a production fab than a process or equipment change.

Manufacturing Science and Technology
Room 131 - Session MS-TuA

In Line and In Situ Process Control

Moderator: E.G. Seebauer, University of Illinois, Urbana-Champaign

2:00pm **MS-TuA1 Plasma Etch Endpoint and Diagnostic Fault Detection Using Evolving Window Factor Analysis**, ***H.M. Anderson,*** University of New Mexico*; S. Gunther, B. Fry,* CETAC Technologies

Array detector based systems with statistical analysis capability integrated with real-time data acquisition can provide a wealth of spectral information from a variety of potentially useful gas phase emitting species. In the case of particularly challenging applications such as low-open area self-aligned contact (SAC) etches, utilization of the full optical emission spectrum has been shown to accurately detect endpoint when all other endpoint systems studied failed. Production facility results regarding these and other demanding applications will be presented. The talk will largely focus on oxide etching in AMAT MXP and TEL DRM platforms. Evolving Window Factor Analysis (EWFA) is the principal multivariate techniques used in the analysis. They allow one to dynamically track the principal components of the oxide etch process. EWFA is also shown to useful for automatic fault detection.

2:20pm **MS-TuA2 Characterization of Pattern Transfer from Litho to Etch Using Scatterometry**, ***T.G. Dziura,*** *U. Whitney, A. Levy,* KLA-Tencor*; G.P. Kota, G. Peng, R.A. Gottscho,* Lam Research

Gate pattern transfer from the lithography after-develop-inspect (ADI) step to post-gate-etch clean was characterized with spectroscopic CD (SCD) measurements on a KLA-Tencor F5-SCD metrology platform. Data were collected on resist-BARC-a-Si gate-gate oxide-Si grating structures at ADI, post-BARC-etch, post-gate-etch, and after-clean-inspect (ACI). Three different gate etch processes were applied using a Lam Research TCP@super ®@ 9400DFM etcher to produce varying sidewall profiles. Measurements were made on grating targets with nominal CD ranging from 75 - 160 nm, and line/space ratios 1:1, 1:3, and 1:5. Both wafer map data and dynamic short-term repeatability data were collected. The profiles obtained were compared to cross-sectional SEM (XSEM) measurements. The CD bias between litho, BARC etch, and gate etch was measured for different nominal CDs and line-to-space ratios. The results indicate that SCD provides enhanced information for optimizing etch processes. Wafer maps of profile parameters can be measured at different stages of the process and correlation coefficients calculated between selected pairs of parameters provide insight into the pattern transfer process. The significantly increased resolution of SCD measurements enables more accurate and detailed process models.

2:40pm **MS-TuA3 Chamber Wall Monitoring and Control for Plasma Etching Reproducibility**, *S.J. Ullal, T.-W. Kim,* University of California, Santa Barbara*; H. Singh, J. Daugherty, V. Vahedi,* Lam Research Corporation*;* ***E.S. Aydil,*** University of California, Santa Barbara

Wafer-to-wafer process reproducibility is one of the major concerns in plasma etching of thin films. Production of a uniform plasma with the same ion density, electron temperature, and species concentrations wafer after wafer is a major challenge. The plasma chamber walls play a crucial role in determining these discharge properties and remain as one of the major sources of irreproducibility. The problem of process sensitivity to the wall conditions has been known for a long time but its management has remained an art. Thus, it is critical to monitor the wall conditions and the nature of the films and adsorbates that are deposited on the walls. Towards this end, we have developed a surface probe based on in situ multiple total internal reflection Fourier transform infrared (MTIR-FTIR) spectroscopy that can be used as a diagnostic to monitor the films and adsorbates on the walls of both plasma etching and deposition reactors. This surface probe was used to study the nature of the species present on the walls of the chamber and process repeatability during Cl@sub 2@/O@sub 2@ plasma etching of Si. This etching process is particularly challenging because SiCl@sub x@ etching products react with O atoms to deposit a SiO@sub x@ Cl@sub y@ film on the chamber walls, which must be cleaned with an SF@sub 6@ plasma to ensure reproducible wall conditions. Infrared spectra of the films depositing on the walls were collected in real time during Cl@sub 2@/O@sub 2@ plasma etching of Si and during the SF@sub 6@ cleaning steps to determine and monitor the effect of each process step and the reproducibility of cleaning. The surface probe was used to minimize the duration of the cleaning step to maximize throughput and to develop cleaning strategies to improve wafer-to-wafer repeatability. Subtle drifts in etch profile shapes could be detected through the use of the MTIR-FTIR probe even though these drifts are not detected through etch rate measurements and other monitoring methods.

3:00pm **MS-TuA4 Integrated RF Sensor for Accurate Control and Monitoring of on Wafer Process Performance**, ***A.M. Paterson,*** *J.M. McChesney, V. Todorov,* Applied Materials*; J. Holland,* Applied Materials, US*; M.S. Barnes,* Applied Materials

As the semiconductor industry moves to 300mm wafer size, it has become essential to have accurate and reliable knowledge of the RF and DC parameters experienced by the wafer being processed. Use of a RF sensor integrated on to the tool will provide accurate information useful for process optimization and repeatability analysis, however, correct placement of the sensor in the RF circuit is essential. Placement of the sensor directly in the wafer pedestal can make the design complicated, more expensive, and less accessible. This paper describes a more reliable method for obtaining the absolute RF and DC parameters on the wafer. This method utilizes accurate knowledge of the complete cathode impedance and an accurate circuit model describing the observed impedance. Accurate knowledge of the cathode impedance allows the RF sensor to be remotely placed, in our case in the RF match box, so that complicated cathodes designs can be avoided. Extensive work has shown that knowing the RF parameters at the output of the match, and the impedance of the cathode, that the RF and DC parameters calculated at the wafer are in excellent agreement with those values actually measured on the wafer. This method then allows for accurate chamber matching, endpoint and process control. Voltage compensation of the electrostatic chuck voltage in order to offset the effects of DC bias is also determined from this integrated probe. Other features of the RF sensor will also be discussed.

3:20pm **MS-TuA5 Fault Identification and Classification using a Plasma Impedance Monitor**, ***M.P. Hopkins,*** *K. O'Leary,* Scientific Systems, Ireland **INVITED**

Semiconductor production fabs regularly encounter faults which result in unscheduled tool downtime. Among these are real-time tool faults, preventative maintenance recovery problems and tool mis-matching at start-up and process transfer. This downtime can be reduced by applying a Fault Detection and Classification scheme where the core problem is identified as rapidly as possible, replacing the usual "trial-and-error" approach to fault identification. Scientific Systems have developed a non-intrusive, high-resolution impedance sensor which is designed to aid fault identification. The sensor is used to characterize a baseline process, operating within control limits, by measuring the Fourier components of RF voltage, current and phase. This results in a unique impedance fingerprint of the chamber. When a fault condition occurs, the impedance fingerprint varies in a predictable pattern. By comparing the fault fingerprint to the baseline, it is possible to classify faults through a diagnostic methodology. Using the system, hardware problems can be separated from process issues and changes in individual process inputs can be identified. We report a number of case studies where the system has been successfully deployed.

4:00pm **MS-TuA7 Real-Time CVD Wafer State Metrology using a Downstream Acoustic Sensor**, ***L. Henn-Lecordier,*** University of Maryland, US*; J.N. Kidder, G.W. Rubloff,* University of Maryland*; A. Wajid, C.A. Gogol,* Inficon, Inc.

An acoustic gas sensor, the Inficon Composer@super TM@, was implemented downstream in a production-scale tungsten chemical vapor deposition (CVD) cluster tool for process sensing to achieve real-time, in-situ film thickness measurements. Process gases were sampled at the reactor outlet and compressed with a diaphragm pump from the 10 Torr process pressure regime to above 50 Torr as required for gas sound velocity measurements in the acoustic cavity. Processes were carried out for various deposition times at 10 Torr, with a H@sub 2@ / WF@sub 6@ flow ratio of 6 to 1 and at wafer temperatures ranging from 300 to 450 °C. The sensor measures the average molecular weight of the gas mixture and is normally employed for control of inlet (upstream) gas flows into the reactor. For downstream applications, depletion of the H@sub 2@ and WF@sub 6@ reactants, as well as generation of the HF product, shift the gas composition with changes in reaction rate in the process. The high depletion rate of the WF@sub 6@ precursor (i.e. 30% or more) during blanket W deposition induced a substantial variation of the average molecular weight of the exhaust gas mixture. By integrating the resonant frequency over the deposition time, real-time in-situ metrology signals

were obtained which correlated to post-process thickness measurements within 1%. This makes the acoustic sensor attractive for advanced process control, either in run-to-run control or through real-time end point control.

4:20pm **MS-TuA8 Thickness Metrology and Real-Time End Point Control in W CVD using in-situ Mass Spectrometry@footnote 1@**, *Y. Xu,* University of Maryland*; L. Henn-Lecordier,* University of Maryland, US*; T. Gougousi, G.W. Rubloff,* ***S. Cho****, Y. Liu,* University of Maryland

In-situ downstream mass spectrometry has been employed in W CVD processes for real-time reaction sensing, thickness metrology, and real-time end-point process control. In the silane reduction process for depositing W CVD from SiH@sub 4@ + WF@sub 6@ using an Ulvac ERA-1000 cluster tool, high reactant reactant conversion rates were obtained at 200-250°C. Both depletion of the SiH@sub 4@ reactant and generation of the H@sub 2@ and SiF@sub 4@ reaction products provided real-time thickness metrology signals which correlated with post-process, ex-situ film thickness measurements with an uncertainty better than 2%. These metrology signals were used as end-points to terminate the process in real-time, leading to corresponding control of the mass spectrometry derived signal even in the presence of random run-to-run process fluctuations and systematic drift intentionally introduced as a run-to-run temperature drift. Actual film thicknesses as measured post-process were controlled to within 3% using this mass-spec-based end-point control. These results demonstrate that downstream mass spectrometry provides real-time thickness metrology suitable for real-time as well as run-to-run process control. Furthermore, the real-time end pointing capability enables compensation for random process fluctuations as well as systematic process drift. @FootnoteText@ @footnote 1@Present affiliations: Y. Xu (IBM Microelectronics, Hopewell Junction, NY); T. Gougousi (North Carolina State University, Raleigh, NC).

4:40pm **MS-TuA9 In-situ FTIR Spectroscopy for Metrology of a Tungsten CVD Process**, ***A. Singhal***, University of Maryland*; L. Henn-Lecordier,* University of Maryland, US*; J.N. Kidder,* University of Maryland*; C.A. Gogol, J.F. Kushneir,* Inficon, Inc.

A Fourier Transform Infrared Spectrometer has been employed for downstream detection of reactants and reaction products in a tungsten chemical vapor deposition process. The objective of this work was to monitor reactant and product concentrations for metrology of the deposition rate on the wafer. The spectroscopy system includes a novel compact interferometer and a heated optical cell with purged optics. Measurements of the gas composition directly downstream of the wafer were done using a pumped sampling system to extract gases from the low pressure CVD process to the optical cell. Experiments showed a linear correlation between the gas concentration in the deposition chamber and the intensity of absorption features detected at the sampling optical cell. In experiments with repeated wafer load/unload and process flow sequences there was no significant drift in the detected steady-state intensity of absorption peaks. In measurements done during deposition process runs at a range of conditions the intensity of absorption features associated with a reactant (WF@sub 6@) and a principal reaction product (HF) were detected and correlated to the weight gain on the wafer for in-situ metrology of the deposition rate.

5:00pm **MS-TuA10 New Mass Spectrometer without Fragment Ions for CVD In-situ Monitoring**, ***Y. Shiokawa***, *M. Nakamura, K. Hino, T. Sasaki,* Anelva Corporation, Japan

In-situ gas monitoring of CVD depending on complicated reactions is more essential and has three objects; residual gases, materials and byproducts (precursors). Residual gases can be measured but the others are difficult by a conventional mass spectrometer using electron impact (EI) ionization. The reason is fragmentation; molecules with low binding energy for CVD are inevitably dissociated and become fragment ions. Therefore, we have developed a new apparatus as commercial product by means of Ion Attachment Mass Spectrometry (IAMS),@footnote 1@ in which a metal ion attaches to a molecule and the excess energy is so small that fragmentation could be avoided. First, we measured PFCs gases exhausted from a plasma-etching system.@footnote 2@ The mass spectra by IAMS showed every natural molecular ion corresponding to materials and byproducts, while not molecular ions at all but merely many fragment ions by EI. So, some diagnostics as well as monitoring was done. Next, we have applied to CVD. Some parts about gas introduction and metal ion emission have been improved because CVD gases are more adsorptive and adhesive. The apparatus, connected to the process chamber of Plasma-CVD, measured SiH@sub 4@, NF@sub 3@ and others as molecular ions. On the other hand, although a metallic-organic molecule for Cu deposition by MO-CVD has very low binding energy, its molecular ion was successfully detected. In-situ monitoring of MO-CVD using low vapor pressure materials is especially desired and seems to be realized by IAMS. We would like to present some examples of CVD in-situ monitoring throughout our talk. @FootnoteText@ @footnote 1@ T.Fujii, Mass Spectrometry Review 19 (2000) 111 @footnote2@ M.Nakamura et al JVST-A Vol.19,No4 (2001) to be published

Dielectrics
Room 130 - Session DI-WeA

Low K Dielectrics
Moderator: Z. Yu, Motorola Labs

2:00pm **DI-WeA1 Materials Issues and Recent Development of Low k Dielectrics for Advanced Interconnects**, ***P.S. Ho,*** The University of Texas at Austin **INVITED**

Materials Issues and Recent Development of Low k Dielectrics for Advanced Interconnects Low k dielectrics are being developed for on-chip interconnects beyond the 0.13 micron generation. To replace silicon dioxide, there are stringent requirements on materials properties imposed on the low k dielectrics. The challenge is how to maintain the thermomechanical properties of the material while decreasing its dielectric constant, particularly for porous materials with dielectric constant less than 2. In spite of this difficulty, several materials have been developed and process integration demonstrated recently. The materials issues and characterization of low k dielectrics will be presented. Recent developments based on optimization of molecular structures will be discussed.

3:40pm **DI-WeA6 Formation of Self-Assembled Molecular Layers on the Low Dielectric Porous Methyl Silsesquioxane**, ***J.C. Hu,*** *C.W. Wu, L.J. Chen,* National Tsing Hua University, Taiwan, R.O.C.*; C.H. Li,* National Chiao Tung University, Taiwan, R.O.C.*; T.C. Chang,* National Sun Yat-Sen University, Taiwan, R.O.C.*; C.J. Chu,* Nanmat Technology Co., Taiwan, R.O.C.

Porous methyl silsesquioxane (PMSQ) with a low dielectric constant (~1.8) is of great interest for ULSI applications. However, many hydrophilic methyl groups (-CH@sub 3@) on the PMSQ were destroyed under O@sub 2@ plasma ashing. Hydroxyl groups (-OH) were bonded with Si dangling bonds on the PMSQ films. H@sub 2@ plasma post-treatment is usually used to decrease -OH bond formation. In the present work, bottom-up growth behavior of self-assembled molecular layers (SAMs) on the PMSQ was investigated. Diclorodimethylsilane was used to form SAMs on the PMSQ at the room temperature. Structural properties of the PMSQ films were investigated using FTIR. The absorption peaks of Si-C (781 cm@super -1@), Si-C (1273 cm@super -1@), and C-H (2975 cm@super -1@) in PMSQ samples disappeared after O@sub 2@ plasma treatment for 5 min. It indicated that the majority of methyl groups in the films were removed and Si dangling bonds were exposed. The Si-O cage-like structures in the PMSQ films also decreased due to its loose structure arrangement. As a result, the low dielectric characteristic of PMSQ would be damaged. On the other hand, the absorption peaks of Si-C and C-H were present for the PMSQ films dipped in diclorodimethylsilane solution with and without ultrasonic system. The purpose of using ultrasonic system was to accelerate formation rate of SAMs on the PMSQ. The results revealed that the hydrophobic dimethylsilane groups have been formed on the surface of PMSQ. The Si-OH bonds on the PMSQ changed to Si-O-Si(CH@sub 3@)@sub 2@. The thickness of SAMs was less than 1.0 nm. The -CH@sub 3@ groups of SAMs on the Si-O network surface of the PMSQ films were apparently of ordered array structure owing to minimal steric hindrance arrangement.

4:00pm **DI-WeA7 Temperature-dependent Current Transport in Low-k Inorganic Polymer Dielectrics**, ***J.W. Tringe,*** *R.A.B. Devine,* U.S. Air Force Research Laboratory

Low-k dielectrics are an increasingly important class of materials for high-performance integrated circuits, promising to significantly increase processing speeds by lowering resistance-capacitance delays in global interconnects. However, since these new dielectrics are anticipated to cover large areas of the chip they also represent a potential reliability risk. It is therefore important to understand how charge transport occurs in the low-k films over a range of temperatures in order to avoid breakdown or excess leakage current during circuit operation. Low-k dielectric films based on inorganic polymers such as FOx flowable oxide from Dow Corning have been examined. Spun-on films, 3000 Å thick, were patterned into metal-insulator-semiconductor capacitor structures, then probed to measure current and capacitance as a function of voltage. Temperature-dependent current-voltage measurements, over the range 26 to 150 °C, show that current conduction is predominately via either Schottky or Frenkel-Poole emission. A field-independent thermally activated barrier height of approximately 0.1-0.2 eV is deduced. The measured exponential term proportional to the square root of the electric field in the current-voltage dependence is smaller than expected for Frenkel-Poole emission, however. Additionally, the temperature and field dependences of the exponential prefactor do not enable us to clearly distinguish between Schottky or Frenkel-Poole emission over the experimental temperature range.

4:20pm **DI-WeA8 Characterization of SiC Films for Cu/low-k Integration**, ***F.G. Celii,*** *T. Tsui, R. Willecke, J. Large,* Texas Instruments, Inc.

Silicon carbide (SiC) is being evaluated for integration into Cu/low-k backend process flows. Potential applications include use as a patterning hardmask and as an etch stop layer with Cu diffusion properties. This paper reports the physical and optical characterization of SiC films. Films were deposited on 200 mm wafers in a commercial reactor using plasma-enhanced chemical vapor deposition (PE-CVD). Film composition and bonding were elucidated using SIMS, XPS and FT-IR spectroscopies. Optical properties of the films were determined from variable-angle spectroscopic ellipsometry into the vacuum ultraviolet region (~140 nm). Under some processing conditions, we observed ellipsometry data consistent with a vertical gradient in the SiC refractive indices. The optical constants of the film, along with reflectance modeling using Prolith, suggest SiC can be used as an anti-reflection coating (ARC) layer for lithographic patterning at either 248 or 193 nm. To test the optical modeling results, we have prepared various film stacks containing SiC and organosilicate glass (OSG) on Si or Cu. The reflectivity vs. wavelength will be measured and compared with the calculated reflectivity values. Initial patterning results will also be presented.

Vacuum Science & Technology
Room 125 - Session VST+MS-FrM

Semiconductor & Functional Coating Systems & Processes

Moderator: J. Noonan, Argonne National Laboratory

8:20am **VST+MS-FrM1 Advances in Semiconductor Physical Vapor Deposition Equipment; Vacuum, System Architecture, and PVD Source Technology**, ***D.J. Harra,*** Novellus Systems, Inc. **INVITED**

Recent advances in physical vapor deposition (PVD) equipment have enabled 0.13-micron and smaller semiconductor device geometries, while also supporting technology transitions from traditional aluminum interconnects to copper, as well as wafer size transitions from 200 mm to 300 mm. Evolutions in PVD system architecture and wafer flow that enable high productivity, as well as incorporation of new technologies such as ionized PVD, and CVD are discussed. In addition, recent developments in sputter source technology will also be discussed. Selected process applications and results are presented to illustrate PVD extendibility to future technology nodes.

9:00am **VST+MS-FrM3 Enhancement of Dielectric CVD Remote Clean Competitiveness Through Improved Gas Utilization**, ***T. Nowak,*** *T. Tanaka, B.H. Kim, M. Seamons, K.B. Jung,* Applied Materials, Inc.

Remote plasma cleaning of dielectric CVD process chambers has been shown to virtually eliminate emission of global warming gases, increase chamber throughput, and increase the lifetime of process chamber hardware. Nitrogen trifluoride (NF@sub 3@) is the principal precursor used in remote plasma cleaning applications because of the ease with which it is dissociated and the high atomic fluorine content achievable at the exit of the remote plasma source. The relatively high cost of NF@sub 3@, however, makes improvement of gas utilization during the remote clean and development of alternative chemistries critical to enhancing the competitiveness of this green manufacturing process. Building on earlier experimental work, we have developed process models and designed experiments to investigate fluorine radical loss mechanisms and utilization efficiencies within parallel plate plasma CVD reactors. Modeling was based on an iterative solution of a one-dimensional flow network with variable gas composition to model transport and recombination losses from the remote plasma source to the process chamber. Calculated values of the atomic fluorine concentration in the process chamber were verified experimentally by measuring etch rates on SiO@sub 2@ wafers. Using the results of the simulation we were able to develop more efficient remote clean processes that, depending on residue to be cleaned, reduce NF@sub 3@ consumption by up to 60% without impacting chamber throughput. In addition, we investigated C@sub 3@F@sub 8@ as an alternative feed gas for the remote clean. Experiments showed that cleaning rates on the order of 80% of NF@sub 3@-based cleans were achievable using C@sub 3@F@sub 8@.

9:20am **VST+MS-FrM4 Vacuum System Architecture for Disk and Flat Panel Production Tools**, *J.L. Hughes,* ***J. Busch,*** Intevac Inc. **INVITED**

Production tools using high vacuum environments are increasingly used by industry, with their requirements growing more difficult. Two such applications are flat panel displays and magnetic hard disks. The flat panel uses up to 1.2 x 1.6 meter rectangular substrates of 1.1 mm thick glass, while hard disks are typically 95 mm circular aluminum. The methods for thin film deposition by sputtering for the two systems varies greatly for the two applications. The same thing is true for substrate transport. But some methods and principals remain the same in either type of production. Vacuum levels run from 1.0E-08 Torr for high vacuum to sputtering pressures of 5.0E-03 Torr. This article looks at two specific examples of vacuum system architecture and draws out the specifics of difference and samenesss between the two.

10:00am **VST+MS-FrM6 Disassembling and Materials Recovering Process of Zinc-Carbon battery by Vacuum Aided Recycling Systems Technology**, ***Y. Saotome,*** Gunma University, Japan*; Y. Nakazawa,* Kokushikan University, Japan*; Y. Yamada,* Nagata Seiki Co., Ltd., Japan

Every material has its own vapor pressure and the principle of VARS Tech. is based on sorting and recovering a specific material from the midst of other combined products through evaporation in a vacuum and the use of different evaporation temperatures for each material.@footnote 1@ In the present paper, VARS Tech. has been applied to the recycling of used batteries. Zinc-Carbon battery R20PU was selected as a specimen and was heated by radiation through vacuum vessel wall made of glass. The resulting relationship between vacuum pressure, reduction in mass and the temperature during heating indicates the occurrence of some evaporation. For the analyses of these complex phenomena, similar experiments were carried out on each component and material of the battery. As a result, at the temperature of about 450K, PVC insulation ring at the top of the battery becomes warped and then water(solution) is evaporated from the inside of battery. From the aspect of recycling process, softening and decomposition phenomenon of PVC insulation ring is correspond to the beginning of disassembling of battery as an assembled product. Actually, disassembling process is accelerated by the evaporation of ZnCl@sub 2@ and can-zinc above about 700K. After the vacuum thermal cycle, the specimen is disassembled and comes to parts such as jacket-metal, some plate metals, an electrode-carbon and positive reactant in powder state. As shown above, the vacuum-aided recycling method is a process that consists of disassembling, sorting, and recovering materials. As shown above, vacuum aided recycling technology has superior characteristics as a restoration systems technology of EcoFactory. As shown above, vacuum aided recycling technology has superior characteristics as a restoration systems technology of EcoFactory. @FootnoteText@ @footnote 1@ Y.Saotome, Y.Nakazawa and Y.Yamada, Vacuum, 53(1999), 101-104.

10:40am **VST+MS-FrM8 The Foundations of Vacuum Coating Technologies**, ***D.M. Mattox,*** Management Plus, Inc.

Vacuum coatings processes use a vacuum environment and an atomic or molecular vapor source to deposit thin films and coatings. The vacuum environment is used not only to reduce gas particle density but also to limit gaseous contamination, establish partial pressures of gases and control gas flow. Electric power is used to thermally vaporize material, thermally decompose vapors, activate reactive species, generate plasmas and accelerate ions. This paper will trace the development of vacuum technology from the piston water pumps of the Roman Empire, the development of electric power from frictional electricity machines and the electrolytic cell, and the development of deposition techniques based on thermal evaporation, sputtering, arc vaporization, laser ablation and chemical vapor precursors. Both patent and technical literature will be cited as to the first reports on phenomena and processes and the beginnings of sustained applications of various vacuum-coating processes. Several areas of uncertainty will be described and discussed. Often these uncertainties are due to problems with terminology or to the differing nature of patent and technical literature. Several areas where original ("pioneering") work is commonly attributed to an inappropriate individual(s) will be discussed.

11:00am **VST+MS-FrM9 Downstream Effluent Management Subsystems for Semiconductor Manufacturing Processes**, ***Y. Gu,*** MKS Instruments, Inc. **INVITED**

Smaller geometry and larger wafer size are the major trends for today's semiconductor device manufacturing industry in order to attain higher throughput and better device performance. At the same time, tool uptime and process yield become more important as they are closely related to the fab throughput. Significant efforts have been spent on improving the process throughput by employing advanced tools, new process chemistries and more efficient in-situ cleaning steps. However, it was found that the tool usage is often reduced because of existing downstream problems. In addition, particle levels on wafer surface are also related to the cleanness of the pump line. These problems are even getting worse because of the use of more reactive precursors, which are intended to reduce the process temperature and increase the deposition rate. The most common processes which are experiencing significant downstream problems are silicon nitride LPCVD, TEOS LPCVD, Aluminum etch, tungsten CVD process, silicon Epi, and variety of other processes. These problems can be caused by physical sublimation of the condensable by-products, or the complex chemical reactions between unreacted precursors, by-products, and/or the vapor backstreaming from the scrubber. Different techniques are required to manage these effluent problems because of their different mechanism. In addition, a systematic solution is often required in order to prevent creating a problem. Several downstream effluent management subsystems developed at MKS Instruments Inc. will be discussed in this talk. They have been proven very effective to improve semiconductor manufacturing process uptime and yield.

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