Dielectrics
Room 130 - Session DI-MoA
High K Dielectrics I

Moderator: M.A. Leskela, University of Helsinki, Finland

2:00pm **DI-MoA1 Epitaxial High-K Gate Oxides on Silicon: Impact on Future CMOS***, **Z. Yu**, R. Droopad, J. Ramdani, J. Curless, C. Overgaard, J. Finder, K. Eisenbeiser, J. Wang, W. Ooms,* Motorola Labs*; Y. Liang, S.A. Chambers,* Pacific Northwest National Laboratory **INVITED**

One of the main problems facing the semiconductor industry is the scaling of the gate dielectric of silicon CMOS devices. Currently, SiO@sub 2@ gate oxide is being used, but it suffers from tunneling leakage current and reliability problems at thickness below 2 nm. Alternative high-k materials to replace SiO@sub 2@ need to be developed as soon as possible. Single crystal oxides such as SrTiO@sub 3@ (STO) with a simple structure and a much higher k are ideal candidates for future CMOS gate dielectrics. A physically thick high-k layer can behave electrically like a thin one, thereby eliminating the tunneling leakage problems experienced with <2 nm SiO@sub 2@. These oxides also exhibit ferroelectric behavior and their use as the gate dielectric on Si can be exploited in the realization of a single transistor memory element. In this presentation, we will review the atomic simulation, MBE growth, structural, electrical and interface properties of high quality single crystal STO layers on Si with low leakage current density and effective oxide thickness (EOT) < 1 nm. The STO layers are characterized using RHEED, SE, XRD, AFM, TEM and XPS. Atomic simulations have been extensively carried out to predict the reliability of the structure of the epi-oxide/Si interface. The oxide films on Si(001) are (001) orientated as determined by XRD and pole figure analysis confirms that the perovskite oxide lattice is rotated 45° with respect to the Si lattice. AFM measurements shows rms roughness as low as 1.2 Å. Cross-sectional TEM shows smooth interfaces and dislocation free STO films. XPS has been used to determine the band offsets at the oxide/Si interface. Electrical measurements on MOS capacitors fabricated on wafer using platinum gate electrodes demonstrated leakage as low as 10@super -8@ A/cm@super 2@ with interface state densities in the low 10@super -11@ cm@super -2@eV@super -1@. Results on MOSFET devices fabricated using STO as the gate insulator will be presented.

2:40pm **DI-MoA3 High Dielectric Constant Material as an Alternative Gate Dielectric in MOSCAP and MOSFET Applications***, **Y.S. Lin**, J.P. Chang,* University of California, Los Angeles

ZrO@sub 2@ is investigated in this study to replace SiO@sub 2@ as the gate dielectric material in metal-oxide-semiconductor devices. ZrO@sub 2@ films were deposited on P-type Si (100) wafers by a rapid thermal chemical vapor deposition process using Zr(OC@sub 4@H@sub 9@)@sub 4@ as the precursor and oxygen as the oxidant. The two chemistries were introduced sequentially into the reactor with purging and evacuation in between. The deposited films were stoichiometric, uniform and extremely smooth based on X-ray photoemission, ellipsometry, and atomic force microscopy measurements. The high-resolution transmission electron micrograph showed a polycrystalline ZrO@sub 2@ film (monoclinic) and an interfacial amorphous ZrSi@sub x@O@sub y@ layer on the silicon substrate. This interfacial layer is confirmed to be zirconium silicate based on the thermodynamic calculation, chemical etching resistance, and medium energy ion scattering analysis. Excellent step coverage was observed by depositing ZrO@sub 2@ over 300 nm features with an aspect ratio of 4. The conformal deposition profile can be simulated by the Monte Carlo method with a sticking coefficient on the order of 10@super -4@. In-situ transmission infrared analysis is used to examine the chemically absorbed surface species during the deposition process with various chemical exposures. Isotope labeling of oxygen is underway to assess the effect of the oxidation/annealing processes on film composition and electrical performance. The dielectric constant of RT-CVD ZrO@sub 2@ was 15-18, and the capacitance-voltage measurement showed a hysteresis around 100 mV, which was slightly higher than desired <45 mV value. The interface state density was ~ 1.2x10@super 11@ cm@super -2@eV@super -1@, as determined by capacitance measure at various frequencies. NMOS transistors are made with n@super +@ polysilicon gate, and good turn-on characteristic and low leakage current density of 2x10@super -7@ A/cm@super 2@ at - 1.5V were observed.

3:00pm **DI-MoA4 High Frequency Characterization of Thin Films with High Dielectric Constant***, **J. Westlinder**, K. Larsson, H.-O. Blom, J. Olsson,* Uppsala University, Sweden

New dielectric materials are required in future IC's. Not only a new gate oxide with higher dielectric constant is needed, but also high dielectric materials must be used in on-chip integrated capacitors in order to increase the integration density. We have investigated the high frequency behavior of (Metal-Insulator-Metal) MIM-capacitors in the frequency range from 1 MHz to 10 GHz. The insulator thin films (about 100 Å to 2000 Å) have been made of high dielectric constant materials, e.g. Ta@sub 2@O@sub 5@, ZrO@sub 2@, or HfO@sub 2@. In the tantalum oxide case, there seems to be a dependence in dielectric constant with frequency. At higher frequencies (over about 1 GHz) there is a rapid decrease in the dielectric constant due to relaxation effects. A first order equivalent circuit model has been developed and simulated, showing good agreement with the measurements. Also, the results show a decrease in dielectric constant with decreasing thickness of the films. These preliminary results indicate that the performance of RF-devices and RF-circuits might be seriously degraded in the GHz region. In addition, the DC I-V characteristics were measured in terms of leakage current density and breakdown voltage, and will be presented.

3:40pm **DI-MoA6 Interfacial Stability of High-k Dielectrics Deposited by Atomic Layer Chemical Vapor Deposition***, **W. Tsai**,* IMEC (Intel assignee), Belgium*; H. Nohira, R. Carter, M. Caymax, T. Conard, S. De Gendt, M.M. Heyns, J. Petry, O. Richard, W. Vandervorst, E. Young, C. Zhao,* IMEC, Belgium*; J. Maes,* ASM Europe, The Netherlands*; M. Tuominen,* ASM Europe, The Netherlands, Belgium

Control of interfacial oxide growth is critical to achieving sub 1 nm Equivalent Oxide Thickness in high k gate stacks for future generations microelectronic devices. The formation of interfacial oxide is dependent on Si surface preparations, high k dielectrics deposition, post deposition conditioning such as thermal anneal and air exposure. In this work, effect of various interfaces on initial growth of high k layers, interface stability and electrical peformance were investigated. High-k dielectrics layers are grown by Atomic Layer Chemical Vapor Deposition (ALCVD), dielectrics and interfacial layer thickness /composition were characterized by X-ray Fluorescence, X-ray Photoelectron Spectroscopy (XPS) and Transmission Electron Microscopy (TEM). An initial high k dielectrics layer formation with inhibited growth was observed for both ALCVD Al2O3 and ZrO2 films, followed by a linear growth regime with a full coverage layer. For high k dielectrics deposited on Si substrates with hydrogen termination from HF dip, growth of interfacial oxide SiOx was quantified as a function of air exposure. Interfacial oxide forms due to oxygen permeation through the high k layers, either during air exposure; during thermal anneal in an oxygen ambient (>500oC) or during the ALCVD growth itself whereby the growth process itself acts as an oxygen source. The latter is observed in the case of ZrO2 where the interfacial oxide scales with ZrO2 layer thickness. In addition, an intrinsic interfacial oxide growth is observed with XPS from as-deposited high k dielectrics films. For Al2O3, an interfacial oxide of approx. 1.5 Ã… for thickness > 2 nm, reflecting the possible formation of Al-O-Si bond. Minimization of interfacial oxide growth in high k gate stacks was demonstrated with an in-situ poly-silicon cap on Al2O3 to restrict the oxygen diffusion. The stability of such capped high k/ Si interface was also shown to be intact after 1000oC RTP anneal in nitrogen.

4:00pm **DI-MoA7 First Step Towards Crystalline Titanate-Si Integration: Formation of Atomic Layer Strontium Silicate on Si(001)***, **S. Gan**, Y. Liang, S. Shutthanandan, S. Thevuthasan,* Pacific Northwest National Laboratory

Recent work showed that crystalline titanates grown on Si(001) exhibited promising properties as the potential high-K gate oxides for CMOS. One of the critical issues in this approach is the interfacial template layer that needs to possess favorable struc tural and chemical properties for growth of crystalline oxides on Si. We present our recent results on the study of the initial stage of oxide growth on Si(001). Using scanning tunneling microscopy (STM), x-ray photoelectron spectroscopy (XPS), low-energy electron diffraction (LEED), and Rutherford back scattering (RBS), we investigated the structural and chemical behaviors of six strontium based templates grown on Si. It was found that depending on the surface strontium coverage, the strontium-covered Si surfaces exhibit a series of reconstructions. These reconstructions not only had different atomic structures but also different stability against oxidation and the oxide growth. For instance, upon exposure to oxygen, the (3x2) reconstruction was converte d to a disordered (1x1) surface while the Sr/Si-(1x2) reconstruction remained intact. For the growth of oxides, the (1x2) structure was found to provide the most stable interface, as evidenced by a uniform layer in angular dependence XPS results, the lack of interfacial SiO@sub2@ layer, and the ability to form single-crystal SrO films on this structure. By combining results obtained from STM, XPS, RBS, and LEED, we correlated the interface structures with film properties, which allowed us to identify suitable interfacial templates for optimized growth of titanates. @FootnoteText@ Pacific Northwest Laboratory is a multiprogram national laboratory operated for the U.S. Department of energy by Battelle Memorial Institute under Contract DE-AC06-76RLO 1830.a.

4:20pm **DI-MoA8 High-k Metal Oxide Dielectrics Deposited by CVD using Oxygen and Ozone**, ***M. Yoon***, *V.K. Medvedev, K.D. Hauch,* University of Washington; *J.W. Rogers, Jr.,* Pacific Northwest National Laboratory; *Y. Ono, S.T. Hsu,* Sharp Laboratories of America

TiO@sub 2@ thin films have generated considerable interest in high-k gate oxide applications. Previously we have described a novel process for creating high purity, carbon-free TiO@sub 2@ films on Si utilizing a TiO@sub x@ buffer layer.@footnote 1@ Here, improvements in oxidizing this buffering Ti layer using ozone (O@sub 3@) are presented. Auger electron spectroscopy (AES) analysis show similar stoichiometry of Ti and O when using either oxygen or ozone at room temperature. Low energy electron diffraction (LEED) analysis was conducted on Si, Ti/Si, and O@sub 2@ oxidized Ti/Si. Preliminary results show: an initial Si substrate with a highly ordered 2x1 structure prior to the deposition of Ti, a crystalline Ti film deposited on the Si, and the amorphorization of the Ti after oxidation with O@sub 2@. It is our aim to produce an amorphous TiO@sub 2@ film on the TiO@sub x@ buffer layer and thus the amorphous structure of this buffer layer is desired. Oxygen deficiency in TiO@sub 2@ gate oxide films is a major cause of increased leakage current. O@sub 3@ is an attractive alternative to O@sub 2@ as an oxidizer since it produces atomic oxygen (O) upon decomposition which can react with single dangling bond sites on the film surface, and thus create a denser, oxygen rich film. The co-deposition of the titanium isopropoxide (TTIP) precursor with O@sub 3@ for creating a CVD-TiO@sub 2@ film on the buffer layer has been compared to the co-deposition of TTIP with O@sub 2@. AES and electron spectroscopy for chemical analysis (ESCA) measurements show few compositional differences between the two TiO@sub 2@ films, however, atomic force microscopy reveals distinctly different morphology. The application of TiO@sub 2@ and other similarly produced metal oxide films (e.g. HfO@sub 2@) as gate oxides in MOS devices is also being explored. @FootnoteText@ @footnote 1@A. Tuan, M. Yoon, V. Medvedev, Y. Ono, Y. Ma, and J. W. Rogers, Jr., Thin Solid Films, 377-378 (2000) 766-771.

Dielectrics
Room 134/135 - Session DI1-MoP
High K Dielectrics Poster Session

DI1-MoP1 Generation and Relaxation of Positive Charge in Gate Dielectric of MOS Structures at High-fields*, G.G. Bondarenko,* Moscow Institute of Electronics and Mathematics, Russia*; V.V. Andreev, A.A. Stolyarov,* Bauman Moscow State Technical University, Russia

In this work the new technique of investigation of generation and relaxation processes in gate dielectric of MOS structures during and after high-field stress is proposed. The technique is based on the controlling of current stress, applied to the sample, and simultaneous voltage measurement on it. The technique proposed allows carrying out the controlled electron injection into gate dielectric at high-fields, realizing the simultaneous monitoring of MOS structures charge state change both under the present field and under lower fields, that gives possibility to obtain new quality information about charge generation processes in dielectric layers. The technique allows, right after high-field injection without sample re-switching, to monitor the relaxation processes of charges generated by injected electrons in gate dielectric of MOS structures in wide range of electric fields, from the injection field to the structure short circuit. Using the technique proposed the investigation of positive charge generation and relaxation phenomena in silicon MOS structures with thermal SiO@sub 2@ film had been carried out. It was shown that under high injection current densities, the positive charge value monitoring by voltage shift on MOS structure can lead to significant error, to decrease which it is necessary to measure the positive charge value using voltage shift under less current densities. It was found out that the relaxation time of positive charge, generated by tunnel Fowler-Nordheim electron injection from silicon in thermal SiO@sub 2@ film, has field dependence, decreasing with external electric field rise.

DI1-MoP2 Stability of Chemical Vapor Deposited Thin Films HFO@sub 2@ and HFSi@sub x@O@sub y@*, H. Bhandari,* *V. Rangarajan, T.M. Klein,* University of Alabama

Two desirable properties for candidate high dielectric constant materials for MOSFET gates are that the material remains amorphous and does not react with silicon substrate during post deposition anneals. Uncontrolled multiple oxide layer growth during post deposition anneals can result in a decrease in the overall capacitance while a polycrystalline or phase-separated material could have excessive current leakage along grain boundaries. Hafnium oxide and hafnium silicate are two materials, which are predicted to be thermodynamically stable with silicon at 1000°C. We have deposited these materials using organometallic chemical vapor deposition with Hf (IV) t-butoxide and various oxygen atom sources including N@sub 2@O and O@sub 2@, as well as remote N@sub 2@O and O@sub 2@ plasmas. Rapid thermal annealing experiments were performed in Ar, O@sub 2@ and N@sub 2@ ambients up to 1000°C. Thin film stability was examined using XPS, Fourier transfer infrared spectroscopy and X-ray diffraction measurements.

DI1-MoP3 A Study of MOS Characteristics of Reoxidized HfO@sub 2@ Thin Film for Gate Oxide Applications*, H.-J. Choi,* *D.W. Lee, J.-H. Yoo, S.-W. Nam, D.-H. Ko,* Yonsei University, Korea*; J.-H. Ku,* R&D Center Semiconductor Samsung Electronics Co.*; M.-H. Cho,* Yonsei University, Korea*; S. Choi,* R&D Center Semiconductor Samsung Electronics Co.*; C.-W. Yang,* Sungkyunkwan University, Korea

We investigated the change of the microstructure which depend on the thickness of Hf films deposited by DC magnetron sputtering on Si substrate for gate dielectric application. Also, we estimated the electrical property and the microstructure of the interlayer between the thin HfO@sub 2@ films and Pt and Al gate electrode. The Hf films reoxidized by the RTP(rapid thermal processing) were analyzed by spectroscopic ellipsometry, AFM, XRD, XPS, and HR-TEM. We observed small grains of the HfO@sub 2@ film due to the local crystallization of the as-deposited Hf film ~90Å by HR-TEM. The thickness of the interfacial layer between hafnium oxide and Si substrate was about 8Å. After RTP treatment at 800°C in N@sub 2@ ambient, the thickness of interfacial layer was equal to that of as-deposited film. For 500Å thick as-deposited Hf film, the HfO@sub 2@ layer at the surface was observed about 55Å by HR-TEM. The HfO@sub 2@ layer increased to be 90Å at 800°C in N@sub 2@ ambient. Especially, the HfO@sub 2@ grains were shown not only at the surface of the Hf film but also at the silicide(Hf@sub 5@Si@sub 4@) grain boundaries. And the buckling of the silicide film on the Si substrate was locally observed due to the stress generated during the silicide and hafnium dioxide formation. XRD peaks indicated the formation of silicide after RTP treatment over 700°C. We evaluated C-V and I-V of the MOSCAP structures in the Pt/Hf(~100Å)/Si and Al/Hf(~100Å)/Si , and it demonstrated that the capacitance and the leakage current level of the MOS structures were changed upon the temperature of RTP treatments.

DI1-MoP4 Investigation of Tungsten Silicide Gate for the Integration with High-k Hafnium Oxide (HfO@sub 2@) in Metal-Oxide-Semiconductor Devices*, K. Roh,* *S. Yang, H. Kang, Y. Roh, G. Bae, D. Jung, N.-E. Lee, C.-W. Yang,* Sungkyunkwan University, Korea

Sub-0.1 µm MOSFETs face a scaling limit when a SiO@sub 2@ gate dielectric is used due to high direct tunneling leakage current. Recently, many high-k gate dielectrics such as Al@sub 2@O@sub 3@, Y@sub 2@O@sub 3@, ZrO@sub 2@, HfO@sub 2@ and their stacks have been studied extensively to replace thermal SiO@sub 2@. Among those dielectrics, Hafnium oxide and their silicates have been suggested as a strong candidate for the alternate gate oxides. In this work, we report the structural and electrical properties of HfO@sub 2@ films with tungsten silicide (WSi@sub 2@) as a metal gate. The samples were fabricated on 4-in n- and p-type (100) wafers with 4~7 @ohm@cm resistivity. Hf films were deposited using rf reactive magnetron sputtering method from 99.5 % Hf target on the Si wafers, and were thermally oxidized in furnace at 500 °C. Annealing of the formed HfO@sub 2@ in furnace at 500 °C was then followed. During sputtering, the gas pressure and rf power were 10 mTorr and 50 W, respectively. Tungsten silicide films for gate electrode were deposited directly on the HfO@sub 2@ films in a cold-wall low pressure chemical vapor deposition system with the thickness of 500 ~ 1500 Å. For electrical characterization, the WSi@sub 2@/HfO@sub 2@/Si MOS capacitors were. Additional annealing was carried out at various conditions to minimize the resistance of WSi@sub 2@ and etching damage. The hysteresis of the WSi@sub 2@/HfO@sub 2@/Si MOS capacitors before and after annealing was negligible (<10 mV); it was independent on frequencies from 10 kHz to 1 MHz and on bias ramp rates from 10 mV to 1 V. Gate depletion effect was not also observed. After furnace annealing of the WSi@sub 2@/HfO@sub 2@/Si MOS capacitors at 500 °C, EOT (equivalent oxide thickness) was reduced from 26 to 22 Å. In addition, the leakage current was 1x10@super -5@ A at 1 V after annealing, which is reduced by approximately one order as compared to that measured before annealing.

DI1-MoP5 Annealing Effects on Optical Properties of Hafnium Oxide Films Observed by Spectroscopic Ellipsometry*, Y.J. Cho,* *N.V. Nguyen, C.A. Richter, J.R. Ehrstein,* National Institute of Standards and Technology

We have applied spectroscopic ellipsometry (SE) to investigate a set of HfO@sub 2@ films and correlate their optical properties with fabrication processes, in particular, with high temperature annealing. Among the many proposed high-k dielectrics such as HfO@sub 2@, Ta@sub 2@O@sub 5@, TiO@sub 2@, and ZrO@sub 2@, the use of HfO@sub 2@ films as the replacement for SiO@sub 2@ as the gate dielectric in CMOS devices has received much attention recently due to its high dielectric constant, low leakage current, good thermal stability, and interface characteristics comparable to silicon dioxide/silicon interface. In spite of these promising properties, little is known about the optical properties of HfO@sub 2@. Thin HfO@sub 2@ films were grown on Si substrate by dc magnetron sputtering and then annealed at high temperatures. SE measurements were performed on a high-accuracy custom-made spectroscopic ellipsometer. The dielectric functions of these films were determined by inversions of SE data and compared with the results with those obtained by using a Tauc-Lorentz (TL) dispersion function. It will be shown that, in the near-IR-visible-UV spectral range, TL can be used to effectively describe the optical properties of HfO@sub 2@. From the characteristics found in the pseudo-dielectric functions or the TL dispersions, when the annealing temperatures increase from 500 to 700 °C, we observed that, for the HfO@sub 2@ films, the optical band gap increases. In addition, for samples annealed at 600 °C and above, new optical features, which are not present at lower temperature, are clearly seen in their dielectric functions. These features are the signature of poly-crystallization in the film attributable to the annealing. As a result, we conclude that SE can easily and quickly identify the onset or the existence of crystalline HfO@sub 2@ films without employing a more elaborate and destructive method such as a transmission-electron microscope (TEM).

DI1-MoP6 Physical and Electrical Characteristics of W-TiN/HfO@sub 2@/Si (MOS) Devices*, **S. Yang**, K. Roh, H. Kang, Y. Roh, K. Kim, N.-E. Lee,* Sungkyunkwan University, Korea

Recently, the metal/high-k oxide structures have been investigated extensively to implement sub-100 nm MOSFETs technology. In this work, we present the physical and electrical characteristics of MOS capacitors with HfO@sub 2@ gate dielectric and W/TiN gate electrode. The Hf thin films were deposited directly on n-type silicon substrate by a RF magnetron sputtering method. The HfO@sub 2@ films with thicknesses of 6-7 nm were formed by a thermal oxidation of Hf thin film in O@sub 2@ ambient at 500 °C for 120 min in furnace. The annealing of the HfO@sub 2@ films was then carried out in N@sub 2@ ambient at 500 °C for 60 min in furnace. TiN films (30 nm) were deposited on HfO@sub 2@ by a DC reactive sputtering method followed by W deposition (200 nm) using LPCVD. For some samples, only the W films were deposited on HfO@sub 2@ films to investigate the roles of the TiN films. The sheet resistance of W/TiN was ~ 4 @ohm@/square. The intermediate layer between gate dielectric and Si was observed by TEM, which is believed to be a hafnium silicate (HfSi@sub x@O@sub y@) layer. To evaluate the EOT and leakage current characteristics, the C-V and I-V measurements of MOS capacitors with different gate electrode (i.e., W/TiN, W and Pt gate) were performed. The hysteresis of W/TiN gate was negligible (100 mV) due to gate dielectric damage during sputtering deposition. The EOT of W/TiN/HfO@sub 2@ MOS capacitors was 1.9 nm based on the C-V measurement. In addition, as compared to the results obtained from the W/HfO@sub 2@/Si MOS structures, the W/TiN/HfO@sub 2@/Si MOS capacitors showed an excellent current-voltage characteristics: The leakage current was ~2x10@super -5@ A/cm@super 2@ at 2 V which is lower than published results reported by other researchers at the same EOT.

DI1-MoP7 Characteristics of HfO@sub 2@/HfSi@sub x@O@sub y@ Film as an Alternative Gate Dielectric in Metal-Oxide-Semiconductor Devices*, **H. Kang**, Y. Roh, G. Bae, D. Jung, C.-W. Yang,* Sungkyunkwan University, Korea

Recently, research efforts on high-k gate oxides have been focused on materials such as HfO@sub 2@, ZrO@sub 2@, and their silicates due to their excellent electrical properties. In particular, the HfO@sub 2@/HfSi@sub x@O@sub y@ gate-oxide produces the excellent interfacial properties between HfSi@sub x@O@sub y@ and Si, while the effective dielectric constant can be further increased by forming the HfO@sub 2@ layer on HfSi@sub x@O@sub y@. In this work, we investigated the physical and electrical properties of the HfO@sub 2@/HfSi@sub x@O@sub y@ prepared by a simple method; that is, the oxidation of sputtered Hf metal films on Si followed by N@sub 2@ annealing. Thin Hf layers were directly deposited on Si substrate by sputtering. The oxidation and annealing were performed at 500 °C for 120 min and in N@sub 2@ ambient at 500 °C for 60 min in furnace, respectively. Al gate was thermally evaporated on the HfO@sub 2@ film using a shadow mask. Using the TEM, AES, and XPS techniques, we confirmed that the oxidation of the thin Hf films on Si results in a HfO@sub 2@/HfSi@sub x@O@sub y@ stack layer. In addition, the thickness of an amorphous HfSi@sub x@O@sub y@ layer (HfO@sub 2@ layer) reduces (increases) after the post-oxidation annealing in N@sub 2@ ambient, which causes the increase of the effective dielectric constant. The hysteresis window and the interface state density of HfO@sub 2@/HfSi@sub x@O@sub y@ were less than 10 mV and ~3x10@super 11@ /cm@super 2@ eV without PMA, respectively. The leakage current was also low (1x10@super â€“5@ A/cm@super 2@ at 2 V). It is believed that these excellent results were obtained due to existence of the amorphous HfSi@sub x@O@sub y@ buffer layer. We also found that the degradation of HfO@sub 2@/HfSi@sub x@O@sub y@ gate oxides is more severe when electrons were injected from the gate electrode.

DI1-MoP8 Interface Formation and Electrical Properties of TiN@sub x@ (Titanium Nitride)/HfO@sub 2@/Si Structure for Application in Gate Electrode*, **Y.S. Ahn**, K.J. Kim, S.H. Ban, N.-E. Lee, S. Yang, K. Roh, Y.H. Roh,* Sungkyunkwan University, Korea

Recent extensive research activities on HfO@sub2@ as a high-k gate dielectric material are focused on the layer formation and interfacial properties between HfO@sub2@ and Si substrate. For the integration of HfO@sub2@ in MOS structures, metals as gate electrode materials are expected to be required. One of candidates for metal gate electrode is CVD tungsten. For application of CVD-W as a gate electrode, a diffusion barrier such as TiN@subx@ are often necessary to avoid the chemical etching of gate dielectrics by F atoms in the CVD precursor gas, WF@sub6@, resulting in increased leakage current. In this work, interface formation and electrical properties between TiN@subx@ and HfO@sub2@ for application of gate electrode were investigated as a function of annealing temperature. Hf layers were deposited on n-type Si(001) using rf magnetron sputter deposition. HfO@sub2@ layers of 6-7 nm thickness were formed at 500 °C by a thermal oxidation of the Hf layers for 120 min in furnace with O@sub2@ ambient. Further thermal annealing at 500 °C in N@sub2@ ambient for 60 min was carried out in order to reduce the fraction of silicate glasses formed. Then, TiN@subx@ layers of 100 nm were deposited at room-temperature by reactive d.c magnetron sputtering using Ar and N@sub2@ mixed in flow ratios of 6:1 and 6:3 at the working pressure of 4x10@super-3@ Torr and at the source power of 100 W. Phase identification of TiN@subx@ layers before and after thermal annealing of TiN@subx@/HfO@sub2@/Si at 650, 750, and 850°C in furnace, respectively, was carried out by XRD. Depth profiling analysis of Ti, Si, Hf, N, and O element for TiN@subx@/HfO@sub2@/Si structure was performed by Auger electron spectroscopy (AES). Sheet resistances of TiN@subx@/HfO@sub2@/Si systems were measured by a four-point probe. The interfacial reaction of TiN@subx@/HfO@sub2@ will be discussed by measuring the chemical binding states at the interface using XPS.

DI1-MoP9 Deposition and Characterization of Thin ZrO@sub2@ Films*, **L. Koltunski**, R.A.B. Devine, R. Marquardt,* University of New Mexico

Amorphous films of ZrO@sub2@ up to ~ 100 nm thick have been deposited on Si substrates at room temperature using O@sub2@ and Zr(C@sub4@H@sub9@O)@sub4@ source gases in an electron cyclotron resonance excited plasma enhanced chemical vapor deposition reactor working in the pressure range ~ 2 millitorr. The film composition was measured by X-ray emission and found to be stoichiometric (ZrO@sub2@) within experimental error. The refractive index at 632.8 nm was ~ 1.74 - 1.84 whilst the dielectric constant, measured on metal-oxide-semiconductor capacitor structures, was ~ 20. Glancing incidence X-ray scattering was used to ascertain the film density which was ~ 5 g cm@super-3@ as compared to a monoclinic, crystalline value ~ 5.83 g cm@super-3@. Infrared absorption spectroscopy of the amorphous films evidenced a strong transverse optic mode at 410 cm@super-1@ and an associated longitudinal optic mode at 693 cm@super-1@. From the transverse/longitudinal optic mode splitting we determine that the dielectric constant is > 11. Since the experimental value is ~ 20 other transverse/longitudinal modes must be present but not observed in the spectral range we have examined (350 - 1600 cm@super-1@). Evidence for crystalline phases (monoclinic and tetragonal) was found in the infrared spectra of samples deposited using radio frequency substrate bias. The presence of crystalline inclusions was confirmed by X-ray scattering analysis. The amorphous film dielectric constant is only ~ 9% smaller than the crystalline value (~22) whereas the refractive index is smaller by 16-21 %. The origin of these differences will be discussed.

DI1-MoP10 Material and Electrical Characteristics of ZrO@sub 2@ Film Obtained by Electron Cyclotron Resonance Plasma Enhanced Chemical Vapor Deposition (ECR-PECVD)*, B.O. Cho, **J. Wang**, S.X. Lao, J.P. Chang,* University of California, Los Angeles

ZrO@sub 2@ is investigated in this work to replace SiO@sub 2@ as the dielectric material in metal-oxide-metal (MOM) capacitors in dynamic random memory (DRAM) devices for its high dielectric constant, good thermal stability, excellent conformality, and large bandgap. ZrO@sub 2@ films were deposited on p-Si (100) wafers by ECR-PECVD method using zirconium tetra-tert-butoxide (Zr(OC@sub 4@H@sub 9@)@sub 4@) as an organometallic precursor, Ar as a carrier of the precursor vapor, and O@sub 2@ as an oxidant. X-ray photoelectron spectroscopy and secondary ion mass spectrometry indicated that stoichiometric ZrO@sub 2@ film was obtained with various amount of carbon incorporation depending upon the electron temperature and the O@sub 2@/Ar flow rate ratio. X-ray diffraction showed that the films deposited without substrate heating were amorphous. By manipulating the negative substrate bias and raised the deposition temperature to around 400 °C, carbon-free amorphous ZrO@sub 2@ was obtained. High resolution transmission electron microscopy was used to observe the interfacial thin film formation between the deposited ZrO@sub 2@ and the substrate Si. The electrical property of the as deposited ZrO@sub 2@ was assessed by forming Al/ZrO@sub 2@/Si capacitor structures. Good capacitance-voltage and current-voltage characteristics were obtained with k=22 at 1 MHz and J=4x10@super -5@ A/cm@super 2@ at -1.5 V, respectively. The C-V response showed a small hysteresis of <60 mV and an interfacial state density of 2x10@super 11@ cm@super -2@ eV@super -1@ based on capacitance measurement at various frequencies. The influences of carbon incorporation, substrate heating and biasing, and post-annealing on the bulk and the interfacial trap formation were investigated by photoconductivity measurement, which enables the determination of leakage conduction mechanism.

**DI1-MoP11 Characteristics of Zirconium Oxide with Different Gate Electrodes*, S.-W. Nam,* *J.-H. Yoo, D.W. Lee, D.-H. Ko,* Yonsei University, Korea*; J.-H. Ku,* Samsung Electronics Co., Korea*; M.-H. Cho,* Yonsei University, Korea*; S. Choi,* Samsung Electronics Co., Korea*; C.-W. Yang,* Sungkyunkwan University, Korea

MOS devices are being continuously scaled, especially the gate oxide thickness and the source/drain junction depth. Key process issues in conventional SiO@sub 2@ scaling are with the gate stack, including boron penetration and gate leakage for very thin gate oxides and depletion effects in the polysilicon electrodes. The solution is to use a gate dielectric with a higher dielectric constant than that of SiO@sub 2@. Together with a high-K dielectric, dual metal gate may be implemented to enable the scaling of MOS devices. We investigated the electrical properties and thermal stability on sputtered ZrO@sub 2@ films with various electrodes for p-type silicon substrate. ZrO@sub 2@ thin films as a gate dielectric were deposited by reactive dc magnetron sputtering, followed by thermal annealing in either O@sub 2@ or N@sub 2@ using furnace. And then various metals such as Al, Pt, TiN, TiN/Al, and TiN/Pt were deposited by sputtering as a gate electrode. Also, conventional poly-Si and poly-SiGe as a gate electrode were deposited by chemical vapor deposition. By HRTEM and XPS analyses, we evaluated compatibility and thermal stability between the ZrO@sub 2@ films and electrodes. We focused on the interfacial layer between high-k dielectric and electrodes. In comparison with Pt electrode, the accumulation capacitance of the MOS with Al electrode demonstrated about 8% degradation. And we compared electrical characteristics of Al (or TiN/Al) and Pt (or TiN/Pt) with other well-known gate electrodes such as poly-Si and poly-SiGe.

DI1-MoP12 Diffusion Studies of High k Gate Dielectric Candidates Hafnium and Zirconium Silicates into Si*, M.A. Quevedo-Lopez,* *M. El-Bouanani, S. Addepalli, C. Huang, J.L. Duggan, B.E. Gnade, R.M. Wallace,* University of North Texas*; L Colombo, M. Bevan, M. Douglas, M. Visokay,* Texas Instruments Inc.

The area of advanced gate dielectrics has gained considerable attention recently because the SIA technology roadmap predicts the need for a <2.0 nm SiO@sub 2@ gate dielectric for sub-0.13 mm scaled silicon CMOS.@footnote 1@ Desirable properties for new gate dielectrics include; higher permittivity (@kappa@) than SiO@sub 2@ (@kappa@ = 3.9), minimal reaction barrier, thermodynamic stability in direct contact with silicon, low leakage current (<1 A/cm@super 2@ at 1V), and very low diffusion into silicon. Considering these requirements, Hf silicate and Zr silicate have been proposed as suitable candidates for advanced gate dielectric applications.@footnote 2,3@ However, more issues have to be resolved. Among those issues metal diffusion (Zr, Hf) into the channel is critical because impurity diffusion from the gate dielectric into the channel region would likely result in deleterious effects on carrier mobility. We have studied the diffusion of Hf and Zr from high-@kappa@ gate dielectric candidates HfSixOy and ZrSixOy. The studies were carried out after aggressive thermal annealing followed by chemical etching. The annealed/etched films were studied using monochromatic X-ray Photoelectron Spectroscopy (XPS), Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS), High resolution TEM, and Rutherford Backscattering Spectrometry (RBS). Film deposition, chemical etching and characterization issues are discussed. No detectible Hf diffusion into Si from RTP and furnace-annealed films is observed. In contrast Zr diffusion is observed upon RTP and furnace anneals. Implications for high-k gate dielectric applications are also discussed. This work was supported by the Texas Advanced Technology Program, the Semiconductor Research Corporation, and DARPA. @FootnoteText@@footnote 1@Semiconductor Industry Association roadmap 1999 @footnote 2@G.D. Wilk and R.M. Wallace, Appl. Phys. Lett. 74, 2854 (1999). @footnote 3@G.D. Wilk and R.M. Wallace, Appl. Phys. Lett. 76, 112 2000). @footnote 4@W.-J. Qi, et al., Appl. Phys. Lett. 77, 1704 (2000).

DI1-MoP13 High-dielectric Constant Aluminum Oxide Films*, C. Falcony,* CINVESTAV and ESFM-IPN, Mexico*; M. Aguilar-Frutis,* CICATA-IPN, Mexico*; J. Guzman,* CICATA-IPN, IIM-UNAM, Mexico*; M. Garcia,* IIM-UNAM, Mexico

Aluminum oxide films deposited by Spray Pyrolysis at low temperatures (450 to 650°C) have been studied as high-K dielectric layers on silicon. Dielectric constants in the range of 6.7 to 8.5 and interface states in the order of 10@super 11@ at midgap have been obtained. Overall optical, electrical, and structural characteristics are strongly dependent on the deposition parameters, as well as the presence of carbon as impurity. Dielectric breakdown for these films is larger than 5 MV/cm.The electrical conduction mechanisms are discussed.

DI1-MoP14 UHV-CVD of Al@sub 2@O@sub 3@ for Gate Dielectric Applications*, B.R. Rogers,* ***Z. Song****, R.D. Geil, T.P. Hanusa, R.A. Weller,* Vanderbilt University

Successful replacement of silicon dioxide-based MOSFET gate dielectrics by a high-permittivity (high-k) dielectric is a critical step in the continued drive to build the smaller, faster, lower-power, more-integrated circuits that society is demanding. Our goal toward this effort is to develop a thermodynamically and microstructurally stable, amorphous material system, having no interfacial silicon dioxide formation. In this presentation we will discuss our work on developing alumina/zirconia alloys for use as gate dielectrics. We have begun this effort by studying the deposition of alumina films in an ultra-high-vacuum chemical vapor deposition (UHV-CVD) system. We use a precursor of a mixed alkyl alkoxide aluminum dimer. This compound contains triethyl (tri-sec-butoxy) dialuminum, tetraethyl (di-sec-butoxy) dialuminum, and diethyl (tetra-sec-butoxy) dialuminum. This mixture is non-pyrophoric and is less susceptible to hydrolysis than other tialkoxide aluminums. Our studies have included total deposition pressures between 10@sup -5@ and 10@sup -3@ torr, and substrate temperatures between 350 and 500 °C. In addition we will discuss the characterization of these films using time-of-flight medium energy ion scattering (ToF-MEIS), a characterization capability unique to Vanderbilt University. . @FootnoteText@ This work is supported by the National Science Foundation grant # CTS-0092792.

DI1-MoP15 Annealing Effects of Al@sub 2@O@sub 3@ Films Grown on Si(100)*, Y.S. Roh,* *M.-H. Cho, Y.K. Kim, S.A. Park, D.-H. Ko, C.N. Whang, K.H. Jeoung,* Yonsei University, Korea

The annealing effects of the thin Al@sub 2@O@sub 3@ films grown on Si(100) by sputtering method was deeply investigated using various physical and electrical measurement methods. All the films grown in the temperature below 300@super o@C using sputtering Al@sub 2@O@sub 3@ target showed amorphous structure as examined by x-ray diffraction and transmission electron microscopy. The amorphous structure was maintained up to 600@super o@C and then transformed to @gamma@-Al@sub 2@O@sub 3@ phase above the annealing temperature of 600@super o@C . In particular, the characteristics of the leakage current density in MOS structure depended on the annealing temperature. The densification of the film due to the crystallization resulted in improved electrical characteristics; the crystallization enhanced the improvement of the dielectricity and breakdown field strength. Moreover, the depth profiling data using XPS showed that the improvement of the leakage properties in Al@sub 2@O@sub 3@ film closely related with the change of interfacial layer under the high temperature annealing. In particular, the fixed trap density was increased even after the annealing process, which resulted from the difference of the chemical state of the Al@sub 2@O@sub 3@ film along with the structural change.

DI1-MoP16 Studies on Ta@sub 2@O@sub 5@ Thin Films Deposited on Si(100) by MOCVD and Sputtering Techniques*, P. Passacantando, L. Lozzi, V. Salerni, P. Picozzi,* ***S. Santucci****,* University of L'Aquila, Italy

Tantalum oxide is one of the most promising dielectric materials to be used for high performance in integrated circuits and electronic packaging applications. In this work stoichiometric Ta2O5 thin films have been successfully grown on Si(100) substrate by metal-organic chemical vapor deposition (CVD) technique using tantalum ethoxide (Ta(OC2H5)5) as precursor and by DC sputtering in reactive Ar/O2 atmosphere. The growth rate, the stoichiometry, the surface morphology and the structural properties of the films growth with and without nitrogen passivation of the silicon substrate, have been studied by X-Ray Reflectivity (XRR), X-ray Photoelectron spectroscopy (XPS), Atomic Force Microscopy (AFM) and X-ray Diffraction (XRD). We observed how the formation of a SiO2 layer between the silicon substrate and the Ta2O5 deposited film is nearly totally inhibited by a pre-treatment at 750Â°C in NH3 flux of the H-terminated silicon surface before the Ta2O5 deposition. Furthermore, we observed that a post growth annealing in a O2/N2 mixture up to 850Â°C determines a lowering of the leakage current whose dominating mechanism has been attributed to trap assisted Frenkel-Poole emission.

DI1-MoP17 Microstructure of BaTiO@sub3@ Films Prepared by Electrochemical Depostion on Ti-Coated Silicon Substrates*, **C.-T. Wu,*** National Chung Hsing University, Taiwan*; F.-H. Lu,* National Chung Hsing University, Taiwan, Taiwan, R.O.C.

Crystalline BaTiO@sub3@ films were directly synthesized onto Ti-coated silicon substrates in highly alkaline condition at 55°C using Ba(OH)@sub2@ or Ba(CH@sub3@COO)@sub2@ as electrolyte. Titanium films were first deposited by Filtered Cathodic Arc Deposition (FCAD) of varying thickness about 0.2 µm, 2µm and 5µm onto silicon wafer. The electric charge of electrolysis was carefully controlled to grow appropriate thickness of BaTiO@sub3@ films by applying a anodic oxidation method. From previous studies using pure Ti plates as substrates, we prepared the films by the potentiodynamic method to the preset voltages. X-ray diffraction results showed cubic BaTiO@sub3@ phase could be present at low electrolytic voltage of 3 V and higher voltage of 75 V. The BaTiO@sub3@ films synthesized at 3 V develops uniformly distributed spherical like small particles, and crater-shaped and large-grained BaTiO@sub 3@ films were observed at 75 V. The great differences of morphology between these two electrolytic conditions were also verified by surface roughness measurements. SEM/EDS, AES and XPS were used to analyze the composition of BaTiO@sub3@ films. The growth mechanisms of BaTiO@sub3@ films were also discussed.

DI1-MoP18 Electrical Properties of BST Thin Films on Si Substrates*, **N.A. Suvorova**, A.H. Mueller, E.A. Irene,* University of North Carolina, Chapel Hill*; O. Auciello,* Argonne National Laboratory*; J.A. Schultz,* Ionwerks, Inc.

Among many materials with high dielectric constant for use in advanced MOSFET's, Ba@sub 0.5@Sr@sub 0.5@TiO@sub 3@ (BST) is one of the most promising candidates, since it has a static dielectric constant over 300 for bulk material. However, BST thin films always exhibit much lower dielectric constant. The formation of interfacial layers between BST and Si substrate results in reduction of the overall dielectric constant that dramatically decreases the capacitance of the stack. Our BST thin films studies@footnote 1@ have included in-situ real time material characterisation as well as ex-situ material and electronic characterizations. The present study focuses on electronic characterization of Al/BST/p-Si and Ir/BST/p-Si structures with and without intervening SiO@sub 2@ layers between BST and Si substrate. Among the electronic measurements included are the dielectric constant and leakage current of the BST thin films as well as interface charges. Attepmts will be made to correlate the electronic properties with the material characteristics that will be presented separately.@footnote 1@ @FootnoteText@ @footnote 1@ A.H. Mueller, N.A. Suvorova, E.A. Irene, O. Auciello, and J.A. Schultz. In-situ, real time studies of interface formation of BST thin films on Si substrates. Present Conference Proceedings.

DI1-MoP19 Thermal Decompostion Mechanisms of (Ba,Sr)TiO@sub 3@ Film Precursors*, **J.P. Senosiain**, C.B. Musgrave,* Stanford University

Next-generation memory devices will require high-permittivity dielectric materials able to handle sufficient charge as the dimensions of memory cells continue to scale down. Barium strontium titanate (BSTO) is a strong candidate for such applications, with a dielectric constant many times higher than that of the presently used silicon oxy-nitrides. To grow BSTO thin films effectively, a basic understanding of the precursor chemistry and deposition mechanism is needed, yet the literature in this areas is quite scarce. We have employed Density Functional Theory (DFT) and pseudopotential basis sets to study the thermal decomposition mechanisms of the @beta@-diketonate precursors: Ba(thd)@sub 2@, Sr(thd)@sub 2@ and Ti(OH)@sub 2@(thd)@sub 2@. In all these species, we find the metal-oxygen bond to be the weakest and thus the first to be broken. The cleavage of a second metal-oxygen bond leads to considerable geometric rearrangement and is energetically favourable. This is followed by the detachment of tert-butyl radicals and possible ring-closing reactions. Other decomposition channels, as well as their implications to the deposition process, are discussed in terms of their thermochemistry.

DI1-MoP20 Enhancement of Etching Characteristics of (Ba,Sr)TiO@sub 3@ Using Magnetically Enhanced Inductively Coupled CF@sub 4@/Ar Plasma*, D.P. Kim, C.I. Kim,* Chung-Ang University, Korea*; **T.H. Kim,*** Yeojoo Institute of Technology, Korea*; Y.J. Seo,* Daebul University, Korea*; E.H. Kim,* Cheju National University, Korea*; E.G. Chang,* Chung-Ang University, Korea

Now, three major trends in IC device fabrication are putting more functions on individual chips, fabricating faster chips, and lowering IC fabrication costs. Smaller memory cell increases its speed with using other materials sets like metal gates and electrodes, and high-k dielectrics. Ferroelectric (Ba,Sr)TiO@sub 3@ (BST) thin film have been attractive for advanced dynamic random access memories (DRAMs) applications due to its high dielectric constant. The smaller features need better plasma-etching processes to ensure etch fidelity and new features. Because the etch rate of BST thin film is low in a reactive ion etcher and an inductively coupled plasma etcher, magnetically enhanced inductively coupled plasma (MEICP) was used. Plasma density of MEICP is higher than that of RIE and ICP. In this study, BST thin films were etched in CF@sub 4@/Ar. The experiments were carried out with measuring etch rates and selectivity as a function of gas mixing ratio, rf power, dc bias voltage and chamber pressure. The maximum etch rate of BST thin film was 1800 Å/min at CF@sub 4@(10)/Ar(90), rf power of 600W, dc voltage of -300V, and chamber pressure of 5 mTorr. The selectivities of BST to Pt and photoresist were 0.6 and 0.7, respectively. The chemical states on the etched surface were investigated with x-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS). Atomic force microscopy (AFM) and scanning electron microscopy (SEM) were used to investigate the surface morphology of BST thin films exposed in plasma. X-ray diffraction (XRD) was evaluated to investigate physical properties of BST before and after etching process. Electrical property was characterized by measuring leakage current.

DI1-MoP21 Structural and Microwave Properties of Artificial BaTiO@sub 3@/SrTiO@sub 3@ Superlattice on MgO and SrTiO@sub 3@ Substrate by Pulsed Laser Deposition*, **J.H. Kim**, L. Kim, Y.N. Kim, D. Jung, Y.S. Kim, J. Lee,* Sungkyunkwan University, Korea

BaTiO@sub 3@ (BTO)/SrTiO@sub 3@ (STO) superlattice has been deposited on MgO and STO substrates by pulsed laser deposition (PLD). BTO/STO superlattice has an epitaxial layer of BTO and STO with the parallel crystallographic orientation to MgO or STO substrates. The periodicity of the BTO/STO superlattice was varied from 0.8 nm thickness to 50 nm and the total thickness of the superlattice was fixed at 100 nm. Structural properties of the superlattice with various periods were examined by X-ray diffraction (XRD) and high resolution transmission electron microscopy (HRTEM). This superlattice exhibited ferroelectricity in capacitance-voltage (C-V) characteristics, i.e., inverted butterfly hysteresis loop. Asymmetric behavior in C-V characteristics were also observed in the superlattice, which had different bottom and top electrodes each other. For microwave applications, the voltage tunability in the C-V characteristics was measured. The voltage tunability increased with decreasing the period of the superlattice. The tunability reached 90 % at the period of 2 nm. The tunability of BTO/STO superlattice was discussed in terms of periodicity and strain relaxation.

DI1-MoP22 Ferroelectric PMNT Thin Films Deposited on TiN:O@sub 2@ by Laser Ablation*, **J.M. Siqueiros,*** UNAM, Mexico*; A. Fundora, J. Portelles,* Universidad de La Habana, Cuba

Pb(Mg@sub 1/3@Nb@sub 2/3@)@sub0.9@Ti@sub 0.1@O@sub 3@ (PMNT) polycrystalline thin films were deposited on TiN/Si substrates at different temperatures by laser ablation, using a wavelength of 248 nm, 30 ns pulse duration, 10 Hz repetition rate and a fluence of 2 J/cm@super 2@. As a result of this previous study, it was determined that deposits at 250 @super 0@C in a 200 mTorr oxygen atmosphere gave the best results with a post annealing treatment at 500 @super 0@C where a PMNT perovskite single phase formation was confirmed by x-ray diffraction (XRD) analysis. Higher and lower annealing temperatures presented a secondary pyrochlore phase. The electrical properties and the influence of the annealing temperature on the dielectric properties of the PMNT thin films were characterized through P-E hysteresis. Fatigue measurements were used to evaluate the long-term performance of the PMNT/TiN/Si system. The characteristics of the TiN films used as bottom electrodes were evaluated using Auger Electron Spectroscopy (AES) and Transmission Electron Microscopy (TEM) with particular emphasis in the interfaces. @footnote 1@ This work has been partially supported by CoNaCyT-Mexico, through grant No. 33586E and by DGAPA-UNAM grant No. IN104000. The technical support by I. Gradilla, E. Aparicio, V. Garcia and F. Ruiz is acknowledged.

Dielectrics

Room 134/135 - Session DI2-MoP

Low K Dielectrics Poster Session

DI2-MoP1 Deposition of Si-C-O-H Alloy Dielectric Films as a Low Dielectric Permittivity Insulators*, B.K. Hwang,* Dow Corning Corporation*; M.J. Loboda,* Wacker Siltronic Corporation*; W.D. Gray, G.A. Cerny, R.F. Schneider, J.A. Seifferly, D.W. Roehl,* Dow Corning Corporation

As the feature size in ultra large scale integrated circuit (ULSI) decreases, the minimization of interconnect resistance - capacitance (RC) coupling through the use of copper interconnect metalization and low dielectric permittivity (low-k) has become an intensive interest to the semiconductor industry. Among many low-k candidate materials, carbon-doped silicon oxides, i.e., Si-C-O-H alloy dielectric films have been investigated. These films can be deposited by plasma enhanced chemical vapor deposition (PECVD) of organosilicon gas, (CH3)xSiH4-x, and oxidant mixtures. In this study, we will present the structure, composition, and electrical characteristics of PECVD Si-C-O-H films with different process parameters. The precursor gas mixture used in this study is the trimethylsilane (Dow Corning Z3MS(TM), Semiconductor Grade), oxygen (O2), and helium (He). Samples of Si-C-O-H films were deposited on silicon wafers using a 200mm PECVD reactor. Rutherford backscattering spectrometry and hydrogen forward scattering spectrometry (RBS/HFS), Fourier transform infrared spectroscopy (FTIR), and X-ray photoelectron spectroscopy (XPS) were evaluated to understand the composition and structure of films. The electrical properties such as a dielectric constant, leakage current density, and dielectric breakdown voltage were tested with a metal-insulator-silicon (MIS) structure. The typical film properties of this study are as follows: (1) FTIR spectra indicate that the hydrogen and carbon are incorporated in the form of Si-(CH2)n-Si, Si-H, Si-CH3, and Si-C into a SiO2 backbone. (2) Composition of Si-C-O-H film : Si / O / C / H = 0.2 / 0.36 / 0.12 / 0.32 (based on RBS/HFS). (3) Bulk film density : 0.97 (g/cm3). (3) Dielectric constant (k) at 1MHz : 2.7 ~ 3.2 and k value has a strong relationship with Si-OH content. (5) Leakage current density : 3x10-10 (A/ cm2) at 0.5 (MV/cm) (6) Dielectric breakdown field : > 4 (MV/cm).

DI2-MoP2 Characterization of Plasma-CVD Grown Low-k Porous Silica Films using Positron-annihilation Lifetime Spectroscopy*, T. Ohdaira,* *R. Suzuki,* National Institute of Advanced Industrial Technology (AIST), Japan*; Y. Shioya,* Semiconductor Process Laboratory Co., Ltd., Japan*; T. Ishimaru,* Canon Sales Co. Inc., Japan

Positron-annihilation lifetime spectroscopy was used to determine the pore size distributions in low-k porous silica films deposited by plasma-enhanced chemical vapor deposition (PE-CVD) with source gases of hexamethyldisiloxane (HMDSO) and nitrous oxide (N@sub 2@O). In PE-CVD, the porosity of the film can be controlled by the deposition conditions, e.g. the pressures and flow rates of the source gases. In the present study, several kinds of porous films with k values ranging from 2.6 to 3.2 were prepared. The positron-annihilation lifetimes at selected depths in the porous films (500 nm thick) were measured by using a mono-energetic pulsed positron beam (0.5 keV - 20 keV). The obtained results show that the pores with average volumes of 0.3 - 1.1 nm@super 3@ are introduced in the films, and that the pore size strongly depends on the deposition conditions. The correlation between the pore size and the dielectric constant will be discussed.

DI2-MoP3 Plasma-Reacting Behaviour of Spin-on Hybrid Organic Siloxane Polymer (HOSP) Low-Dielectric-Constant Thin Films*, S.-T. Chen,* *G.-S. Chen,* Feng Chia University, Taiwan*; T.-C. Chang,* National Sun Yat-Sen University, Taiwan*; C.-P. Liu,* National Cheng Kung University, Taiwan

This work employs Fourier transform infrared spectroscopy and Raman spectroscopy, along with atomic force and transmission electron microscopies to examine microstructure and bonding stabilities of spin-on hybrid organic siloxane polymer (HOSP) low-dielectric-constant (k) thin films after they are exposed to oxygen ashing and (or) various passivating plasma treatments. The spectroscopic and microscopic analyses reveal that, upon exposure to the oxygen plasma, the Si-CH@sub 3@ and Si-C bonds inherent in the thin HOSP (k = 2.5) film are disrupted substantially and, subsequently replaced by highly polarized Si-O, Si-H and (or) Si-OH bonds. These replacements thus degrade the HOSP dielectric film by increasing the magnitude of k significantly. Preliminary results indicate that the HOSP film can be strengthened by passivating it in an adequate plasma. Doing so allows the HOSP to be treated by oxygen-plasma ashing while still maintaining a fairly stable bonding and dielectric properties. Finally, the capability of several ultra-thin (<= 5 nm) capping layers in retarding copper diffusion into the HOSP dielectric layer will be evaluated by measuring C-V and I-V curves of Si/HOSP/capping layers/Cu capacitor samples under conditions of biased thermal stress of 2-4 MV/cm and 150-250 °C.

DI2-MoP4 Process Characterization of Low Dielectric Constant Silicon Containing Fluorocarbon Films by Plasma Enhanced Chemical Vapor Deposition*, Y.Y. Jin,* Louisiana State University*; H. Kim,* Kyungpook National University, S. Korea*; G.S. Lee,* Louisiana State University

The development of low dielectric constant (low-k) materials has become one of the most important key challenges for interlayer dielectrics (ILD) of the high performance ultra-large-scale-integration (ULSI) devices. As the decreased design rule and increased complexity of ULSI circuits have essentially increased the crosstalk and RC time delay caused by parasitic capacitance, a great deal of effort has been spent in reducing the dielectric constant of the interlayer as well as reducing the resistance of the wiring metals. Silicon containing fluorocarbon (SiCF) thin films for use as low dielectric ILD have been investigated. The SiCF films were deposited with plasma enhanced chemical vapor deposition (PECVD) using 5% disilane in helium (5%Si2H6/He) and carbon tetrafluoride (CF4) as the precursors. The properties of SiCF films effected by the total flow, the flow rate ratio of CF4/Si2H6 and annealing were investigated to obtain optimal deposition. This work presents the results of a process characterization of PECVD which are the deposition rate, the refractive index and the roughness as functions of the total flow and the flow ratio, and the shrinkage rate and the dielectric constant before/after annealing.

DI2-MoP5 Etching Characteristics of Polyimide Film as Interlayer Dielectric Using Inductively Coupled Plasma*, P.S. Kang,* *C.I. Kim,* Chung-Ang University, Korea*; S.G. Kim,* ETRI, Korea*; H.S. Choi,* Juseong College, Korea*; C.I. Lee,* Ansan College of Technology, Korea*; E.G. Chang,* Chung-Ang University, Korea

In ultra-large-scale integrated circuits, where critical dimensions continue to shrink into the deep submicrometer range, RC constant becomes an increasingly dominant factor in governing both the velocities of operation and the corresponding power consumption. One method to reduce RC constant is the reduction of the dielectric constant of the intermetal material. Therefore, many low-k materials such as amorphous carbon, Teflon, SiOF, Polyimide have been studied by the various research institutes. Among them polyimide (PI) films are widely due to low dielectric constant ,low water absorption, high gap-fill and planarization capability. In this study, etching characteristics of polyimide film with O@sub 2@/CF@sub 4@ gas mixing was studied using inductively coupled plasma (ICP). The etch rate and selectivity were evaluated to rf power, dc-bias voltage, chamber pressure, and substrate temperature. High etch rate (over 10000Å/min) and vertical profile was acquired in CF@sub 4@/(CF@sub 4@+O@sub 2@) of 0.2. The selectivities of polyimide to PR and SiO@sub 2@ was 1.1, 34, respectively. The profiles of polyimide film etched in CF@sub 4@/O@sub 2@ were measured by a scanning electron microscope (SEM) with using an aluminum hard mask pattern. The chemical states on the PI film surface were measured by x-ray photoelectron spectroscopy (XPS). Ion current density and plasma density of O radical and fluorine in O@sub 2@/CF@sub 4@ were investigated by Langmuir probe and optical emission spectrometer (OES). After the etching process, leakage current and dielectric constant were characterized by semiconductor parameter analyzer (HP4145B) and impedance analyzer (HP 4192 at 1MHz) using Al/PI/Al capacitor.

DI2-MoP6 An Opportunity to Study the Outgassing Behavior of a Novel Organic Low K Material*, J.F. Bernard,* *S. Pangrle, C. Gabriel,* Advanced Micro Devices

Lowering interlayer dielectric(ILD) capacitance is key to enjoying the benefits of further advances in IC design and Cu interconnect technology. Conventional SiO2 is now being replaced as an ILD by an array of new materials. In some cases porosity is used to lower k, in others the films are actually novel organic materials. These new low k dielectrics can behave very differently from the SiO2 used in conventional IC fabrication to date. Outgassing is one metric that is a direct measure of film stability, curing, and contamination. Organic films especially can exhibit significant changes in outgassing vs. etch, cleaning and thermal budget. This complex outgassing of organics due to or during processing is a definite departure from SiO2, even for organo-precursor based glasses such as TEOS. We at AMD have had the opportunity to extensively study the outgassing behavior of DOW Chemical's organic low k, SiLK, with both Dynamic and Isothermal Evolved Gas Analyses(EGA). Two distinct regimes of outgassing were observed. At lower temperature atmospheric contaminants are dominant. Benzene related film outgassing was observed above 450°C.

XPS analyses confirmed the presence of aromatic binding. The stability of SiLK with respect to various processing steps was investigated with interesting results. These investigations led us to also take a look at our wafer storage materials. The affinity for the absorption of organics was demonstrated and minimized. The effects of processing on a porous derivative were examoned with an etch and clean matrix. Overall evolved gas analyses are proving to be a key data point in understanding and, ultimately, utilizing low k films in advanced IC fabrication.

DI2-MoP8 The Effect of Hydrogen Plasma Treatment on Low-k Hybird-Organic-Siloxane-Polymer (HOSP) Against Damage During Photoresist Removal*, T.C. Chang,* National Sun Yat-Sen University, Taiwan, R.O.C.*; Y.S. Mor,* National Chiao Tung University,Taiwan, R.O.C., Taiwan, R.O.C.*; **P.T. Liu,*** National Nano Device Laboratory, Taiwan, R.O.C*; T.M. Tsai, C.W. Chen,* National Chiao Tung University, Taiwan, R.O.C.*; W.C. Gau,* National Tsing Hua University, Taiwan, R.O.C.*; S.M. Sze,* National Chiao Tung University, Taiwan, R.O.C.

While critical dimensions continue to shrink into the deep submicron range for the need of ULSI circuit, the RC constant that governs both the parasitic delay time (i.e. the speed of operation) and corresponding power dissipation, becomes a dominant factor in improving the chip performance. An organic SOG, the Hybird-Organic-Siloxane-Polymer (HOSP) has high evaluation in ULSI applications because of the low dielectric constant about 2.5. It is also one suitable material of Methyl-Hybrido-Silsesquioxane (MHSQ) films, and simultaneously has good gap filling, low stress and comparable enough strength etc. Face with the same issues of organic low k materials, however, the quality of HOSP film is degraded after photoresist removing. This instability is one of the major problems in using HOSP as a low-k material. In this study, the HOSP film has been investigated for the intermetal dielectric application. In addition, H@sub 2@ plasma pre-treatment was applied to HOSP films. This treatment prevents HOSP films from O@sub 2@ plasma and chemical wet stripper damage during photoresist stripping processes. In the H@sub 2@ plasma treatment, hydrogen radicals can passivate the HOSP surface, preventing the formation of Si-OH bonds so that moisture uptake can be avoided. In addition, dielectric degradation due to photoresist stripping process can thereby solve by H@sub 2@ plasma treatment. These experimental results indicate that H@sub 2@ plasma treatment is a promising technique for integrating the HOSP as intermetal dielectric application.

Dielectrics
Room 130 - Session DI-TuM
High K Dielectrics II

Moderator: Y. Yasuda, Nagoya University, Japan

8:20am **DI-TuM1 Vibrational and Band-Gap Engineering of Transition Metal Oxides for High-k Gate Applications***, **S. Zollner**, R. Liu,* Motorola SPS **INVITED**

CMOS devices will change around 2005, when the SiO2 thickness reaches 15-20 A and the gate length 0.1 um. Beyond that, the physical thickness of the gate oxide can no longer shrink, since the leakage currents due to tunneling render the devices useless. Instead of reducing the physical thickness, scaling the gate length is accompanied by increasing the low-frequency dielectric constant k of the gate oxide. Apart from a number of requirements related to stability under CMOS processing, new gate oxide materials need to have properties that can be engineered by changing the electronic band structure and the vibrational properties: (1) A large band gap with reasonable band offsets compared to the valence and conduction bands of Si. (2) A large lattice polarizability, which can be associated with a soft phonon driving a transition between two crystalline phases. In a way, engineering of the band gaps and band offsets of high-k gate oxides is not too different from band-engineered semiconductors, such as SiGe:C or InGaP for heterostructure bipolar transistors. Optical spectroscopies (spectroscopic ellipsometry from 300 um to 9 eV, FTIR transmission and reflection, UV Raman scattering) and x-ray structural analysis are ideally suited for a rapid screening of a large class of materials for potential high-k applications, since they do not require processing for electrical measurements. Ab initio band structure calculations can assist in the interpretation of experimental results. This talk will describe recent work on SrTiO3 and various transition metal oxides (TiO2, ZrO2, and HfO2). Specifically, we will show how the band gap of SrTiO3 can be increased by 0.5 eV or more through changing the composition, which reduces the leakage currents of metal-gate CMOS devices. @FootnoteText@ Collaborators: R. Gregory, P. Fejes, A. Demkov, J. Curless, Z. Yu, J. Ramdani, R. Droopad, K. Reid, B.-Y. Nguyen, T.E. Tiwald, J.N. Hilfiker, J.A. Woollam.

9:00am **DI-TuM3 Electrical and Physical Characteristics of Sputtered HfO@sub 2@ Films for Alternative Gate Dielectrics***, **S.-W. Nam**, J.-H. Yoo, H.-J. Choi, S. Nam, D.-H. Ko,* Yonsei University, Korea*; J.-H. Ku,* R&D Center Semiconductor Samsung Electronics Co., Korea*; M.-H. Cho,* Yonsei University, Korea*; S. Choi,* R&D Center Semiconductor Samsung Electronics Co., Korea*; C.-W. Yang,* Sungkyunkwan University, Korea

SiO@sub 2@ has been used as the primary gate dielectric material in MOSFET devices for over 40 years. As the thickness of SiO@sub 2@ decreases, a direct tunneling of carriers through the potential barrier occurs, which results in the significant leakage current through the SiO@sub 2@ layer. Because of this issue, a conventional SiO@sub 2@ process shows limitation in the fabrication of CMOS devices in sub-2.0nm thickness regime. Therefore, the development of alternative dielectric materials is required for the fabrication of sub-0.1µm MOSFET devices. Dielectric materials with a high dielectric constant, large band-gap, low interface state density, and good thermal stability have drawn a lot of attention as alternative gate dielectric materials. Recently, HfO@sub 2@ has been considered as promising alternative materials due to high dielectric constant and good thermal stability with Si substrates. We have studied the microstructures and electrical properties of HfO@sub 2@ films. The HfO@sub 2@ thin films on (100) silicon substrate treated by a HF solution, chemical oxide, and NH@sub 3@ nitridation were deposited by reactive dc magnetron sputtering for gate dielectrics applications, followed by Pt sputtering for gate electrode. The resulting films were analyzed by ellipsometry, XRD, HRTEM, RBS, and XPS/AES. The crystalline peaks with orthorhombic phase of HfO@sub 2@ were observed in the films annealed at elevated temperatures (>650°C). By HRTEM and XPS/AES analyses, we observed the properties of HfO@sub 2@ films and the interfacial layers between the HfO@sub 2@ films and the Si substrate upon annealing. The electrical properties were assessed by C-V and I-V measurements for MOS structures.

9:40am **DI-TuM5 Solid State Reactions in Hafnium Silicate Thin Films***, H.T. Johnson-Steigelman, A.V. Brinck, **P.F. Lyman**,* University of Wisconsin-Milwaukee

Oxides and silicates of hafnium are promising high-dielectric candidates for microelectronics applications because it seems likely that these materials will be stable at their interface with silicon@footnote 1@ due to the large heat of formation of Hf oxides. If hafnium oxides and silicates are indeed stable against reduction by Si at the dielectric/silicon interface, then, as a corollary, Hf metal should be able to reduce SiO@sub 2@. This supposition was tested by forming nm-thick films of hafnium silicates by solid state reaction of Hf metal films deposited on SiO@sub 2@ in ultrahigh vacuum. Charge transfer during the reaction was monitored by examining the binding energies of the Hf 4f and Si 2p core levels using x-ray photoelectron spectroscopy (XPS). As predicted, the Hf levels shifted to deeper binding energies upon annealing, while the Si core level corresponding to SiO@sub 2@ shifted to shallower binding energy. These shifts are consistent with charge being transferred from the Hf to the Si atoms, as would be expected for reduction of SiO@sub 2@ by Hf. Other aspects of the reaction between Hf, O, and Si were explored using thicker (µm) films. It is clear from these investigations that Hf metal can consume SiO@sub 2@ layers, with sometimes surprising results. @FootnoteText@ @footnote 1@ G.D. Wilk and R.M. Wallace, Appl. Phys. Lett. V.76, p.112 (2000)

10:00am **DI-TuM6 Kinetic Study on ZrO@sub 2@-CVD using Zirconium-Tetra-tertiary-Butoxide***, **T. Kawamoto**, Y. Shimogaki,* University of Tokyo, Japan

ZrO@sub 2@ films have lately attracted much attention as high-k dielectrics for high performance ULSI gate applications. We carried out kinetic study on ZrO@sub 2@-CVD by using hot-wall tubular reactor to understand the basic reaction mechanisms. Zirconium-Tetra-tertiary-Butoxide (ZTB) was used as the Zr source and injected into the reactor by bubbling with He. We investigated the fractured surface of the sample by FE-SEM to obtain the growth-rate and step coverage of deposited ZrO@sub 2@ films on Si substrate with microtrenches. The deposition profile at 663K showed the increase in the up-stream part, and then the decrease was observed in the down-stream part. This implies that this reactive process has the special path, precursors decomposed into intermediate species by the gas-phase reaction, and the intermediate species deposits on growing surface. Furthermore, we examined depositions into the trench substrates with different aspect ratio at several positions in the reactor, and could found out that the step coverage became poorer, as samples were laid further from inlet. As a result of carrying out fitting these experimentally observed step coverage profiles with a single species model, the predicted composition profiles did not match well with the all observed profiles. This result indicates that some growth species contribute to film growth. Then, by fitting with two species model, we determined reactive sticking coefficients of two growth species; @eta@@sub 1@=0.0095 and @eta@@sub 2@=0.20, respectively. And we found out that the less active growth species (@eta@@sub 1@=0.0095) existed dominantly in the up-stream part, on the other hand, the high active growth species (@eta@@sub 2@=0.20) did the same role in the down-stream part. The dependence of the step coverage quality on the distance from inlet could be explained by the relative ratio of these species. The film properties may have different characteristics by this precursor ratio.

10:40am **DI-TuM8 Correlations Between Local Bonding and Electronic Structure, and Gate Dielectric Performance of Zirconium Silicate Alloys***, **G. Rayner, Jr.**, D. Kang, M. Schultz, G. Appel, G. Lucovsky, H. Ade, D.E. Aspnes, D.E. Sayers,* North Carolina State University

Zirconium silicate alloys have been prepared by remote plasma enhanced metal organic chemical vapor deposition, RPE-MOCVD, using down-stream injected SiH@sub 4@ as the Si-atom source, Zr(IV) t-butoxide as the Zr-atom source, and plasma excited O@sub 2@/He mixtures to produce active oxygen species to drive the deposition reactions. Bulk film properties have been studied for as-deposited films, and films subjected to post-deposition annealing at temperatures to 1000C in an Ar ambient. This paper extends previously reported studies of thermal stability (chemical phase separation and crystallization) by infrared, IR, spectroscopy and x-ray diffraction, XRD.@footnote 1@ Specific spectroscopic studies include i) x-ray photoelectron spectroscopy, XPS, ii) x-ray absorption spectroscopy, XAS, iii) extended x-ray absorption fine structure, EXAFS, and iv) spectroscopic ellipsometry, SE. The spectroscopic studies have confirmed that the lowest lying anti-bonding states are derived from d-states of the Zr-atoms. Results demonstrate that the energy of these states relative to vacuum, and the Si conduction band, do not change as a function of alloying, or as a function of long or short range order. This result is consistent with a molecular orbital description of the electronic structure derived from the Zr d-states. This aspect of the electronic structure has important implications for the interpretation of electrical studies, e.g., current-voltage and capacitance-voltage measurements that are also reported in this talk. For example, changes in the coordination and bonding symmetry of the bonding and anti-bonding orbitals derived from Zr d-states provide insights into the microscopic mechanism responsible for enhancements in the dielectric constant at low ZrO@sub 2@ concentrations.@footnote 2@ Supported by ONR, SRC and the Sematech SRC Center for Front End Processes @FootnoteText@ @footnote 1@ G. Rayner, R. Therrien and G. Lucovsky, MRS Symp Proc 611, c1 3.1 (2001) @footnote 2@ G. Lucovsky and G. Rayner, Appl. Phys. Lett. 77, 2912 (2000).

11:20am **DI-TuM10 Interface Reactions of High-K Y@sub 2@O@sub 3@ and Gd@sub 2@O@sub 3@ Gate Oxides with Si***, B.W. Busch,* Agere Systems*; W.H. Schulte,* Rutgers University*; R. Kwo, M. Hong, J.P. Mannaerts, B.J. Sapjeta,* Agere Systems*; T. Gustafsson,* ***E. Garfunkel,*** Rutgers University

Ultrathin Y2O3 and Gd2O3 films were e-beam evaporated onto Si(100) and investigated by high-resolution medium energy ion scattering with and without in-situ Si capping layers. Si-capped metal oxide films were stoichiometric (M2O3), and their interface with the Si substrate was sharp. Uncapped films that were exposed to air, however, contained excess oxygen and showed a 6-8 @Ao@ thick interfacial layer. Other than limited intermixing between the capping Si and metal oxide layers during deposition, the oxides did not react with the initially-amorphous Si overlayer until ~800 °C. Uncapped films showed additional Si uptake from the substrate at ~700 °C, while the capped films did not react with the substrate until ~900 °C. Results are discussed within the framework of the relevant solid-solid and solid-gas thermodynamics and kinetics. This work demonstrates the critical importance of gas ambient during growth and processing of high-K gate oxides.

Dielectrics
Room 130 - Session DI-TuA
High K Dielectrics III

Moderator: S. Zollner, Motorola SPS, PMCL

2:00pm **DI-TuA1 Post-deposition Densification of Yttrium Oxide High Dielectric Constant Insulators Deposited by Oxygen Plasma Assisted Chemical Vapor Deposition*, D. Niu,*** *R.W. Ashcraft, G.N. Parsons,* North Carolina State University

Understanding and controlling interface and bulk chemical stability of CVD high-k dielectrics is an important research issue. Several groups report that the equivalent oxide thickness of vapor deposited dielectrics changes during post-deposition processing, but mechanisms that control the changes are not well understood. We examine the effect of post-deposition annealing on yttrium-based high-k dielectrics formed by oxygen plasma assisted CVD at temperatures between 350 and 450°C. Using yttrium-based materials, our group has previously demonstrated dielectrics with equivalent oxide thickness of 10-12Å with k=14. In this work, depositions were compared on Si(100) using two different yttrium diketonate precursors introduced downstream from a remote oxygen plasma source. Physical film thickness ranged from 1000Å, and films were characterized using IR, XPS and IV and CV electrical analysis, before and after annealing at temperatures >900°C. For the thin films, XPS indicates mixing of yttrium and oxygen with silicon at the substrate interface during deposition. Over a wide range of thickness, as deposited Y@sub2@O@sub3@ films show evidence for O-H and C-H bonds in the IR spectra. After annealing at 900°C in N@sub2@ (with >10@super-5@ Torr O@sub2@ pressure), the IR shows almost complete removal of O-H and C-H bonds. The films also show a remarkable decrease in macroscopic thickness (e.g. from 600Å to ~400Å after annealing at 900°C for 10 minutes), which cannot be accounted for simply by film crystallization. After anneal CV analysis shows good behavior, with evidence for positive fixed charge and substrate oxidation. This data suggests that density of as deposited CVD dielectrics is a critical issue, and hydroxyl bonds present in as-deposited films can react at the interface during post-deposition annealing. Approaches to control hydroxide incorporation and improve material stability will be presented and discussed.

2:40pm **DI-TuA3 Substitutional Effects of the Dielectric Constant in Ta@sub 2@O@sub 5@*, K. Larsson,*** *J. Westlinder, H.-O. Blom, J. Olsson,* Uppsala University, Sweden

Tantalum pentoxide (Ta@sub 2@O@sub 5@) is considered to be a promising candidate as a dielectric material. The reported dielectric constant (@epsilon@? for Ta@sub 2@O@sub 5@ ranges between 20-40. Depending on annealing temperature, process temperature and process method, the Ta@sub 2@O@sub 5@ films have crystallised into different phases. Since @epsilon@ is greatly dependent of phase of Ta@sub 2@O@sub 5@ as well as dependent of various solutions of additives (e.g., Ti, Zr, Nb), it is of a large interest to study and compare different phases and solutions separately. The purpose with the present study has been to theoretically investigate the substitutional effect of various additives (Ti, Zr, Hf, V, Nb, Sn) in the @beta@-phase of Ta@sub 2@O@sub 5@ on the dielectric constant. The ionic, as well as the electronic, part of the dielectric function have then been calculated for mono-crystalline materials, using the first principle Density Functional Theory. In addition, the electronic part of @epsilon@ has also been calculated for a polycrystalline material as well. In the present study, an atomic substitution of 12 % of Ta with Ti, Zr, Hf, V, Nb and Sn, respectively, has been performed with a maintained ideal stoichiometry. For the situation with a Ti solution, the substitutions of 8 and 13 atom% were also used. As a general result, dielectric constants very similar to experimentally obtained values have been theoretically calculated in the present investigation.

3:00pm **DI-TuA4 Ta d-state Derived Electron Traps in non-Crystalline Al@sub 2@O@sub 3@-Ta@sub 2@O@sub 5@ Alloys Prepared by Remote PECVD*, R.S. Johnson,*** *J.G. Hong, G. Lucovsky,* North Carolina State University

The bonding coordination of Al and Ta in Al@sub 2@O@sub 3@ and Ta@sub 2@O@sub 5@ is known, respectively, from Al27 nuclear magnetic resonance, NMR,@footnote 1@ and X-ray diffraction, XRD.@footnote 2@ There are 4- and 6-fold coordinated Al-atoms in non-crystalline Al@sub 2@O@sub 3@ and these are bonded to 3-fold coordinated O-atoms. XRD of high temperature crystalline Ta@sub 2@O@sub 6@ indicates a mix 6- and 8-fold coordinated Ta, with 2- and 3-fold coordinated O-atom neighbors. FTIR and Raman studies confirm similar bonding arrangements in non-crystalline Ta@sub 2@O@sub 5@. Non-crystalline Al@sub 2@O@sub 3@-Ta@sub 2@O@sub 5@alloys have been prepared by remote PECVD. Robertson@footnote 3@ has shown that the anti-bonding Ta d-state energy levels are significantly below the p-states of Al and Si and cause a reduced conduction band offset with Si of ~0.36 eV. Miyazaki@footnote 4@ has measured band offsets by photoemission and has found good agreement with theory. The temperature dependence of C-V and J-V traces for capacitors with Al@sub 2@O@sub 3@-Ta@sub 2@O@sub 5@ dielectrics indicate trapping and trap release that is consistent with the trapping states being associated with anti-bond d-states of Ta. In particular, hysteresis in the C-V traces is consistent with electron trapping, and is significantly increased by addition of Ta@sub 2@O@sub 5@ into Al@sub 2@O@sub 3@. The temperature dependence of J-V traces, combined with the C-V traces is consistent with different activation energies for electron trapping, and trap release. The energies obtained from analysis of the data are in agreement with conduction band offset energies determined from the photoemission studies of Miyazaki.@footnote 4@ The activation for electron injection into Ta trapping states is 0.30±0.05 eV, consistent with the energy of empty Ta-atom d-states relative to the Si conduction band. The activation energy for trap release is 1.5±0.1 eV, in agreement with the energy difference between these Ta d-states and the Al@sub 2@O@sub 3@ conduction band position as determined from band offset energy measurements.@footnote 4@ Supported by the Office of Naval Research and the SEMATECH/SRC Front End Processing Center @FootnoteText@ @footnote 1@ D. Muller, W. Gessner, H.J. Behrens, and G. Scheller, Chem. Phys. Lett. 59, 79 (1981). @footnote 2@ N.C. Stephenson and R.S. Roth, J. Solid State Chem. 3, 145 (1971). @footnote 3@ J. Robertson, J. Vac. Sci. Technol. B 18, 1785 (2000). @footnote 4@ S. Miyazaki, presented at PCSI 28, Lake Buena Vista, FL, 7-11 January 2001, submitted to J. Vac. Sci. Tech. B (2001).

3:20pm **DI-TuA5 Angle-Resolved XPS and Auger Analysis of Ultra-Thin Al@sub 2@O@sub 3@ Films Deposited by Atomic Layer Deposition*, O. Renault*,** *D. Rouchon, L. Gosset, A. Ermolieff,* CEA/Grenoble-LETI, France

Ultra-thin (1-4.5 nm) aluminium oxide (Al@sub 2@O@sub 3@) films prepared by Atomic Layer Deposition on HF-passivated Si substrates were characterized by ARXPS and AES. Results were analysed in terms of chemical quality of the oxide layer as well as physico-chemical characteristics of the intermediate layer, before and after RTP annealing. For both as-deposited and annealed films, Al2p and Si2p line analysis revealed that only Al-O bonds were present (neither Al-Al bonds@footnote 1@ nor silicate-type compounds@footnote 2@ were observed at the interface with the substrate); the films, as well as 50 nm-thick ones, were found to be stoechiometric with O/Al ratios around 1.5. For as-deposited films, decomposition of the O1s line evidenced the formation of Al-OH groups@footnote 3@ during the deposition process; their concentration was maximum at the surface and decreased as the depth probed increased; this additional contribution of Al-OH bonds to the O1s signal was not observed on annealed films. Results gained from both decomposition of the Si2p line at different analysis angles and AES depth profiling showed that an intermediate layer of oxidized Si grows up upon annealing, its thickness being related to that of Al@sub 2@O@sub 3@ and equal to 0.6±0.2 nm for 2.5 nm-thick films; sub-oxides appear to be localized at the Si interface whereas fully oxidized Si forms above. Additional results concerning films deposited on thermally grown SiO2-coated Si substrates will be also presented. @FootnoteText@ @footnote 1@ Yang et al., Surf. Coat. Technol. 131 (2000) 79-83 @footnote 2@ Klein et al., Appl. Phys. Lett. 75 (25), 4001 (1999). @footnote 3@ Alexander et al., Surf. Interface Anal. 29, 468 (2000).

3:40pm **DI-TuA6 In-situ, Real Time Studies of Interface Formation of BST Thin Films on Si Substrates*, A.H. Mueller,*** *N.A. Suvorova, E.A. Irene,* University of North Carolina, Chapel Hill*; O. Auciello,* Argonne National Laboratory*; J.A. Schultz,* Ionwerks, Inc.

The decrease in feature size of electronic devices and the commensurate electronic properties scaling has resulted in a search for new materials to achieve the electronic properties required for such miniature technologies. Ba@sub 0.5@Sr@sub 0.5@TiO@sub 3@ (BST) and other oxide films have become the front-runners in a search for materials to replace existing dielectrics in future technologies. Precluding the integration of BST as a gate dielectric into silicon devices are issues regarding the interface quality between the dielectric and semiconductor as well as the metal contact, as these affect critical electrical properties of the film such as the magnitude of the dielectric constant and the leakage current. In-situ studies of the oxygen incorporation into these films and the interface formation between BST films and Si substrates using time of flight ion scattering and recoil spectrometry (ToF-ISARS) as well as spectroscopic ellipsometry (SE) are presently being employed to ascertain conditions which minimize interface intermixing and maximize oxygen incorporation during reactive ion beam sputter deposition, and these studies comprise the focus of this presentation. Ex-situ material and electronic characterizations have also been used to characterize devices (Ir/ BST/ Si) prepared completely in vacuo and have shown the film's overall dielectric constant to be reduced by an intermixed layer of BST and Si substrate possessing an intermediate dielectric constant, while leakage characteristics of the film indicate a dependence upon the degree of oxygen deficiency as well as the BST/ metal contact interface quality. The electronic characterization studies will be presented separately.@footnote 1@ @FootnoteText@ @footnote 1@ N.A. Suvorova, A.H. Mueller, E.A. Irene, O. Auciello, and J.A. Schultz. Electrical properties of BST thin films on Si substrates. Present Conference Proceedings.

4:00pm **DI-TuA7 Direct Observation of Atomic Disordering at the SrTiO@sub 3@/Si Interface Due to Oxygen Diffusion***, **V. Shutthanandan**, S. Thevuthasan, Y. Liang,* Pacific Northwest National Laboratory*; Z. Yu, R. Droopad,* Motorola Labs

Since CMOS devices based on the conventional dielectric material, SiO@sub 2@, will soon reach their dimensional limits in device technology, alternative high dielectric materials received much attention in recent years. Several oxides are being considered as alternative dielectric materials and strontium titanate is one of the most attractive choices of such materials. Recently, single crystal SrTiO@sub 3@(100) films have been successfully grown on Si(100) substrates at Motorola.@footnote 1@ The stability of these films that were grown at Motorola was studied as a function of temperature under various control environments including vacuum, hydrogen and oxygen using Rutherford backscattering spectrometry (RBS) along with channeling techniques, nuclear reaction analysis (NRA) and x-ray photoelectron spectroscopy (XPS) at Pacific Northwest National Laboratory (PNNL).@footnote 2@ Results from channeling measurements are consistent with the reported thin silicate/silica layer at the interface of an as grown sample. Annealing experiments in the vacuum and hydrogen indicate more disordering at the interface and in the bulk of the film due to oxygen movement from the film to the interface for the growth of silica. On the other hand, annealing in oxygen show improvements in crystalline quality of both film and interface. Experiments with isotopic labeled oxygen (@super 18@O) were carried out to understand the oxygen diffusion through the film to the interface using @super 16@O and @super 18@O nuclear reactions. Film collapses in the temperature range of 1070-1120 K regardless of the heating environment. @FootnoteText@ @footnote 1@ Z. Yu, J. Ramdani, J.A. Curless, C.D. Overgaard, J.M. Finder, R. Droopad, K.W. Eisenbeiser, J.A. Hallmakrk, and W.J. Ooms, J. Vac. Sci. Technol. B 18, 2139 (2000). @footnote 2@ Work conducted at PNNL was supported by the DOE Laboratory Technology Research (LTR) Program and by Office of Biological and Environmental Research (OBER).

4:20pm **DI-TuA8 Core-level Photoemission of High-K Dielectrics on Si Substrates***, **J.E. Rowe**,* Army Research Office*; M.D. Ulrich, R.S. Johnson,* North Carolina State University*; T.E. Madey,* Rutgers University*; G. Lucovsky,* North Carolina State University

High resolution soft X-ray photoelectron spectroscopy (SXPS) with synchrotron radiation is used to study the interface of device quality ultrathin gate oxides of Al, Ta and Al-Ta alloys. Our present studies were performed on thin oxides grown plasma-enhanced CVD. After growth samples were further processed by rapid thermal annealing for 30 sec at temperatures near ~ 900ÂºC. Our photoemission measurements were performed with synchrotron radiation at the National Synchrotron Light Source (NSLS) located at Brookhaven National Laboratory using beamline U4A which has a total instrumental resolution of better than 0.1 eV. Some data were collected at lower resolution (~0.2 eV) in order to increase data collecting efficiency for better sampling depth at higher photon energies (near 200 eV). We find that our data can be well described by an ultrathin ~5 Ã… interface layer of SiO2 with a graded transition to Al and/or Ta oxides. We have studied a number of samples prepared as described above and find that the interface peak energies relative to the Si-2p peak are 0.81 eV, 1.75 eV, 2.47 eV, and 3.60 eV for the Si+1, Si+2, Si+3, and Si+4 peaks respectively. No evidence of sub-oxides were found for either Al or Ta species. The total concentration of Si-suboxide derived from SXPS data is dependent on the uniformity of the SiO2 interfacial layer as well as data modeling, i.e., fitting of the data; both will be discussed.

4:40pm **DI-TuA9 Quadrupole Mass Spectrometer Studies of a High Temperature Etch Process***, **St. Schneider**, H. Kohlstedt, R. Waser,* Forschungszentrum Juelich, Germany

High temperature etch processes are necessary to pattern Platinum successfully. In contrast to conventional, low temperature sputter driven etch processes, a chemical etch component is observed. >From the process perspective, they yield in redeposition free features (no fences) and in good control over sidewall sloping (minimization of CD loss). Furthermore those process regimes are characterized by a good process stability in terms of wafer counts and particle contamination, which is due to the dominating volatile etch products. To systematically investigate possible reactive etch process regions, we used a reactive ion etching (RIBE) tool with a filament free ICP source, that gives us control over the beam energy and the current density, and allows to use reactive gases. In this study we present the results for a chlorine chemistry with oxygen and carbonmonoxide additives. An energy dispersive quadrupole mass spectrometer is used for in-situ process monitoring. In one configuration, we are able to place the probe in the wafer position, opposite to the ion beam source. In this way it is possible to investigate the beam properties which are normally impinging on the wafer surface. In a second position we are able to lock on the wafer from the side, to monitor the etch process. Though the main focus of the study is on Platinum we also present results from selectivity studies to different hard mask materials and substrate materials.

5:00pm **DI-TuA10 Spectroscopic Ellipsometry Characterization of High-k Dielectric Thin Films***, **N.V. Nguyen**, Y.J. Cho, R.A. Richter, J.R. Ehrstein,* National Institute of Standards and Technology

Spectroscopic ellipsometry (SE) characterization of high-k gate dielectric thin films will be presented in this paper. The materials investigated include HfO2, ZrO2, TiO2, and Ta2O5 films on silicon substrates. These films are candidates to replace traditional SiO2 gate dielectrics. Unlike SiO2, the dielectric functions for these high-k films are not yet established and are strongly dependent on deposition process and conditions. Therefore, the objective of this study is to assess and validate optical models that can reasonably represent the dielectric functions of these materials. The films used in this study were fabricated by different techniques including chemical vapor deposition, jet vapor deposition, and sputtering, and were post-deposition annealed at various high temperatures. To model the SE experimental data, single and multiple Tauc-Lorentz (TL) dispersion function(s) were employed for the dielectric functions of the films. It is found that a simple single TL can generally reproduce the dielectric function below and near the absorption edge. Above the edge, a summation of two or more TL dispersions is needed to improve data fitting. For samples annealed at high temperatures, additional new optical features due to structural changes in the films were seen in their dielectric functions, which require even more than two TL dispersions to fit the data. In addition, the effect of a possible oxide layer at the interface between the substrate and the films was examined in the relation with their determined dielectric functions. We also describe and evaluate the use of other optical dispersions such as harmonic oscillator approximations for high-k thin films and compare the results with those of TL dispersion. A brief discussion for using extended spectral range into vacuum ultraviolet region to characterize these and other high-k dielectric thin films will be presented.

Dielectrics
Room 130 - Session DI-WeM
Atomic Layer Deposition for Silicon Devices

Moderator: P.S. Ho, The University of Texas at Austin

8:20am **DI-WeM1 Growth of Tantalum Oxide Films by Chemical Vapor and Atomic Layer Deposition***, **S. Prasertchoung**, S.-Y. Yang, J.N. Kidder,* University of Maryland

The nucleation and growth of tantalum oxide thin films by chemical vapor and atomic layer deposition was studied. In the CVD process, the films were deposited using Ta(C@sub 2@H@sub 5@O)@sub 5@ and O@sub 2@ as precursors, where tantalum source was delivered to the process using direct liquid injection. Films with thickness of 1 to 50 nm were deposited on Si and Pt-coated Si substrates and characterized using ellipsometry, atomic force microscopy, X-ray diffraction, and electrical measurements. In the CVD process it was observed that the deposition rate was kinetically-limited at substrate temperatures up to 475 C with an activation energy of approximately 1 eV. At temperatures greater than 475 C the growth rate decreased significantly and film properties were poor with rough morphology. This behavior was characteristic of gas phase reaction effects, although similar behavior was observed even with sequential delivery of the oxygen and tantalum ethoxide, where reactions between the precursors were minimized. This effect may stem from reactions with by-products of the alkoxide decomposition, such as water and ethanol, which can have a large effect on the nucleation and growth. In this work we investigated the effect of water on the initial nucleation, the growth kinetics, and the film morphology for ultra thin films of tantalum oxide deposited in both chemical vapor deposition and atomic layer deposition processes where the precursors (Ta(C@sub 2@H@sub 5@O)@sub 5@, O@sub 2@, H@sub 2@O) were delivered under various sequences and conditions. @FootnoteText@ This work was supported by the NSF through the University of Maryland MRSEC(DMR 00-80008).

8:40am **DI-WeM2 Quantum Chemical Study of Zirconium Oxide Atomic Layer Deposition***, **Y. Widjaja**, C.B. Musgrave,* Stanford University

As gate oxide thickness in MOS device decreases, new high-@kappa@ materials are being investigated to substitute for silicon oxide. However, unlike silicon oxide, the oxide layers being investigated do not react readily on silicon surfaces. Here, we use density functional theory to examine the atomic layer deposition of zirconium oxide, one of the high-@kappa@ materials candidates, on the Si(100)-(2x1) surface. The reactants investigated in this study are ZrCl@sub 4@ and H@sub 2@O. The atomistic mechanisms of two different deposition cycles are investigated: 1) ZrCl@sub 4@ is first deposited on the clean Si(100)-(2x1) surface. Upon adsorption, ZrCl@sub 4@ is shown to dissociate into ZrCl@sub 3@(a) and Cl(a) with an activation barrier that is below the entry level. Water is deposited next and various surface reactions and configurations are investigated. We find that the most stable species consists of ZrCl@sub 3@(a) and OH(a) attached to the two silicon atoms of silicon dimers. Alternatively, 2) H@sub 2@O is first deposited on the Si(100)-(2x1) surface. As determined previously, we also find that H@sub 2@O dissociates into OH(a) and H(a) upon adsorption. Subsequent reactions with ZrCl@sub 4@ are then investigated. Upon investigation of the two different deposition cycles, the properties of the interfacial layer between silicon and zirconium oxide are then investigated. Subsequent half cycle reactions on the zirconia surface will also be presented.

9:00am **DI-WeM3 Effect on In-situ H@sub 2@ Plasma Treatment of ZrO@sub 2@ Gate Dielectric Deposited by Plasma Enhanced Atomic Layer Deposition Method***, J.H. Koo, **Y. Kim**, H. Jeon,* Hanyang University, Korea

As the metal oxide semiconductor device continues scale down, the high-k gate dielectrics become one of the solutions in providing increased capacitance and reduced leakage currents without significantly increasing the actual equivalent oxide thickness (EOT) of gate dielectrics. Among the high-k materials, ZrO@sub 2@ is considered as one of the alternatives to SiO@sub 2@ gate dielectric due to the relatively high dielectric constant (~25), low leakage current and its compatibility with the manufacturing of integrated circuits.@footnote 1@ Here, we focus on the in-situ H@sub 2@ plasma effect on ZrO@sub 2@ gate dielectric deposited by plasma enhanced atomic layer deposition (PEALD) method. ZrO@sub 2@ were deposited on p-type Si (100) substrates at 200-300°C using t-butoxide as Zr precursor and oxygen as reactant gas at the process pressure of about 1 Torr. Initial native oxide layer was removed by in-situ hydrogen plasma treatment before ZrO@sub 2@ deposition at the same processing temperature. Oxygen reactant gas was introduced both as in gas and plasma states. About 1000Å layer of Platinum (Pt) as gate electrodes were deposited by e-beam evaporator. The electrical properties of this MOS capacitor were measured after post metal annealing. The physical and chemical characteristics of ZrO@sub 2@ film were analyzed by cross-sectional transmission electron microscope, atomic force microscope, Auger electron spectroscopy, X-ray photoelectron spectroscopy and Rutherford backscattering spectroscopy. The results of electrical properties and reliability characteristics including EOT, hysteresis, leakage current and capacitance were measured by I-V and C-V. This paper presents the plasma effect on ZrO@sub 2@ films deposited by PEALD method and its potential applications for gate dielectric in ultra large-scale integrated circuit devices. @FootnoteText@ @footnote 1@W. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon and J. C. Lee, Appl. Phys. Lett., 77, 3269-3271 (2000).

9:20am **DI-WeM4 Nucleation and Growth Chemistry during Tungsten Atomic Layer Deposition on Oxide Surfaces***, **R.K. Grubbs**,* University of Colorado, Boulder, U.S.A

The nucleation and growth chemistry during tungsten (W) atomic layer deposition (ALD) on SiO@sub 2@ and Al@sub 2@O@sub 3@ surfaces were studied using Auger electron spectroscopy and quadrupole mass spectrometry. W ALD was performed using sequential exposures of WF@sub 6@ and Si@sub 2@H@sub 6@. Differences in the nucleation process and the film growth mode were observed for the two oxide substrates. The nucleation of W ALD on SiO@sub 2@ required 8-9 WF@sub 6@/Si@sub 2@H@sub 6@ reaction cycles. A much shorter nucleation period was observed on Al@sub 2@O@sub 3@. W ALD on SiO@sub 2@ followed a Frank-Van der Merwe, layer-by-layer, growth mode while W ALD on Al@sub 2@O@sub 3@ occurred with a Volmer-Weber growth mode. These results indicate that the identity of the underlying substrate has an affect on the nucleation and growth of W ALD films. The growth chemistry of W ALD was studied using quadrupole mass spectrometry. The reaction products from each sequential reaction were identified and correlated with the Auger results. The reaction products suggest the stoichiometry of the surface reactions during tungsten atomic layer deposition.

9:40am **DI-WeM5 Atomic Layer Deposition of Al@sub 2@O@sub 3@/ZnO Nanolaminates and Alloys: Fabrication and Properties***, **J.W. Elam**, M.D. Groner, Z.A. Sechrist, S.M. George,* University of Colorado

Atomic layer deposition (ALD) of Al@sub 2@O@sub 3@ and ZnO films can be accomplished using sequential exposures to Al(CH@sub 3@)@sub 3@/H@sub 2@O and Zn(CH@sub 2@CH@sub 3@)@sub 2@/H@sub 2@O, respectively. ALD Al@sub 2@O@sub 3@ is smooth, amorphous and insulating. ALD ZnO is rough, crystalline and conducting. Composite mixtures of Al@sub 2@O@sub 3@ and ZnO may have unique and interesting properties. Al@sub 2@O@sub 3@/ZnO nanolaminates and alloys were deposited by ALD in a viscous flow reactor. The Al@sub 2@O@sub 3@/ZnO composite film growth was monitored using an in situ quartz crystal microbalance. A series of Al@sub 2@O@sub 3@/ZnO nanolaminates was prepared where the total thickness of Al@sub 2@O@sub 3@ and ZnO was kept constant while varying the number of individual Al@sub 2@O@sub 3@/ZnO bilayers. Atomic force microscopy was used to measure the root mean squared (RMS) surface roughness of the Al@sub 2@O@sub 3@/ZnO nanolaminate films. The RMS roughness of the nanolaminate films decreased dramatically versus the number of Al@sub 2@O@sub 3@/ZnO bilayers. A series of Al@sub 2@O@sub 3@/ZnO alloy films was also grown using ALD by varying the relative number of Al(CH@sub 3@)@sub 3@/H@sub 2@O and Zn(CH@sub 2@CH@sub 3@)@sub 2@/H@sub 2@O sequential exposures. Four-point probe and mercury probe measurements were performed to determine the resistivity of the Al@sub 2@O@sub 3@/ZnO alloys. The resistivity of the Al@sub 2@O@sub 3@/ZnO alloy films decreased with small Al@sub 2@O@sub 3@ percentage and then increased greatly with increasing Al@sub 2@O@sub 3@ percentage. These studies of the fabrication and properties of ALD composite films will serve as a model for the future development of ALD aluminates and silicates.

10:20am **DI-WeM7 Radical Enhanced Atomic Layer Deposition of TiN Diffusion Barriers***, **F. Greer**, D. Fraser, J.W. Coburn, D.B. Graves,* University of California, Berkeley

Atomic Layer Deposition (ALD) has been proposed as one way to deposit highly conformal thin films for copper diffusion barriers due to the self-limiting, layer-by-layer growth that can be achieved with this technology. One problem with thermally activated ALD is that the deposition temperatures that are required to achieve reasonable growth rates and good quality films with low impurity concentrations can be relatively high. This may make the integration of these barrier films with temperature-sensitive films, such as organic low-k films, impossible. One potential alternative to thermal ALD is to use more reactive species such as radicals to catalyze film deposition at lower substrate temperatures. In this work, TiN films are deposited using Radical Enhanced Atomic Layer Deposition (RE-ALD) using separate, alternating pulses of TiCl@sub 4@ and various combinations of hydrogen and/or nitrogen radicals with or without additional pulses of NH@sub 3@. By directing independent beams of each of these species at a given surface (in this case, silicon dioxide coated on Quartz Crystal Microbalances), kinetic parameters of interest such as the sticking and reaction probabilities of these species have been measured as a function of surface temperature, and will be used to predict the conformality of films deposited using RE-ALD in features of arbitrary aspect ratio. Ex-situ XPS analysis of the deposited films will be presented, paying particular attention to the low residual chlorine content that can be achieved with sufficient hydrogen radical exposure (~0.3%) at deposition temperatures as low as 100°C. In-vacuo Auger Electron Spectroscopy film composition measurements will be presented from different stages during the deposition process. Various measurements of the film quality will also be presented including the dependence of the films' resistivity and crystallinity on deposition conditions.

10:40am **DI-WeM8 Characteristics of Tungsten Nitride Atomic Layer Deposition***, **H.S. Sim,*** Korea Institute of Science and Technology*; Y.T. Kim,* Korea Institute of Science and Technology, Korea*; H. Jeon,* Hanyang University, Korea

Atomic layer deposition method for binary or ternary metal nitride film such as TiN, W-N, TaN, and TiSiN has been proposed to get a nano-scale diffusion barrier thin film. In this work, we have deposited W-N atomic layer with multiple cycles of introducing WF@sub 6@, N@sub 2@, NH@sub 3@, and N@sub 2@ gases in order. A cycle time was varied from 1 - 5 sec for an atomic layer. Deposition rate per cycle, crystal structure, and atomic lattice image for interface of W-N and Si were determined with high resolution transmission electron microscopy (HR-TEM). We have investigated atomic deposition windows at temperatures between 250 - 450 °C. As a result, deposition rate per cycle was nearly the same and the resistivity of as deposited W-N was about 100 ~ 300 µ@OHM@-cm. The diffusion barrier performance of both as-deposited and post-annealed W-N films at temperatures between 500 and 700 °C were investigated in the view points of Cu diffusion mechanisms through surface and grain boundary. As a nano scale diffusion barrier for Cu interconnect, we have investigated correlations between Cu diffusion and texture, composition change and crystalline structures of W-N atomic layer during post-annealing with medium energy ion spectrometry (MEIS) as well as HR-TEM.

11:00am **DI-WeM9 Deposition of Ultra Thin Films by Atomic layer Deposition (ALD)***, **M.A. Leskela,*** University of Helsinki, Finland **INVITED**

In ALD the precursors are pulsed to the substrate alternately one at the time and between the reactant pulses the reactor is purged with an inert gas. With a proper adjustment of the conditions the process can proceed via saturative steps. The precursors chemisorb on the surface or react with the surface groups and form a tightly bound monolayer. Under such conditions the growth is stable and the thickness increase is constant in each deposition cycle. The layer-by-layer principle facilitates the growth of ultra thin films with accurate thickness and conformality on large areas. These advantages of the ALD method are just those required in microelectronics for the manufacturing of future generation integrated circuits. In microelectronics ALD has been studied for deposition of oxide films for dielectrics, nitride films for diffusion barriers for metallizations, and metal films. Examples of those processes will be given. The key issue in a successful ALD process is the precursor chemistry. The development of new precursors is a challenge for the further progress of ALD. ALD can also be used to modify interfaces of thin film structures and surfaces of powder samples. Examples from the use of ALD in preparation of heterogeneous catalysts will be highlighted.

Dielectrics
Room 130 - Session DI-WeA
Low K Dielectrics

Moderator: Z. Yu, Motorola Labs

2:00pm **DI-WeA1 Materials Issues and Recent Development of Low k Dielectrics for Advanced Interconnects*, P.S. Ho,*** The University of Texas at Austin **INVITED**

Materials Issues and Recent Development of Low k Dielectrics for Advanced Interconnects Low k dielectrics are being developed for on-chip interconnects beyond the 0.13 micron generation. To replace silicon dioxide, there are stringent requirements on materials properties imposed on the low k dielectrics. The challenge is how to maintain the thermomechanical properties of the material while decreasing its dielectric constant, particularly for porous materials with dielectric constant less than 2. In spite of this difficulty, several materials have been developed and process integration demonstrated recently. The materials issues and characterization of low k dielectrics will be presented. Recent developments based on optimization of molecular structures will be discussed.

3:40pm **DI-WeA6 Formation of Self-Assembled Molecular Layers on the Low Dielectric Porous Methyl Silsesquioxane*, J.C. Hu,*** *C.W. Wu, L.J. Chen,* National Tsing Hua University, Taiwan, R.O.C.*; C.H. Li,* National Chiao Tung University, Taiwan, R.O.C.*; T.C. Chang,* National Sun Yat-Sen University, Taiwan, R.O.C.*; C.J. Chu,* Nanmat Technology Co., Taiwan, R.O.C.

Porous methyl silsesquioxane (PMSQ) with a low dielectric constant (~1.8) is of great interest for ULSI applications. However, many hydrophilic methyl groups (-CH@sub 3@) on the PMSQ were destroyed under O@sub 2@ plasma ashing. Hydroxyl groups (-OH) were bonded with Si dangling bonds on the PMSQ films. H@sub 2@ plasma post-treatment is usually used to decrease -OH bond formation. In the present work, bottom-up growth behavior of self-assembled molecular layers (SAMs) on the PMSQ was investigated. Diclorodimethylsilane was used to form SAMs on the PMSQ at the room temperature. Structural properties of the PMSQ films were investigated using FTIR. The absorption peaks of Si-C (781 cm@super -1@), Si-C (1273 cm@super -1@), and C-H (2975 cm@super -1@) in PMSQ samples disappeared after O@sub 2@ plasma treatment for 5 min. It indicated that the majority of methyl groups in the films were removed and Si dangling bonds were exposed. The Si-O cage-like structures in the PMSQ films also decreased due to its loose structure arrangement. As a result, the low dielectric characteristic of PMSQ would be damaged. On the other hand, the absorption peaks of Si-C and C-H were present for the PMSQ films dipped in diclorodimethylsilane solution with and without ultrasonic system. The purpose of using ultrasonic system was to accelerate formation rate of SAMs on the PMSQ. The results revealed that the hydrophobic dimethylsilane groups have been formed on the surface of PMSQ. The Si-OH bonds on the PMSQ changed to Si-O-Si(CH@sub 3@)@sub 2@. The thickness of SAMs was less than 1.0 nm. The -CH@sub 3@ groups of SAMs on the Si-O network surface of the PMSQ films were apparently of ordered array structure owing to minimal steric hindrance arrangement.

4:00pm **DI-WeA7 Temperature-dependent Current Transport in Low-k Inorganic Polymer Dielectrics*, J.W. Tringe,*** *R.A.B. Devine,* U.S. Air Force Research Laboratory

Low-k dielectrics are an increasingly important class of materials for high-performance integrated circuits, promising to significantly increase processing speeds by lowering resistance-capacitance delays in global interconnects. However, since these new dielectrics are anticipated to cover large areas of the chip they also represent a potential reliability risk. It is therefore important to understand how charge transport occurs in the low-k films over a range of temperatures in order to avoid breakdown or excess leakage current during circuit operation. Low-k dielectric films based on inorganic polymers such as FOx flowable oxide from Dow Corning have been examined. Spun-on films, 3000 Å thick, were patterned into metal-insulator-semiconductor capacitor structures, then probed to measure current and capacitance as a function of voltage. Temperature-dependent current-voltage measurements, over the range 26 to 150 °C, show that current conduction is predominately via either Schottky or Frenkel-Poole emission. A field-independent thermally activated barrier height of approximately 0.1-0.2 eV is deduced. The measured exponential term proportional to the square root of the electric field in the current-voltage dependence is smaller than expected for Frenkel-Poole emission, however. Additionally, the temperature and field dependences of the exponential prefactor do not enable us to clearly distinguish between Schottky or Frenkel-Poole emission over the experimental temperature range.

4:20pm **DI-WeA8 Characterization of SiC Films for Cu/low-k Integration*, F.G. Celii*,** *T. Tsui, R. Willecke, J. Large,* Texas Instruments, Inc.

Silicon carbide (SiC) is being evaluated for integration into Cu/low-k backend process flows. Potential applications include use as a patterning hardmask and as an etch stop layer with Cu diffusion properties. This paper reports the physical and optical characterization of SiC films. Films were deposited on 200 mm wafers in a commercial reactor using plasma-enhanced chemical vapor deposition (PE-CVD). Film composition and bonding were elucidated using SIMS, XPS and FT-IR spectroscopies. Optical properties of the films were determined from variable-angle spectroscopic ellipsometry into the vacuum ultraviolet region (~140 nm). Under some processing conditions, we observed ellipsometry data consistent with a vertical gradient in the SiC refractive indices. The optical constants of the film, along with reflectance modeling using Prolith, suggest SiC can be used as an anti-reflection coating (ARC) layer for lithographic patterning at either 248 or 193 nm. To test the optical modeling results, we have prepared various film stacks containing SiC and organosilicate glass (OSG) on Si or Cu. The reflectivity vs. wavelength will be measured and compared with the calculated reflectivity values. Initial patterning results will also be presented.

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