Manufacturing Science and Technology
Room 304 - Session MS-MoM

Metrology for IC Manufacturing

Moderator: G.W. Rubloff, University of Maryland

8:20am **MS-MoM1 Inline Quality Analysis in MBE Manufacturing of AlGaAs/InGaAs pHEMT Structure Using Photoreflectance and Contactless Electromodulation Spectroscopy**, ***G. Zhou***, *W. Liu, M. Lin,* Alpha Industries, Inc.

Molecular beam epitaxy (MBE) has become a predominate technology in the manufacturing of pseudomorphic high electron mobility transistors (pHEMTs) for microwave power amplifiers and switchers. In order to keep ahead of the performance and cost curves, nondestructive inline metrologies which leverage the yield learning curve of the fabricator are required. We report the study of implementation of photoreflectance (PR) and contactless electromodulation spectroscopy (CER) as inline quality monitoring tools for AlGaAs/InGaAs pHEMTs manufacturing. Using the reduced mass deduced from experiments, the built-in electric field, the band-gap and/or Al composition in the barrier region is obtained from the above band-gap Franz-Keldysh oscillations (FKO). Two dimensional electron gas (2DEG) density can also be determined by the line shape fitting of the transitions from InGaAs region, and the statistical data both from PR/CER and Hall measurements on a number of wafers are compared. The quality of the device structure and 2DEG density confined within the InGaAs quantum well are found to have a direct relationship both to the intensity of PR/CER transitions from AlGaAs/GaAs superlattice and the built-in electric field in the AlGaAs barrier layer. This observation reveals the possibility to use PR/CER as a screening technique.

8:40am **MS-MoM2 Three Dimensional Reconstruction Metrology by Combinatory Multiple Parameter Characterization and Scanning Probe Microscopy**, ***E.C. Houge***, Lucent Technologies and University of Central Florida; *J.M. McIntosh, J.E. Griffith,* Bell Laboratories; *L.A. Giannuzzi,* University of Central Florida; *J.B. Bindell,* Lucent Technologies

Critical dimension metrology of integrated circuits has historically constituted only single parameter characterization of SEM intensity line profiles, which was intended to be representative of the overall linewidth. Due to the surjective nature of the intensity line profile, different morphological patterns can be represented by a single parameter thus causing the inability to delineate deviant morphologies. As the linewidths continue to decrease smaller variations begin to have significant impact in the overall morphology of the linewidth and the pattern transfer function. Three dimensional reconstruction metrology leverages the advantageous of two next generation inline metrology techniques, multiple parameter characterization and scanning probe microscopy, to create a new methodology of metrology. Multiple parameter characterization of scanning electron microscope intensity line profiles initially has shown promise of being able to distinguish deviations from nominal profiles in the characterization and evaluation against preset process margin templates stored in memory. Inline scanning probe microscopy presents the ability to do morphological shape evaluation by nondestructive cross sectioning of critical dimension features obtaining topographic z(x,y) mapping as a function of planar positioning of the scan system. Through the use of these two techniques along with transform reconstruction, a three dimensional topography of the sample surface can be reconstructed utilizing only two dimensional intensity and topographic mapping of the sample surface. Single parameter characterization is then replaced by the determination of Scale (nm), Shape Quality (A weighted polynomial of process margin template deviation, 0-1), and Deviation Bin (A descriptor for type of deviation, A-Z). This segregation of shape and scale along with the full characterization of the feature morphology presents the possibility for the feedback and feedforward use of metrology.

9:00am **MS-MoM3 Application of Scanning Capacitance Microscopy to the Characterization of Semiconductor Device Operation**, ***C.Y. Nakakura***, *D.L. Hetherington, M.R. Shaneyfelt, P.E. Dodd,* Sandia National Laboratories

Scanning capacitance microscopy (SCM) has become increasingly used for the study of semiconductor doping due to its ability to measure two-dimensional free carrier profiles with nanometer-scale resolution. The bulk of recent SCM work has focussed on carrier profile measurements in cross-sectioned, metal-oxide-semiconductor field-effect transistors (MOSFETs); however, limitations in the hardware and sample structures have restricted most studies to non-functioning devices. To address this, we have modified a commercial SCM and fabricated specially designed test structures that provide independent electrical access to the device regions, enabling the use of SCM to study actively biased devices. By recording images while incrementally increasing the gate bias voltage, we were able to visualize devices switching between the off and on states. The evolution of the SCM images as a function of operating bias provides insight into changes in the channel region during MOS device operation and will be presented in movie form. Complications in image formation, which arise from biasing the device, will be discussed. @FootnoteText@ This work was performed at and supported by Sandia National Laboratories under DOE contract DE-AC04-94AL85000. Sandia National Laboratories is a multi-program laboratory operated by Sandia Corporation for the United States Department of Energy.

9:20am **MS-MoM4 Metrology with Electron Beams - The Current State and Future Directions**, ***D.C. Joy***, University of Tennessee and Oak Ridge National Laboratory **INVITED**

Electron beam tools have become the instruments of choice for CD metrology, as well as for defect detection and analysis, because of the many benefits that they offer. As a result of intensive development work the performance of CD-SEMs and related tools has kept pace with the rapid decrease in feature size and the demands for increased throughput. However with the imminent advent of 100nm design rules in 2003 and the requirement for measurement precisions as low as 1nm and the need to detect defects as small as 10nm, it is clear that this situation is changing because the scope for further enhancements in microscope performance is now small. For example, at low beam energies the SEM is now operating at close to the minimum probe diameter set by diffraction, and the physics of electron-solid interactions and of secondary electron generation set a limit to resolution which may be as poor as 3 to 5nm in materials such as resists. Although some incremental improvements can be anticipated, through new technologies such as aberration corrected lenses, and new ultra-bright electron emitters, these advances will not be sufficient to bring the instruments to the levels required for sub-100nm devices and they will certainly not be sufficient to ensure a continued development path to even smaller structure, and the new molecular devices envisioned beyond the end of the road map. Some radical new solutions must therefore be examined. This talk will therefore examine several possible solutions including the use of high beam energies. the replacement of imaging by holographic techniques, the use of energy filtered imaging methods, and the use of point projection microscopes.

10:00am **MS-MoM6 Limitations of SIMS Depth Profiling for Shallow Implant and Thin Gate Dielectric Metrology**, ***M.G. Dowsett***, University of Warwick, UK **INVITED**

SIMS depth profiling is now expected to extract accurate quantitative data from the top 10 nm of a wafer under circumstances where a significant part of the measurement may be in the top 3 nm, and where the total impurity level in the material may be above 1%. The reality is that, however reproducible the data, accurate profiles can only in general be obtained for impurity levels below 1% and in the depth range 3-10 nm by very careful selection of the analytical conditions. For high dose, ultra-shallow, implants using molecular ions such as BF@sub 2@ (where the total impurity level may be as high as 30%) or for thin (1-5 nm thick) dielectric layers the inherent nonlinearity of both sputtering and ion emission, combined with the fact that the region of interest overlaps with the transient region leads to very strong matrix effects for which no correction procedure has yet been devised (indeed, depending on the level of non-linearity, no correction procedure may be possible). Given that there is an insatiable demand for profiles from the problem region outlined above, how can one obtain accurate profiles, or at least establish the level of error in, say, the dose, junction depth, or internal profile from a 2 nm thick oxynitride layer? The general answer is to examine profiles obtained under different analytical conditions and from different analytical techniques to see if the data converge on a dose or even a shape, to measure changes in erosion rate in the transient region using techniques other than SIMS (e.g. MEIS), and to compare directly profiled data with data where the transient has been removed from the problem by capping the wafer. In addition, measurements should be made under the most linear conditions possible so that reasonable correction procedures can be devised. Of course, suitable reference materials are required, in order to establish such conditions. Techniques for accurate profiling of the top few nm of a wafer still require research and further development of the tools before claims to a reproducible dose and junction depth can be translated into a known accuracy in profile shape, dose and junction depth.

Manufacturing Science and Technology
Room 304 - Session MS-MoA

Challenges in Semiconductor Manufacturing for the First Decade of the 21st Century

Moderator: C.R. Brundle, Applied Materials

2:00pm **MS-MoA1 Chips to Power the Peta-bit Network**, ***D. Eaglesham***[1], Lucent **INVITED**

The net continues to grow at a mind-boggling rate. 1999 was the first year that data traffic exceeded voice. Data traffic in North America continues to double every 6 months. This explosive growth is driven an apparently insatiable demand for bandwidth and continuing improvements in the underlying technology. Electronic switches are rapidly moving up the speed scale from Gb/s to 40 Gb/s, while wavelength multiplexing of these signals drives the capacity of a single fibre up from 10Gb/s, with experimental demonstrations in the multi-Terabit/s range. Bandwidth on a single fibre is likely to top out a little short of a Petabit/s within a few years. The basic technology for data manipulation remains the silicon switch. Transistor scaling has been responsible for much of our ability to move huge chunks of data. I will discuss the level of scaling required in the Pb/day era, and the new transistor structures required to overcome the key technical challenges facing CMOS scaling. I will also discuss the new technologies arising to deliver low-cost highly-integrated networking chips, in particular SiGe BiCMOS technologies. Finally, I will describe an assortment of new technologies including MEMS, and integrated waveguides and modulators, that are starting to change the very core of the network.

2:40pm **MS-MoA3 SOI or USJ?: Laminated Electronics for "Post-Roadmap" CMOS**, ***M.I. Current***, *S.W. Bedell, I.J. Malik, F.J. Henley,* Silicon Genesis **INVITED**

The many challenges that are projected in the ITRS99 study for fabrication of high-performance planar CMOS transistors on bulk Si for gate dimensions smaller than 60-50 nm (expected in year 2006-2008) clearly point to major changes in standard transistor design, materials and fabrication techniques. Various forms of laminated electronic substrates, beginning with Silicon-on-Insulator (SOI), provide a means to relax some of the process and materials constraints on bulk Si devices. SOI substrates also provide new design options, such as dual-gated channels and high-mobility buried channels. New technologies are now available to bond and cleave electronic materials layers with atomic layer control and surface roughness approaching 1 Å (RMS) without the need for CMP or other damage removal and polishing processes. The design and fabrication of complex laminated electronics "master slice" substrates, which can provide for integrated fabrication of opto-electronic circuits, will be illustrated with examples for such components as dual-gate CMOS, compliant substrates for III-V film growth and optical switching and coupling pathways.

3:20pm **MS-MoA5 The Viability of sub-50nm CMOS Technology**, ***G. Timp***, *J. Bude, F. Baumann, D. Muller, Y. Kim, M.L. Green, T. Sorsch, D.M. Tennant, R. Kleiman,* Bell Laboratories, Lucent Technologies*; W. Timp,* Massachusetts Institute of Technology*; P. Silverman, B.E. Weir,* Bell Laboratories, Lucent Technologies **INVITED**

The complexity of an integrated circuit (IC), measured by the number of transistors incorporated into the circuit, is constrained by power dissipation. The viability of sub-50nm CMOS technology, which promises to incorporated nearly a billion MOS transistors into one circuit, is contingent upon the drive current performance of the MOSFET as well as the off-state leakage current. We are obliged to pursue improvements in the drive performance to derate the power supply voltage, thereby reducing power dissipation while improving reliability. The drive current of a MOSFET is dictated by both the thickness of the SiO@sub 2@ gate dielectric and by carrier scattering in the channel. Reducing the thickness of the gate oxide increases the drive current by increasing the carrier density in the channel through an increase in the gate capacitance. However, the gate leakage current due to direct, quantum mechanical tunneling through the oxide renders SiO@sub 2@ thickness' less than 1.3nm impractical because the off-state leakage current becomes intoleralbe.@footnote 1@ Consequently, the drive performance for t@sub ox@>1.3nm is limited by ballistic transport in the channel. We have shown that ballistic transport (with transmittance T>0.80) can be achieved at room temperature in a silicon MOSFET operating with transverse electric fields at the inversion layer in the semiconductor >1MV/cm, provided that the deleterious effect of interface roughness scattering is mitigated by optimizing the transverse field and minimizing the channel length and interface roughness. This optimum illustrates the futility of alternative, high @kappa@ gate dielectrics that give rise to a channel mobility less than that found at the equivalent SiO@sub 2@ thickness or operate at higher transverse fields, and indicates that a more sophisticated design of the source, drain and channel doping profiles will be required to satisfy the drive specifications. @FootnoteText@ @footnote 1@ D. Muller et al., Nature, 399 (1999) 758.

4:00pm **MS-MoA7 Technology for Wired and Wireless Networks**, ***S. Subbanna***, *B. Meyerson,* IBM Microelectronics **INVITED**

In the first decade of this century, we can expect to see extraordinary growth in the availability of information bandwidth. Telecommunications providers and/or service providers will be expanding their capacity to provide increasing numbers and types of services at an ever cheaper rate. This will drive demand for high-speed wired and wireless ICs, and for the seamless connection of both. This talk will focus on the silicon-based process technology, packaging, and design infrastructure requirements for rapid development and supply of cost-effective solutions. In particular the manufacturing advantages of using a silicon (CMOS) base for this technology will be expounded. One technology that unites the cost-effective CMOS base with a high-performance RF NPN bipolar transistor is Silicon-germanium (SiGe) BICMOS. SiGe BICMOS has been used to combine many different RF and digital functions on a single chip. The drive for RF system-on-a-chip is great due to requirements of power, space, and weight reduction for cellular phones. We will discuss design of the SiGe BICMOS technology for manufacturability, as well as issues associated with bringing our 0.5, 0.25, and 0.18um technologies to production. The issues associated with use of CMOS technologies for RF applications will also be discussed, as well as tooling implications and requirements (which are slightly different than CMOS). The issues associated with simulation of (semiconductor) processes and device performance for SiGe BICMOS will also be discussed. We will also discuss challenges for improvement of yield and manufacturability of these technologies. We will also review the limits on silicon technology performance in the light of these new developments.

4:40pm **MS-MoA9 Process Integration Challenges in a Copper/Low-K World**, ***R.A. Powell***, Novellus Systems **INVITED**

It is generally agreed that the wiring of GigaHertz-class ICs will be a multilevel interconnect stack of Cu lines electrically insulated from each other by low-k interlevel dielectrics and assembled using a Damascene process flow. Significant progress has already been made on unit processes needed for 0.10-0.13 µm technology, including deposition of conformal barrier/seed layers by ionized PVD or CVD, bottom-up filling of vias and trenches using additive-enhanced Cu electroplating, and deposition and patterning of CVD and spin-on dielectrics having dielectric constant in the range $2 < k < 3$. On the other hand, integrating these unit processes together without losing the intrinsic material benefits of Cu and low-k dielectrics is a major challenge and requires a balance between performance, reliability and cost. The present talk illustrates how the distinctive physical and chemical properties of Cu and low-k dielectrics are influencing integration schemes as well as presenting new opportunities for process equipment and metrology suppliers. Examples will include issues of wafer-scale and micro-scale Cu contamination; the impact of water vapor exposure and degassing on low-k dielectric performance and film adhesion; and the development of reactive pre-cleaning and annealing methods to deal with the non-passivating nature of the Cu surface.

[1] **Featured Speaker - Science and Technology in the 21st Century**

Incorporating Principles of Industrial Ecology
Room 304 - Session IE-TuA

Green Manufacturing

Moderator: P.M. Beauchamp, Jet Propulsion Laboratory

2:00pm **IE-TuA1 Challenges in Bringing Green Manufacturing Technologies to the Clean Room Floor**, ***S. Raoux,*** Applied Materials **INVITED**

The semiconductor industry is undertaking major research and development efforts to reduce the environmental impact of its manufacturing processes. In particular, technologies have been introduced to eliminate atmospheric emissions of global warming compounds, reduce solid waste and conserve energy and water resources. At each technology node, semiconductor fabrication processes are amenable to change, and implementation of sustainable manufacturing practices should be favored. However, the stringent requirements of the semiconductor fabrication process render the introduction of novel manufacturing techniques a challenge. In this talk, we present innovative concepts that have been developed and integrated within semiconductor fabrication tools. Emphasis is placed on point-of-use (POU) solutions and environmental engineering using plasma technologies. We review the requirements that must be met by green technologies to be integrated to a complex manufacturing environment. We also present arguments to demonstrate that environmentally benign manufacturing methods can be developed and implemented in an economically viable way.

2:40pm **IE-TuA3 Eliminating Perfluorocompound Gas Emissions from CVD Chamber Cleans**, ***P.J. Maroulis,*** *A.D. Johnson, W.R. Entley,* Air Products and Chemicals, Inc. **INVITED**

Perfluorocompond (PFC) gases such as CF4, C2F6, and NF3 are used extensively in semiconductor manufacturing processes. The largest volume use for these gases is for chamber cleaning following chemical vapor deposition (CVD). PFCs have long atmospheric lifetimes and absorb strongly in the infrared region of the electromagnetic spectrum where the earth's atmosphere would otherwise be transparent. Because of their infrared absorbances and persistence, PFCs are suspected of contributing to global warming. Through the World Semiconductor Council (WSC) the global semiconductor industry has voluntarily committed to reduce its cumulative emissions of perfluorocompounds. For the U.S., Europe, and Japan, PFC emissions will be reduced to 90% of 1995 levels by 2010 with some companies announcing even more aggressive reduction targets. Based on industry growth projections, substantial reductions for individual processes will be necessary to achieve these targeted levels. Both process optimization of traditional C2F6 based in situ cleans and substitution of NF3 for C2F6 in situ cleans are effective strategies for reducing the environmental impact of installed CVD tools. For new CVD tools, the manufacturers of semiconductor process equipment have developed and introduced a new remote NF3 cleaning technology that essentially eliminates PFC emissions. The combination of these three strategies, optimization of traditional C2F6 based in situ cleans, the substitution of NF3 for C2F6 in in situ cleans, and the implementation of the remote clean technology, has effectively solved the semiconductor industry's PFC issue. This presentation will contain data demonstrating the effectiveness of these strategies. In essentially all cases, perfluorocompounds emissions have been reduced by 50% to >99%.

3:20pm **IE-TuA5 Meeting IBM's PFC Emission Goals: Using the IBM In Situ Dilute NF@sub 3@/He Plasma Clean in Production on the Applied Materials 200 mm P5000 Lamp-Heated CVD Toolset**, ***C.M. Hines,*** IBM Microelectronics*; W.R. Entley, R.V. Pearce, A.D. Johnson,* Air Products and Chemicals, Inc.

The major use of perfluorocompounds (PFCs) in semiconductor manufacturing is for residue removal following thin film deposition in chemical vapor deposition (CVD) chambers. One promising strategy to reduce PFC emissions in CVD chambers is the use of alternative clean gases that have lower global warming potentials and inherently higher utilization efficiencies (the percentage of the PFC that is consumed during the clean process) than the traditionally used carbon based PFCs, CF@sub 4@ and C@sub 2@F@sub 6@. Using this strategy, IBM developed a one-step in situ dilute nitrogen trifluoride/helium (NF@sub 3@/He) clean to replace the process of record (POR) C@sub 2@F@sub 6@-based cleans used in their Applied Materials (AMAT) 200mm Precision 5000 lamp-heated (DxL) CVD chambers. Successful implementation of the dilute NF@sub 3@/He clean into production is considered key to IBM meeting its PFC reduction goals. Using quadrupole mass spectrometry (QMS) and Fourier transform infrared (FTIR) spectroscopy the process emissions of IBM's POR C@sub 2@F@sub 6@-based cleans and the new one-step dilute NF@sub 3@/He clean following deposition of both phosphosilicate glass (PSG) and tetraethylorthosilicate (TEOS) oxide were quantified. For TEOS oxide deposition the one-step dilute NF@sub 3@/He clean reduced the MMTCE value of the clean by 99 % with respect to the POR C@sub 2@F@sub 6@ clean. For PSG deposition, the one-step dilute NF@sub 3@/He clean reduced the MMTCE value of the POR clean by 96 %. In addition, the one-step dilute NF@sub 3@/He clean significantly reduced the total combined volumetric emissions of F@sub 2@ and HF compared to the POR C@sub 2@F@sub 6@ cleans. This presentation will include an overview of the implementation of the NF@sub 3@/He clean, current production data including tool performance (particles, mean time between wetstrips, etc.), and clean time/emissions comparisons between the POR C@sub 2@F@sub 6@ cleans and the one-step NF@sub 3@/He clean.

3:40pm **IE-TuA6 Treatment of Wastes from Chemical Mechanical Polishing Operations**, ***S. Raghavan,*** *Y. Sun, J. Baygents,* University of Arizona **INVITED**

Chemical mechanical planarization (CMP) of dielectrics and metals has emerged as one of the most important techniques used in the fabrication of integrated circuits. In this technique, dielectric and metal films are globally and locally planarized using particulate slurries made from submicron-sized alumina and silica particles. A multi platen CMP tool can typically process 40 wafers per hour at a slurry consumption of approximately 100 ml/min/wafer. The aforementioned tool, if integrated with a cleaner, will require two to three gallons per minute of DI water. The mixing of CMP waste with the post-CMP cleaning waste typically results in a waste stream that is a very dilute dispersion of solids containing approximately 500 to 5000 ppm solids. In the case of metal CMP, the waste is likely to contain metal ions, unreacted oxidant such as hydrogen peroxide, residual corrosion inhibitors and other additives that are present in the slurry. Wastes from copper CMP may contain anywhere between 10 and 40 ppm of dissolved copper, in the uncomplexed and complexed form. By the year 2002, chemical mechanical planarization processes are expected to account for thirty percent of water consumed in a fabrication facility. Because of this statistics, increasing pressure is put upon fabrication facilities to treat the CMP wastes and recycle the water. Additionally, environmental regulations at the local and national level demand that solids and copper ions be removed before disposal of the water to publicly owned treatment facilities. In this presentation, an overview of the CMP waste problem will be provided and various techniques available for the treatment of CMP wastes will be critically reviewed.

4:20pm **IE-TuA8 Advanced Chemicals for Semiconductor Processing**, ***E.R. Sparks,*** *W. Wojtczak, S.A. Fine,* ATMI **INVITED**

Three of the challenges to semiconductor processing are shrinking dimensions, copper metallization, and low-k dielectric materials. These challenges have been successfully addressed with a new group of water-based chemicals that fortuitously have very favorable properties. - As lithographic dimensions shrink, etching and other processing parameters become more stringent. The residues created from photoresist during these proceses often incorporate fluorocarbon residues, and silicon and metal oxides that are impossible to remove with traditional chemicals. - New processes using copper damascene metallization have additional constraints, as many traditional chemicals are not benign to copper. - Higher speed devices are attainable with low-k dielectric materials, but these materials have special chemical requirements. Advances have been made to meet all three of these requirements by formulating chemical mixtures that are more benign, both environmentally and regarding health issues, than previously possible. These blends are water-based, water-rinsable, and free of regulated solvents, i.e., "green". The resulting technology has a very favorable cost of ownership due to lower costs related to abatement and disposal, compared to more traditional solvent blends.

5:00pm **IE-TuA10 High Throughput Process for Photoresist Stripping and Residual Polymer Removal in a Via Post-Etch Process**, ***M. Boumerzoug,*** *Q. Geng, H. Xu,* Ulvac Technologies Inc.*; S. Gu,* LSI Logic Corporation*; S. Goh,* Silterra (M) Sdn. Bhd.*; T. Meyer, J. Seaton,* LSI Logic Corporation

In fabricating advanced IC, a multi-level interconnect scheme is commonly used and plasma etch is applied to form metal lines and via holes. During the plasma etch, a sidewall polymer is formed to control the etch profile. After the etch, the sidewall polymer needs to be removed completely to

insure a good via contact resistance. Typically, a very aggressive amine based chemical solvent is needed to clean up the sidewall polymer. As the design rule shrinks and aggressive zero overplot of the metal line and via plug is used to minimize the die size, some degree of misalignment between via plug and metal lines is inevitable. Wet chemical based post etch cleaning starts to show problems for the misaligned via and metal because they may attack exposed Ti, W and Al. An advanced dry clean process has been developed for removing post etch polymer. In addition, the dry clean process offers a lower cost of ownership (COO) than the wet clean process and is much safer and environmentally friendly. This technology utilizes the combination of microwave downstream and non-damage ion assisted processes to strip chemically altered and damaged photoresist and clean residue according to the chemical composition of each layer. The ion-assisted process is also found useful in stripping the photoresist at high rate. After this dry process, no wet strippers are needed; thus, the high cost and environment and safety concern associated with chemicals can be eliminated. In some cases, this dry clean process becomes an enabling technology for avoiding Ti and W-plug attack occurring in the wet cleaning processes. Split lots of wafers, which have two layer metal, were processed by the all-dry processes and tested electrically. The via chain resistance, metal bridging yield, metal continuity and electrical CD are all equal or better than the control wafers which were processed by wet chemicals.

Dielectrics
Room 312 - Session DI+EL+MS-WeM

Low K Dielectrics
Moderator: J.A. Kelber, University of North Texas

8:20am **DI+EL+MS-WeM1 Ultra Low k Mesoporous Silica Dielectrics for Semiconductor Interconnects**, ***S. Baskaran***, *J. Liu, X. Li, C. Coyle, J. Birnbaum, G.C. Dunham, G.E. Fryxell,* Pacific Northwest National Laboratory*; C. Jin,* International SEMATECH **INVITED**

The semiconductor industry is currently targeting new intermetal dielectric (IMD) films with dielectric constants (k) less than 2.5 for interconnect applications in the 100 nm technology node, and films with k less than 2.0 for the 70 nm technology node. To meet extreme low k needs for advanced on-chip interconnects, films with incorporated porosity will most certainly be required. Porous dielectric films with k values less than 2.2 ("ultra low k") are not easily synthesized using conventional vacuum based technology such as chemical vapor deposition. A simple approach to nanoporous dielectric films involves spin-on deposition of formulations consisting of silicate, polymeric, or hybrid organosilicate precursors with thermally degradable pore-formers. Ultra low k mesoporous silica films have been synthesized with molecularly templated porosity using this approach. Molecularly organized nanostructured aggregates between 2 and 10 nm in size can function as templates for pore formation in spin coated sol-gel silicate films. The use of a structurally organized template during synthesis results in a uni-modal pore size distribution in the final film. In this paper, we present information on precursor chemistry for designing mesoscale porosity, pore architecture and surface chemistry, and the critical dielectric and mechanical properties for mesoporous silica films. Using formulations developed at PNNL, mesoporous films have also been prepared at SEMATECH on production-size wafers, and evaluated. Copper single-damascene one-level test structures were built using mesoporous silica as the intermetal dielectric. No major structural failures were observed after chemical mechanical planarization on both blanket films and patterned wafers, indicating relatively good mechanical integrity for a highly porous structure. With controlled film synthesis and dehydroxylation conditions, mesoporous silica films with k@super 2@ 2.0 and elastic modulus of 4.0 GPa have been synthesized at PNNL. The results of the one-level metal screening tests at SEMATECH combined with properties obtained at PNNL indicate that mesoporous molecularly-templated silicate films hold promise as ultra low k intermetal dielectrics.

9:00am **DI+EL+MS-WeM3 Deposition of Thermal Stable Amorphous Carbon Nitride Thin Films with Low Dielectric Constant by ECR-CVD**, *X.W. Liu,* National Tsing Hua University, Taiwan, ROC, Taiwan,ROC*; J.H. Lin,* National Tsing Hua University, Taiwan, ROC*;* ***H.C. Shih****,* National Tsing Hua University, Taiwan, ROC, Taiwan,ROC

Amorphous carbon nitride thin films with low dielectric constants and high thermal stability were synthesized on silicon by using an electron cyclotron resonance chemical vapor deposition (ECR-CVD) system in which a rf bias was applied to the silicon substrate and a mixture of C@sub 2@H@sub 2@, N@sub 2@ and Ar was used as precursors. The dielectric constants of our amorphous carbon nitride thin films were found as low as 2.4 at 1 MHz. The thermal stability of the films has been improved by the incorporation of nitrogen to the carbon film. The basic structure, composition and electronic properties of these films were analyzed by Fourier transformation infrared (FTIR) spectroscopy, Raman spectroscopy, X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and field emission scanning electron microscopy (FE-SEM) and dielectric constant measurements.

9:20am **DI+EL+MS-WeM4 Impact of Hydrogen Addition on the Deposition Rate of SiOF Films Prepared by High Density Plasma CVD**, *Y.W. Teh,* Nanyang Technological University, Singapore*; T.C. Ang,* Chartered Semiconductor Manufacturing, Singapore*;* ***K.S. Wong****,* Nanyang Technological University, Singapore*; K.H. See, S.Y. Loong, Y.C. Wong,* Chartered Semiconductor Manufacturing, Singapore

Fluorinated Silicon Dioxide film (SiOF) has been considered as the more successful first generation interlevel low-k dielectric material. However, the impact of hydrogen addition on SiOF film properties are not extensively studied. In this paper, we present a spectroscopic study of the chemical bonding in SiOF film grown with silane gas added to the standard precursors using the techniques of ellipsometry and infrared (IR) absorption spectroscopy. These SiOF films have been prepared by high density plasma (HDP) chemical vapor deposition at substrate temperature at about 420°C. Addition of hydrogen through silane gas feed is found to control deposition rate and the fluorine doping concentration of the SiOF films. The addition of SiH4 does not lead to the incorporation of hydrogen in detectable quantities in the SiOF films. This phenomenon may be attributed to the strong mutual attraction between hydrogen and fluorine radicals in the HDP. The decrease of refraction index at 632.8nm and the frequency decrease of the dominant IR active bond-stretching vibration at ~1085cm@super -@@super 1@ were found to be approximately linear with increase in fluorine concentrations. The silane added to the process gas mixture has been found to play an active role in the SiOF film formation process both in the surface reactions and the chemical bonding properties. Our results show that with an optimized silane flow rate, the film stability of the SiOF towards moisture attack is significantly improved. In addition, a high deposition rate can be achieved together with comparable fluorine incorporation in the film as compared to the standard non-silane precursors.

9:40am **DI+EL+MS-WeM5 Solid-state Nuclear Magnetic Resonance of Low Dielectric Constant Si:O:C:H Films**, ***P.-Y. Mabboux****, K.K. Gleason,* Massachusetts Institute of Technology

Adding organic content to SiO@sub 2@ is an evolutionary pathway to low dielectric films with k @<=@ 3.0. Alternate names for these materials include carbon-doped oxides, organosilicate glasses (OSG), and Si:O:C:H films. Both spin-coating and chemical vapor deposition (CVD) processes have been developed for this class of low-k films. Fourier transform infrared spectroscopy (FTIR) and x-ray photoelectron spectroscopy (XPS) have only a limited ability to distinguish variations in Si:O:C:H film chemistry. In this work, solid-state nuclear magnetic resonance (NMR) is shown to have sufficient sensitivity to determine the network structure of low dielectric constant Si:O:C:H films. Characterization of Si:O:C:H films by @super 1@H, @super 13@C, and @super 29@Si magic-angle spinning NMR will be demonstrated. Because of its wide range of chemical shifts, @super 29@Si NMR is particularly useful to elucidate new details regarding the composition and structure of these low dielectric constant films. Up to ten different environments can be resolved in some of the films. Many of the observed chemical bonding configurations have been previously observed in bulk organosilicate glasses. The NMR results can be expressed in terms of a connectivity number, which is simply the average number of bonds between network forming atoms. The connectivity number may provide a means to correlate with the mechanical properties. Fundamental understanding of structure-property-processing relationships will facilitate the engineering of the molecular architecture required for successful integration of Si:O:C:H dielectric films.

10:00am **DI+EL+MS-WeM6 A New Simple and Accurate Method to Measure Intra-Metal Capacitance of Low-K Fluorinated Silicon Dioxide**, *K.S. Wong,* ***Y.W. Teh****,* Nanyang Technological University, Singapore*; T.C. Ang, S.Y. Loong, W.B. Loh, Y.C. Wong,* Chartered Semiconductor Manufacturing, Singapore

An accurate and simple technique for intra-metal capacitance measurement is presented. This on-chip technique is based on a test structure design that utilizes only interdigitated capacitors sandwiched between metal plates. Compared to other techniques which utilize transistors in addition to the unknown interconnect capacitance to be characterized, this new technique requires only capacitors and thus much simpler processing and shorter cycle times but with the same level of accuracy. With this test structure design, no reference capacitor is needed. Capacitance voltage (C-V) method is commonly used for intra-metal capacitance measurement. However, the measurement accuracy is often compromised by probe-induced stray capacitance. In this paper, a new measurement technique that can eliminate this stray capacitance is reported. This new technique uses multiple probe configurations to obtain 3 capacitance values and these values can be used to eliminate the probe-induced stray capacitance and obtain the actual intra-metal capacitance. Results show much better accuracy than the conventional C-V measurement. Comparisons between the new technique, the conventional C-V measurement and the Charge-Base Capacitance Measurement (CBCM) techniques are made. Our results based on the new technique show great improvement in the measurement accuracy over the conventional technique. In addition, our results are consistent with the results obtained from the CBCM technique which requires the use of transistors and thus more complex processing and longer cycle times. In this paper, the different measurement techniques were evaluated on high-density plasma chemical vapor deposition (HDP-CVD) fluorinated silicon dioxide (SiOF) inter-level dielectric (IMD) films in 0.18um technology.

10:20am **DI+EL+MS-WeM7 DC and RF Characteristics of Advanced MIM Capacitors for MMIC's Using Thin and Low Temperature PECVD Si@sub 3@N@sub 4@ Dielectric Layers**, ***C.R. LIM***, *J.H. LEE, S.W. Paek, K.W. Chung,* LG-ELITE, Republic of Korea

In this work, we show the excellent DC and RF characteristics of MIM (metal-insulator-metal) of PECVD Si@sub 3@N@sub 4@ thin film deposited at 85°C. The breakdown field strength of MIM capacitors with 490 Å Si@sub 3@N@sub 4@ was larger than 4.1 MV/cm which indicates the excellent quality of the deposited Si@sub 3@N@sub 4@ film. The main capacitance of unit area extracted by RF (radio frequency) measurements was 1240 pF/mm@super2@. So, its high capacitance enables us to reduce the size of MIM to a quarter size compared with the conventional MIM having 2000 Å Si@sub 3@N@sub 4@. In spite of its thin thickness of dielectrics, RF characteristics showed good performance. Above all, it was fabricated at low temperature, so we were able to develop the process of MIM fabrication using dielectric lift-off. At this point, the thickness adapted in dielectric lift-off process was about 1000 Å for adjusting capacitance to a designed capacitance.

10:40am **DI+EL+MS-WeM8 Rapid Prototyping by Local Deposition of Siliconoxide and Tungsten Nanostructures for Interconnect Rewiring**, *H.D. Wanzenboeck, S. Harasek, H. Langfischer, A. Lugstein,* ***E. Bertagnolli***, Vienna University of Technology, Austria

The local deposition of dielectric material and metal wires as typically used for rewiring of interconnect layers has been demonstrated to be a promising approach for rapid prototyping of integrated circuits. With an ion beam induced surface reaction dielectric structures were fabricated with a selected geometric configuration in dimensions ranging from several hundred Âµm down to the deep sub-Âµm scale displaying the potential application in interconnect modification. A focused Ga ion beam at 50 kV acceleration voltage was applied to induce the surface decomposition of gaseous precursors. A dynamic adsorption state was achieved characterized by the equilibrium between influx through a nozzle system and the outlet through the vacuum pump. Siliconoxide was obtained by using siliconorganic compounds and oxygen as precursor adsorbed on the surface at a total pressure typically between 10E-5 to 10E-6 Torr. Conductive W-structures were obtained using W(CO)6. The suitability for practical applications in microelectronics has been demonstrated by measuring the electrical properties of deposited dielectrics using test vehicles with a metal-insulator-metal (MIM) capacitor setup. The thickness of the dielectric layer was varied between 70 nm and 1.4 Âµm. The resistivity and capacitance of FIB deposited dielectrics was found to vary with deposition parameters such as exposure time and scanning rate of the ion beam. A chemical characterization of the fabricated dielectric layers has been performed. The electrical properties of locally deposited dielectrics were correlated with the material composition of the deposited material. The suggested optimized deposition process can provide improved dielectrics suitable as interline and interlayer insulator for a complex microelectronic interconnect architecture.

Incorporating Principles of Industrial Ecology
Room 304 - Session IE+PS+MS+SE-WeM
Environmentally Friendly Process Development

Moderator: D.R. Baer, Pacific Northwest National Laboratory

8:20am **IE+PS+MS+SE-WeM1 CVD Films as Directly Patternable Low-k Dielectrics**, ***K.K. Gleason***, *H.G. Pryce Lewis,* Massachusetts Institute of Technology*; G.L. Weibel, C.K. Ober,* Cornell University **INVITED**

As microelectronic feature sizes decrease to 100-nm and below, major advances in both interconnect and lithographic technologies are necessary. Novel low-k candidates being assessed include fluorine- and silicon-containing materials produced by chemical vapor deposition (CVD). Fluorine- and silicon-containing polymeric materials are also ideal resist candidates for 157-nm photolithography, as conventional photoresists are opaque at this wavelength. In this paper, we present a collaboration aimed at merging the role of sacrificial resist and low-k dielectric. Specifically, we are investigating a direct dielectric patterning process in which a low-k fluorocarbon or organosilicon material is deposited by CVD, exposed, and developed using no wet processing. In our scheme, a film is deposited using hot-filament CVD, a non-plasma technique which offers the ability to tailor film chemistries. The film is masked and exposed using e-beam or a 157-nm source, and developed using supercritical CO@sub 2@ as a dry developing medium. The patterned film then serves as a low-k material compatible with metallization schemes such as the damascene process. This technology would greatly simplify future device manufacture by reducing the number of steps involved in patterning. The CVD process and the use of dry development also offer environmental, safety and health advantages over solvent-based spin-on coating and aqueous development. Positive-tone contrast has been demonstrated in fluorocarbon CVD films and fully-developed images of 0.25-micron have been demonstrated from e-beam exposure. We are presently working to enhance sensitivity and optimize image resolution.

9:00am **IE+PS+MS+SE-WeM3 Characterization of Remote Plasma Clean Process for Plasma CVD Chamber**, ***T. Tanaka***, *T. Nowak, M. Seamons, B.H. Kim, K. Lai, M. Cox, P. Loewenhardt, D. Silvetti, S. Shamouilian,* Applied Materials Inc.

Remote plasma cleaning of CVD process chambers has proven to be more efficient than conventional in-situ plasma cleaning in terms of higher throughput and higher gas breakdown efficiency. It is still important, however, to maximize the efficiency of the remote plasma clean process because of the potential environmental impact and the cost of process gases. The remote clean process involves three steps: generation of reactive species (mostly fluorine atoms) in a remote plasma source, transport of the reactive gas, and the cleaning reaction in the CVD chamber. We studied the efficiency of the process in each step. Since accurate direct measurement of the atomic fluorine concentration in the various parts of the CVD reactor is difficult, we used etching of thermal oxide wafer coupons to estimate the relative distribution of atomic fluorine within the reactor. Source dissociation efficiency was studied using an indirect technique based on correlation of pressure to effluent composition. We found that it requires approximately 24eV to break down each NF@sub 3@ molecule. This translates to 1.7W/sccm of NF@sub 3@ flow. This was seen to be approximately the same for both a microwave discharge operating at 2.45GHz and an inductively coupled plasma at 13.56MHz. Results characterizing the transport step demonstrate the importance of system design on minimizing recombination losses of the reactive species which, for a parallel plate reactor, can be as high as 50% of the atomic fluorine generated in the remote plasma source. The experimental results are compared with a simple model, which describes the general behavior of the cleaning process.

9:20am **IE+PS+MS+SE-WeM4 Silicon Oxide Contact Hole Etching Process Employing Environmentally Harmonized Technique**, ***K. Fujita***, *M. Hori, T. Goto,* Nagoya University, Japan*; M. Ito,* Wakayama University, Japan

Etching process of SiO@sub 2@ contact holes in ULSI has been developed by using high-density plasmas employing stable PFC gases. PFC gases, however, cause a serious environmental problem, namely global warming and hereby the uses of fluorocarbon gases would be restricted in the near future. Recently, we proposed environmentally harmonized technique replacing stable PFC gases for preventing global warming, where polytetrafluoroethylene (PTFE) is evaporated by a CO@sub 2@ laser and the generated fluorocarbon species (C@sub x@F@sub y@) are injected into ECR plasma reactor from externally. This technique, therefore, enables us to achieve a novel plasma process with new gas chemistries. In this study, this system has been successfully applied to ECR plasma etching of SiO@sub 2@ contact hole and the behavior of CF@sub x@ (x=1-3) radical densities in the plasma were evaluated by infrared diode laser absorption spectroscopy (IRLAS). The high SiO@sub 2@ etching rate of 780 nm/min was obtained at a microwave power of 400 W, a pressure of 2.7 Pa, a total flow rate of 80 sccm and a bias voltage of -450 V. Dependence of contact hole etching characteristics on Ar dilution and pressure has been investigated. Anisotropy of contact hole etching was improved with increasing the Ar dilution ratio and decreasing the pressure because the fluorocarbon polymer deposition was suppressed at the higher Ar dilution and the lower pressure. IRLAS measurements indicate CF@sub 2@ radicals and higher radicals (C@sub x@F@sub y@) have the good relation with the polymer deposition. The anisotropic contact hole etching was achieved at an Ar dilution ratio of 90 %, a pressure of 0.4 Pa and the etching rate of SiO@sub 2@, selectivity of SiO@sub 2@ to Si and selectivity of SiO@sub 2@ to resist were 340 nm/min, 31 and 6.4, respectively. These results indicate that this environmentally harmonized technique will propose the alternative etching system replacing PFC gases.

9:40am **IE+PS+MS+SE-WeM5 Photocatalytic, Anti-fogging Mirror**, ***K. Takagi***, ULVAC Japan, Ltd., Japan*; H. Hiraiwa, T. Makimoto, T. Negishi,* ULVAC Japan, Ltd.

Recently, environmental pollution is growing more serious everyday, and it is urgently required to develop resource-saving and non-chemical products, which may save and even purify the nature. In such circumstances,

titanium dioxide (TiO@sub 2@) thin coating film has come into the spotlight as a savior of the environmental problems. Because of its attractive photocatalytic natures, such as anti-bacterial, self-cleaning, decomposition of organic substances, and super-hydrophilic natures, TiO@sub 2@ has been studied and developed energetically in these days. Already, its super-hydrophilic and self-cleaning natures are applied to automobiles' anti-fogging side mirrors, which are now in practical use, and ULVAC Japan is one of the top makers for manufacturing vacuum deposition system for anti-fogging mirrors. The film architecture of this mirror is the double layer of SiO@sub 2@ / TiO@sub 2@ on the substrate coated by E/B evaporation or sputtering. The photocatalytic natures are as follows; 1. The contact angle of water on this surface is less than 10@Ao@ after irradiation of Blacklight, on which the engine oil is spreaded and cleaned by washing. 2. The contact angle keeps less than 10@Ao@ when this sample is preserved in the dark room. This report describes current developmental status of vacuum deposition system for TiO@sub 2@/SiO@sub 2@ thin film coating that is applied to automobile-mounted photocatalytic mirrors and is useful for environment saving and purification.

10:00am **IE+PS+MS+SE-WeM6 Low-k Materials Etching in Magnetic Neutral Loop Discharge Plasma**, *Y. Morikawa, S. Yasunami,* ULVAC JAPAN Ltd.*; W. Chen,* ***T. Hayashi,*** ULVAC JAPAN Ltd., Japan*; H. Yamakawa, T. Uchida,* ULVAC JAPAN Ltd.

Many low-k materials, like Si containing inorganic / organic compounds, purely organic compounds and porous silicate glass, are proposed and examined as the interlayer dielectric one. The magnetic neutral loop discharge (NLD) plasma is very useful for very fine pattern etching process, because the NLD plasma has high density and low temperature characteristics and tends to form uniform density distribution on the substrate, at lower pressure region than 1 Pa under 13.56 MHz oscillating induction field.@footnote 1-3@ So we adopted the NLD plasma to etch organic low-k materials, with very high etch rate over 900 nm/min by using NH@sub 3@. An etching issue for the purely organic low-k materials is bowing in the hole smaller than 200nm in diameter, probably caused by reaction of the hole-wall surface with hydrogen atoms. Based on this consideration, we carried out the etching by using nitrogen gas mixed with a low concentration of hydrogen gas in low pressures below 1 Pa. The etch rate increased abruptly at hydrogen addition of a few quantity and approached gradually to a constant value at 20%. But the bowing size became larger above hydrogen mixed ratio of 20%. So we measured mass spectra of ion species produced in the plasma to know the mechanism. It was found that intensity of N2H+ also increased abruptly and then was close to a constant value at 20%. The other species did not show similar tendency. It is deduced from this result that N2H+ ion may participate in main etching reaction to obtain the conformal etched profile. Etching characteristics for OSG, pure organic low-k materials and porous silicate glass will be shown. @FootnoteText@@footnote 1@W.Chen, T.Hayashi, M.Itoh, Y.Morikawa, K.Sugita, H.Shindo and T.Uchida : Jpn. J. Appl. Phys., 38 (1999) 4296 @footnote 2@W.Chen, T.Hayashi, M.Itoh, Y.Morikawa, K.Sugita and T.Uchida : Vacuum, 53 (1999) 29 @footnote 3@W.Chen, T.Hayashi, M.Itoh, Y.Morikawa, K.Sugita, H.Shindo and T.Uchida : J. Vac. Sci. Technol. A17(5), (1999) 2546.

Plasma Science and Technology
Room 311 - Session PS+MS-WeM

Plasma-Induced Damage

Moderator: L.J. Overzet, University of Texas, Dallas

8:20am **PS+MS-WeM1 Plasma-Induced Charging Gate Oxide Pinhole Formation**, ***T.C. Ang***, *S.Y. Loong, P.I. Ong, W.B. Loh,* Chartered Semiconductor Manufacturing, Singapore*; Y.W. Teh,* Nanyang Technological University, Singapore

Plasma process induced charging damage to gate oxide is a growing concern in ULSI MOS device fabrication. This is due to gate oxide thinning resulting from continuous CMOS downsizing and increasing use of high density plasma (HDP) tools. In this paper, we study the extent of the plasma induced damage resulting from HDP inter-metal dielectric deposition process in 0.18um transistor technology. Gate oxide pinhole formation resulting from plasma induced charging damage was observed above a threshold ion density. Transistor test structures with different types of antennas and antenna ratios were used to monitor the plasma damage. The extent of the plasma charging damage was evaluated through shift in gate leakage, threshold voltage and transconductance from a reference transistor with no antenna attached. Each of these parameters were measured for a large number of transistors in order to statistically assess the level of plasma based gate oxide damage. Gate oxide pinhole formation was observed in transistors with antenna ratios above a certain value. The pinholes were caused by localized breakthrough of the gate oxide resulting from charge imbalance in the plasma and are only present when the charge imbalance exceeds a threshold value. Based on our results, we have determined the threshold value for charge imbalance and ion density to cause gate oxide pinhole formation. We have also developed a novel integration scheme which is effective in reducing the charging damage from the high density plasma process significantly and no gate oxide pinholes were observed with the implementation of this scheme.

8:40am **PS+MS-WeM2 Effects of Plasma-induced Charging Damages on Thin Gate Oxide during Plasma Etching Processes**, ***Y.-K. Kim***, *K.-O. KIm, J.-Y. Kim, C.J. Choi, J.W. Kim,* Hyundai Electronics Industries Co., Ltd., Korea

Using the plasma damage monitoring (PDM) system, we investigated the plasma-induced charging damage in the thermally-grown SiO@sub 2@ on p-type Si substrates after plasma etching of gate electrode. Recently, the technique has been frequently employed to monitor oxide damages induced by plasma processes. It determines the changes in oxide electrical properties such as flatband voltage (V@sub fb@), oxide resistivity (@rho@@sub ox@), effective charges (Q@sub eff@), interface trap density (D@sub it@), etc. The measured Q@sub eff@ as well as D@sub it@ value indicates that the plasma has induced a large amount of positive charges trapped in the bulk oxide and the interfacial defects in the SiO@sub 2@-Si interfaces. The trapped oxide charges are also the origin of the large V@sub fb@ shifts as well as the reduced @rho@@sub ox@. The observed charging damages have been found to be dependent strongly on the etching gases as well as the plasma conditions. The site-dependent variations of the charging damages were attributed to the non-uniform radial distribution of the charges on the oxide surfaces during the etching processes. A MOS capacitor was fabricated over the thin thermal oxide by employing the above plasma exposures during the poly-Si electrode and the subsequent pad etching to measure the changes in the gate oxide integrity (GOI) characteristics. Finally, we will quantitatively show that the leakage current of the thin gate oxide after the plasma processing is strongly related with the measured PDM results.

9:00am **PS+MS-WeM3 The Use of Simultaneous Modulation of Source and Wafer RF to Reduce Plasma Induced Damage**, ***N. Hershkowitz***, University of Wisconsin, Madison **INVITED**

A variety of different types of plasma phenomena can lead to plasma induced damage in the fabrication of small geometry devices. Oxide charging (probably the most significant source of damage), macroscopic and microscopic differential charging, over energetic ion beams, UV induced carriers and plasma etch induced silicon substrate roughness are some examples. In this paper, it is argued that simultaneous modulation of source and wafer RF in HDP tools provides a "control knob" for eliminating and/or reducing many of the sources of damage. Data are presented showing improvements resulting from simultaneous source and wafer (on-off) modulation. RF frequency and modulation duty cycle effects are discussed together with damage reduction mechanisms.

9:40am **PS+MS-WeM5 Effect of Oxide to Nitride Etch Selectivity on Plasma Induced Charging Damage**, ***S. Ma***, *C. Björkman, R. Wang, L. Zhang, H. Shan,* Applied Materials Inc.*; R. Ramanathan,* Conexant Systems

Nitride layers are widely used for dual-damascene, self-aligned contact and border-less contact dielectric etch process as etch stop layers. It is also believed that such etch stop layer on top of metal electrode can also serve as plasma charging damage protection layer. This study shows no relationship between the dielectric to nitride etch selectivity and plasma induced charging damage. A Magnetically Enhanced Reactive Ion Etching (MERIE) chamber is used for this study with 0.25 um technology devices. In fluorine contained etching chemistry, strong recipe dependence on plasma charging damage is found regardless of the dielectric to nitride etch selectivity. A model of leaky nitride with charge built up on via hole bottom is proposed to explain the phenomena. In pure oxygen chemistry for in-situ polymer removal, plasma induced charging damage depends on the remaining nitride thickness. It is found that power is the most sensitive parameter than B-field, pressure, overetch and gas species to control damage. A mechanism is also proposed to explain the role of polymer formation and removal on top of nitride stop layer to plasma charging damage sensitivity

10:00am **PS+MS-WeM6 Aspect Ratio Dependent Plasma-Induced Charging Damage in RF Pre-Cleaning of Metal Contact***, **J. Kim**, K.S. Shin, W.J. Park, C.J. Kang, T.-H. Ahn, J.-T. Moon,* Samsung Electronics, Korea

As the packing density increases in the fabrication of semiconductor, the aspect ratio and the CD (Critical Dimension) of a metal contact are exponentially aggravated in the dry etch process. The aspect ratio dependency on a plasma-induced charging damage during the RF pre-cleaning of a metal contact has been evaluated with the two dimensional Monte-Carlo simulation and the related experiments. From the simulation of a metal contact opened on a gate metal, it is found that the potential on a metal contact bottom, which is directly related to plasma-induced charging damage, is saturated near 4 of aspect ratio after linearly increasing with the aspect ratio. However, the linear decrease of CD of a metal contact exponentially increases the potential stress on gate oxide. These simulation results are confirmed with the two different experiments, an in-situ charge-up monitoring and the electric test of a fully fabricated CMOS wafers. A phase-controlled inductively coupled plasma is proposed to suppress the plasma-induced charging damage. With the phase-controlled inductively coupled plasma, the plasma-induced damage is strongly suppressed when the phase delay of the bias power to the source power is near 180 degree.

10:20am **PS+MS-WeM7 Real-time Observation of Relaxation of Disorder-induced Surface Stress***, **T. Narushima**, N. Ueda,* University of Tsukuba, Japan*; A.N. Itakura,* National Research Institute for Metals, Japan*; T. Kawabe,* University of Tsukuba, Japan*; M. Kitajima,* National Research Institute for Metals, Japan

We present relaxation of disorder-induced surface stress. The surface stress changes on Si(100) were measured by means of an optical micro-mechanical cantilever technique. The samples were Si(100) cantilevers (450μm x 50μm x 2μm). They were treated by being dipped in 10% HF acid solution for 5 minutes, rinsed with deionized water for 5 minutes, and annealed at 1000K for 30 minutes in a UHV. To introduce disorder to surface, the surfaces were bombarded using an argon plasma with applying negative biases (-30V to -100V) at room temperature. Then, the disordered surfaces were oxidized using an oxygen plasma with applying positive bias (+45V), where the surfaces were subject to electron irradiation. We found a development of compressive stress on the Si surface due to defects produced by ion bombardment. This disorder-induced compressive stress was completely relaxed by the following plasma oxidation. The initial evolution of the surface stress during oxidation on the bombarded surfaces is quite different from that on unbombarded Si(100) surfaces. The disorder-induced stress was also relaxed completely by an exposure to argon plasmas under anodic conditions. The stress relaxation should be promoted not only by oxidation but also by electron irradiation. A possible mechanism of the stress relaxation is surface diffusion of Si adatoms via electron irradiation.

10:40am **PS+MS-WeM8 Transient Charging Effects of Insulating Surfaces Exposed to a Plasma During Pulse Biased DC Magnetron Sputtering***, **E.V. Barnat**, T.-M. Lu,* Rensselaer Polytechnic Institute

The ability to control the charging of thin dielectric films exposed to ionized discharges, using a pulsed bias, is studied experimentally and theoretically. A dielectric film is exposed to the discharge and the transient currents associated with the dielectric's charging are measured after each pulse. Factors effecting the time scale the film undergoes charging, including the dielectric constant, the dielectric's thickness, the plasma density, and the amount of potential applied during each pulse are explored. By constructing a simple model based on the plasma's impedance to the pulsed bias and the capacitive coupling between the electrode and the surface of the dielectric where the charge accumulates, the observed transient currents are explained. Calculations are then made to determine the energy distribution of the ions extracted from the plasma and how both the pulse of the electrode and the charging of the dielectric influence the ion energy distributions. To demonstrate an application of the pulse bias technique, it is shown that we can dramatically control the film morphology and microstructure by pulse biasing the electrode. Also, by properly setting the pulse bias, the pulse frequency or the pulse duty, damage to thin dielectric films, such as electrical breakdown, is prevented during metallization.

Dielectrics
Room 312 - Session DI+EL+MS-WeA

Alternate Gate Dielectrics
Moderator: R. Ramesh, University of Maryland

2:00pm **DI+EL+MS-WeA1 Materials Considerations for High-K Gate Dielectrics for Scaled CMOS**, ***G.D. Wilk,*** Lucent Technologies*; R.M. Wallace,* University of North Texas **INVITED**

Many materials systems are currently under consideration as potential replacements for SiO@sub 2@ as the gate dielectric material for sub-0.13 µm CMOS technology. A systematic consideration of the required properties of gate dielectrics, however, indicates that the key issues for selecting a high-k dielectric are permittivity and band offset, thermodynamic stability, crystal structure, and compatibility with the current or expected materials to be used in processing for CMOS devices. Many dielectrics satisfy some of these criteria, but very few materials actually satisfy all. A review of current work and literature in the area of high-k gate dielectrics is given, and some conclusions are drawn for various systems based on reported results and fundamental materials considerations.

2:40pm **DI+EL+MS-WeA3 New High k Thin Films with Improved Physical and Electrical Properties**, ***Y. Kuo,*** *J. Donnelly, J. Tewg,* Texas A&M University

When the minimum device dimension is shrunk to 100 nm, the conventional silicon oxide cannot fulfill many requirements of the device.@footnote 1@ For example, the thin gate dielectric layer (e.g., < 1.2 nm) will have a high leakage current and cannot stop the boron penetration. The dielectric constant of silicon oxide (e.g., 4.0) is too low for the small-size storage capacitor cell. Therefore, it is urgent to develop a new kind of thin film dielectric that has a high dielectric constant (high k) and can satisfy all stringent material, process, and device requirements. Metal oxides are ideal candidates for the gate dielectric application because their compositions are simple and their k values are high enough to last for next several generations of devices. In addition to the high interface states, a metal oxide has the problem of high leakage current, which is caused by the polycrystalline phase formation during the high temperature process.@footnote 2,3@ In this paper, we present new results on high k metal oxides that have high amorphous-to-polycrystalline transition temperatures. By adding a third element into tantalum oxide, e.g., Ti, Cu, and Mo, the film can exist in the amorphous phase in an extended temperature range. The leakage current at a high temperature is lowered. Material and electrical characteristics of the new film, e.g., by x-ray diffraction, ellipsometer, current-voltage and capacity-voltage curves, will be shown and discussed. The influence of the deposition process, i.e., reactive co-sputtering, to film properties will also be presented. These new high k dielectrics have the potential of being used as gate dielectrics in future MOS devices. @FootnoteText@ @footnote 1@ International Technology Roadmap for Semiconductors, 1999 ed., SIA, etc. @footnote 2@ S. R. Jeon, S. W. Han, and J. W. Park, J. Appl. Phys. 77, 5978, 1995. @footnote 3@ R. B. van Dover, R. M. Fleming, L. F. Schneemeyer, G. B. Alers, and D. J. Werder, IEDM, 823, 1998.

3:00pm **DI+EL+MS-WeA4 Chemical and Microstructural Separation of Homogeneous Plasma Deposited (ZrO@sub2@)@subx@(SiO@sub2@)@sub(1-x)@ films (x @<=@ 0.5) into SiO@sub2@ and ZrO@sub2@ Phases after Rapid Thermal Annealing in Ar at 900°C**, ***B. Rayner,*** *R. Therrien, G. Lucovsky,* North Carolina State University

Zr-silicate alloys along the pseudo-binary join from SiO@sub2@ to ZrO@sub2@ have attracted interest as high-k dielectrics for Si CMOS devices with equivalent oxide thickness extending to 0.6 nm. In this study alloy films were deposited on HF-last and pre-oxidized and/or nitridized Si(100) by remote plasma enhanced chemical vapor deposition using Zr(IV)-t-butoxide. Film and interface chemical composition, local atomic bonding, and film morphology were studied by Auger electron spectroscopy, Fourier transform infrared absorption, X-ray diffraction, and Rutherford back-scattering. These studies identified two alloy regimes: (i) SiO@sub2@-rich compositions to the compound silicate, ZrSiO@sub4@ (x = 0.5), where properties may be suitable for high-k applications, e.g., films are amorphous on deposition and remain so up to at least 800°C, and (ii) ZrO@sub2@-rich compositions in which films are either partially or totally crystalline on deposition, or after relatively low temperature (< 600°C) anneals. Alloys in the SiO@sub2@-rich regime are chemically-ordered as-deposited at ~350°C with predominantly Si-O-Si and Zr-O-Si bonds, but after annealing in Ar at 900°C for 60 s, separate chemically and microstructurally into SiO@sub2@ and ZrO@sub2@ phases. The ZrO@sub2@ phase is crystalline at the ZrSiO@sub4@ composition. This separation may limit integration of these films into devices which incorporate polycrystlline-Si gate electrodes requiring dopant activation at temperatures > 900°C. Capacitance-voltage and current-voltage characteristics will be presented for as-deposited and annealed films to illustrate the effects of chemical phase separation and crystallization in defining maximum post deposition processing temperatures.

3:20pm **DI+EL+MS-WeA5 A Study of ZrO@sub2@ and Zr-silicate Thin Film for Gate Oxide Applications**, ***S.-W. Nam,*** Yonsei University & Samsung Electronics Co., Korea*; J.-H. Yoo, H.-Y. Kim, D.-H. Ko,* Yonsei University, Korea*; S.-H. Oh, C.-G. Park,* Pohang University of Science and Technology (POSTECH), Korea*; H.-J. Lee,* Stanford University

We investigated the microstructures and electrical properties of ZrO@sub2@ and Zr-silicate thin films deposited by reactive DC magnetron sputtering on Si substrate for gate dielectric application. The films deposited on Si with various deposition conditions and annealing treatments were analyzed by spectroscopic elipsometry, XRD, AFM and XPS. The refractive index of the ZrO@sub2@ thin films increased upon annealing. The ZrO@sub2@ film deposited at low temperature and low power showed amorphous structure, which the films deposited at high temperature and high power showed crystalline structures. The growth of the interfacial oxide between ZrO@sub2@(or Zr-silicate) and Si substrate was observed by cross sectional HR-TEM. C-V and I-V measurements of the MOSCAP structures showed that the accumulation capacitance value and the leakage current level decreased upon annealing in O@sub2@ gas ambient, which is explained by the formation of the interfacial SiO@sub2@ layer.

3:40pm **DI+EL+MS-WeA6 Ultra-thin Zirconium Oxide Films Deposited by Rapid Thermal CVD for MOSFET Applications**, ***Y. Lin,*** *J.P. Chang,* University of California, Los Angeles

The increasingly tighter process specifications for the next generation microelectronic devices dictate the usage of metal oxides such as zirconium oxide as insulators for better process control and a more reliable dielectric/silicon interface.@footnote 1@ Zirconium t-butoxide is used with O@sub 2@ in this work to deposit zirconium oxide in a RTCVD system. The deposition temperature can be rapidly ramped to and controlled at 400-600°C, and the physical properties of the ZrO@sub 2@ films are characterized by XPS, XRD, AFM, TEM, and spectroscopic ellipsometry to determine the film compositions, chemical states, film microstructures, morphology, thickness, and index of refraction. Amorphous and nearly stoichiometric ZrO@sub 2@ has been deposited with less than 0.2nm variation in thickness across a 4" wafer. The dielectric constant is 3-4 times greater than that of SiO@sub 2@. Leakage current of a ZrO@sub 2@ film with an effective oxide thickness of 10 Å is three orders of magnitude lower than that of a 10Å thermal SiO@sub 2@ film. Post-deposition annealing at 500-700°C is shown to be effective in removing the majority of the incorporated carbon and further reduce the leakage current. However, there exists an optimal carbon doping level where carbon effectively passivates the electrically active defects and reduces the leakage current. We propose a simple kinetic model to describe the heterogeneous reactions responsible for the film deposition. NMOS transistors are fabricated and tested to determine the dielectric constant, leakage current, I-V and C-V characteristics of the zirconium oxide films. Moreover, stress induced leakage current and time dependent dielectric breakdown will also be detailed to assess the material reliability for its applications in microelectronics. @FootnoteText@ @footnote 1@G. D. Wilk, and R. M. Wallace, "Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon," Appl. Phys. Lett., 74(19), 2854(1999).

4:00pm **DI+EL+MS-WeA7 High-quality Ultrathin Fluorinated Silicon Nitride Gate Dielectric Films Prepared by Plasma Enhanced Chemical Vapor Deposition Employing NH@sub 3@ and SiF@sub 4@**, ***H. Ohta,*** *M. Hori, T. Goto,* Nagoya University, Japan

The silicon nitride (SiN@sub x@) film attracts much attention as scaled gate dielectric films in next generation@super ,@s ULSI. However, the conventional SiN@sub x@ film has a poor interface with silicon and is leaky due to a high trap density in the film. Recently, we have developed ultrathin fluorinated SiN@sub x@ films formed by ECR-PECVD employing NH@sub 3@/SiF@sub 4@. It is known that the average bond energy (5.73eV) of Si-F is higher than that of Si-H (3.18eV). Therefore, it is

expected that the Si-F bond in the film should have improved the quality of gate dielectric film. In this study, we have investigated properties of ultrathin SiN@sub x@ films (4nm) formed at 350°C. These films (fluorinated SiN@sub x@ films) contain fewer hydrogen atoms than the conventional SiN@sub x@ films formed by ECR-PECVD employing NH@sub 3@/SiH@sub 4@. As-deposited fluorinated SiN@sub x@ films indicated the excellent hysteresis loop (20mV) in the C-V curve, and reduced the leakage current by several orders of magnitude than the thermal SiO@sub 2@ in the identical equivalent oxide thickness (EOT). These film properties and the surface reactions for the SiN@sub x@ film formation with good quality are discussed on the basis of results of the in-situ XPS, in-situ FT-IR RAS, FT-IR, and thermal desorption mass spectroscopy (TDS). As a result, the control of fluorine concentration in the SiN@sub x@ films was found to be a key factor for forming the fluorinated SiN@sub x@ films with high quality at low temperatures. The fluorinated SiN@sub x@ is very effective for ultrathin gate dielectric films in next generation@super ,@s ULSI.

4:20pm **DI+EL+MS-WeA8 Elimination of Carbon Impurities in the Metalorganic Chemical Vapor Deposition (MOCVD) of Titanium Dioxide on Silicon**, ***M. Yoon***, *A.C. Tuan, V.K. Medvedev,* University of Washington*; J.W. Rogers, Jr.,* Pacific Northwest National Laboratory

A novel process has been developed for the deposition of titanium dioxide thin films on p-type Si(100) with high quality interfacial characteristics and the absence of carbon. Elimination of carbon contaminants in the titanium dioxide film and at the interface between the oxide and silicon is important because the presence of impurities can severely degrade the electrical properties of the device. This novel process consists of three stages of deposition in an ultra-high vacuum chamber. Initially, a continuous titanium layer is deposited on silicon using a titanium sublimator. This titanium layer is then oxidized using a gas phase oxygen source to form a TiO@sub x@ buffer layer. Subsequently, a titanium dioxide thin film is deposited by MOCVD using titanium tetrakis-isopropoxide (TTIP) at low temperature (below 650K). Auger electron spectroscopy (AES) analysis at each stage of growth shows no evidence of carbon contamination either within the titanium dioxide layer or at the TiO@sub 2@/Si interface. Additional AES measurements suggest that the titanium layer grows on silicon according to the Stranski-Krastanov mode, which permits uniform growth. A carbon-free titanium dioxide thin film was successfully deposited on silicon using this novel process.

4:40pm **DI+EL+MS-WeA9 Microscopic Understanding of the Interface for the Heteroepitaxy of Crystalline Oxides on Silicon**, ***S. Gan***, *D.E. McCready, D.J. Gaspar, Y. Liang,* Pacific Northwest National Laboratory

With SiO@sub 2@ approaching its fundamental limit as the gate dielectric in the existing Si-based CMOS technology, searching for alternative gate oxides with high dielectric constants is crucial for the next generation of devices. Recent work showed crystalline oxides such as SrTiO@sub 3@ (STO) is promising as an alternative to SiO@sub 2@ in MOS capacitors. One of the most important issues is how to integrate it into the existing Si-based technology, the first step of which is the growth of epitaxial oxides on Si substrates. Here we present our recent results on the study of the oxide-silicon interface, which plays a critical role in growing high-quality STO films. Employing scanning tunneling microscopy (STM), x-ray photoelectron spectroscopy (XPS), low-energy electron diffraction (LEED), we characterized the interfacial structure of each template layer (Sr and SrO) grown on Si in situ. The results revealed that the strontium covered silicon surfaces exhibit a series of reconstructions, including a (2x1) structure that provides the most stable interface for the growth of oxides. In addition, we used time-of-flight second ion mass spectrometry (TOF-SIMS) and x-ray diffraction (XRD) to investigate the interfacial chemistry and film structure. By combining these techniques, we correlated the interface structures with film properties, which allowed us to identify suitable interfacial templates for optimized growth. @FootnoteText@ Pacific Northwest Laboratory is a multiprogram national laboratory operated by Battelle Memorial Institute for the U.S. Department of Energy under Contract DE-AC06-76RLO 1830.

5:00pm **DI+EL+MS-WeA10 Formation of Ultrathin Yttrium Silicate by Thermal Oxidation of Yttrium on Silicon**, ***M.J. Kelly***, *J.J. Chambers, D. Niu, G.N. Parsons,* North Carolina State University

We show that direct thermal oxidation can be used to form thin (<50@Ao@) high-k metal silicate layers directly on crystalline silicon. Bulk thermodynamics indicates that several high-k metal oxides (including oxides of Hf, Zr, Al, Y, La, etc.) will be stable with respect to silicon dioxide formation when the oxide is in contact with silicon. However, most low temperature approaches (PVD, CVD, or MBE) for metal oxide deposition on silicon involve elementary reaction steps that include metal-silicon bond formation before oxidation, resulting in uncontrolled interface layers between the metal oxide and silicon. We can utilize this mechanism to form yttrium silicate films on silicon by first sputtering thin (<10@Ao@) metal films on silicon, vacuum annealing at 300-600Â°C to form a silicide, then oxidizing at 600-900Â°C. XPS, medium energy ion scattering, and IR indicate film composition is close to yttrium orthosilicate (Y2O3Â·SiO2) with some excess Y2O3, depending on anneal conditions. Oxidation kinetics (determined from thicknesses measured by TEM) indicate an initial fast oxidation rate (due to oxidation of metal silicide), followed by a slower process (due to oxidation of underlying silicon). CV analysis of 42@Ao@ films show oxide equivalent thickness ~12@Ao@, consistent with dielectric constant ~14. Leakage is <1A/cm2 at 1V in accumulation. IR and XPS indicate that films do not phase separate when annealed up to 900Â°C for 20 minutes. Thin (<10@Ao@) silicon oxide and nitride interface layers have been formed in-situ by remote plasma exposure before metal deposition and their effect on interface reaction kinetics have been analyzed by XPS and MEIS. Interfacial oxide is observed to have a negligible effect on interface reactions, but results suggest interface nitrogen tends to block silicide formation before oxidation. These results give important insight into controlling interface structure for implementing high-k materials into silicon devices.

Manufacturing Science and Technology
Room 304 - Session MS-WeA

Process Integration (Cu/Low-k/300mm)

Moderator: M. Surendra, IBM T.J. Watson Research Center

2:00pm **MS-WeA1 Integration Challenges for Copper Metallization with Low-k Dielectrics**, ***B.L. Chin***, Applied Materials **INVITED**

The transition from Al metallization to Cu has been implemented during the past several years and successfully introduced into several device products. This has resulted in improvement in device chip speed due to the resistivity reduction. To further decrease the RC time delay and minimize cross talk between interconnect lines, the transition to low-k materials has been actively investigated but the implementation has not been as rapid or straightforward. The convergence of Cu metallization with low-k dielectric has been hampered by the difficulty in replacing the present SiO@sub2@ with a low-k material that meets all the film property requirements: mechanical, thermal and electrical compatibility. Key integration issues for the low-k material include dual damascene pattern definition, adhesion of the barrier/ seed and adequate planarization. A review of the various materials and technologies (PVD, CVD) to deposit the barrier/ seed will be presented along with the pre-clean methods to ensure low via resistance. A survey of the different barrier films and barrier testing will illustrate the need for evaluating not only out-diffusion of Cu into the dielectric but also the in-diffusion of other components from the dielectric (e.g. diffusion of F from FSG to Cu). The currently used Ta-based barriers will be compared with composite layered structures and new materials. The necessity for decreasing the seed layer thickness for electroplating fill has placed a greater demand on the step coverage and resultant interface properties. Recent advances in electroplating technology may resolve this issue and its impact on integration with low-k materials will be highlighted. These challenges will be further amplified with the introduction of porous low-k materials and may force the implementation of other technologies to satisfy the requirements for sub- 0.1 µm devices.

2:40pm **MS-WeA3 Adventure of the first 300mm Pilot Line**, ***M. Peschke***, Semiconductor 300 GmbH&Co.KG, Germany **INVITED**

The transition in wafer size has always been a risky project in the past. Even for very sophisticated and wealthy companies it was a painful experience. Using the synergy of the know how and share the costs Infineon Technologies and Motorola announced in 1998 a Joint venture (Semiconductor 300) for a 300mm pilot line located in Dresden. Based on the standards provided by i300i and Selete (i.e. CIM/ Automation or FOUP requirements, process specifications), the equipment manufacturers could provide the simultaneous availability of all required tools. When SC300 started first test results were already available and the visibility "first sample of a working transistor" was already shown by Motorola. The factors to influence the productivity improvement of 30% per year, become smaller so the manufacturing effectiveness has to gain to keep the improvement rate. The focus was directed to reliability of the tools, whereas the process performance was assessed as a "must criteria". The equipment industry has grown tremendous in the last years so the financial strength and expertise has grown as well. All the new ideas of

improvement which could not implemented in the existing tool set went into the design of the new generation. A key factor for the success of the SC300mm project has been the open relationship with the equipment suppliers. Jointly the tools were tested and stressed under manufacturing conditions. The technology which was used to ramp up the 300mm pilot line was a state of the art DRAM product. With the redundancy of a DRAM the impact of defect density is limited and so learning cycles were faster. With the help of the local infrastructure of the 200mm production line, which ran the same product, problems were solved faster. The success of the first 300mm pilot line nine month after tool installation, demonstrates the potential of the existing tool set.

3:20pm **MS-WeA5 Cluster Formation on Copper Evaporated Onto Dow Cyclotene 3022**, ***E. Sacher***, *D.-Q. Yang, S. Poulin, S. Rodrigues, L. Martinu, M. Meunier,* Ecole Polytechnique, Canada

Dow Cyclotene 3022 is a low permittivity polymer used in the microelectronics industry. It is made through the Diels-Alder polymerization of bis-benzocyclobutene-terminated divinyl siloxane monomers. Key Cu integration issues concern the adhesion of patterned Cu lines and the stability of the Cu-polymer interface to metal diffusion. Photoacoustic FTIR and XPS have shown that the Cu atoms interact asymmetrically with the aromatic rings of the Cyclotene to give weak bonding across the interface. XPS, XRD, AFM, TEM, spectroscopic ellipsometry, and other techniques, have shown that the Cu exists in the form of surface clusters. TEM micrographs, for example, show that a nominal 3.2 nm deposit exists in the form of irregular clusters with an average diameter estimated at 9 nm. This may be compared with an XPS estimate, based on an intensity comparison at two different orbital energies, which suggests that the clusters are spherical and about 7 nm in size. The weak bonding permits surface diffusion, which causes cluster coalescence on annealing, although there is no evidence, from any technique available to us, of diffusion into the bulk Cyclotene. The structure and properties of the Cu/Cyclotene interface will be compared with adhesion studies by microscratch and adhesive tape peel tests.

3:40pm **MS-WeA6 FSG Film Characterization and Process Development for Copper/Damascene Technology**, ***J.S. Martin***, *K.J. Taylor, J.D. Luttmer, A.R.K. Ralston, T.D. Bonifield, J.A. West,* Texas Instruments, Inc.*; C.T. Adams, K.-H. Chew, A. Bayman, B. van Schravendijk,* Novellus Systems, Inc.

The microelectronics industry is transitioning from wiring devices with aluminum and oxide-based interconnect structures to damascene-based integration, with both copper and low-k materials. Toward this end, we outline the process technology and material characterization for a fluorosilicate glass (FSG) developed specifically for copper/damascene technology, where both the via and metal line are embedded in FSG at six levels. We compare FSG deposited in both high density plasma (HDP) and standard PECVD reactors, for K values within the range 3.50 - 3.70. Fluorine loss and water absorption are appreciably less for HDP-FSG films. We note two additional issues for FSG processes and films. First, adhesion to subsequently deposited PECVD silicon nitride is problematic and delamination increases with thicker FSG films. Second, deposition temperature strongly influences in-film [F], but for systems without active wafer temperature control, wafer temperature, and hence in-film [F] depends on the substrate dopant concentration. We briefly outline our methods for actively controlling wafer temperature to ± 5°C during deposition and monitoring [F] in-line via X-ray fluorescence (XRF). HDP-FSG thin films are thus deposited with active temperature control, and in-film [F] is controlled to within ± 0.2 atomic percent, as measured by XRF. Most important, by systematically decreasing in-film [F] over a 25% range, we observe that K-value increases by 0.10 and adhesion to silicon nitride significantly improves. We view this as a viable FSG process, applicable at the 0.18 μm and 0.13 μm nodes.

4:00pm **MS-WeA7 300mm Manufacturing Meterology Needs**, ***R. Goodall,*** Sematech **INVITED**

PLEASE SEND US AN ABSTRACT. Thank you.

Plasma Science and Technology
Room 310 - Session PS1+MS-WeA

Sensors and Control in Plasma Processing

Moderator: I.P. Herman, Columbia University

2:00pm **PS1+MS-WeA1 Supervision of Plasma Processes using Multiway Principal Component Analysis**, ***D. Knobloch***, *F.H. Bell,* Infineon Technologies AG, Germany*; K. Voigtlaender, J. Zimpel,* Fraunhofer Institute IVI, Germany

In modern IC-manufacturing lines, plasma processing is still one of the most complex single process steps. The trend towards even smaller feature sizes and greater wafer diameters results in the need of better process and equipment control. In previous studies@footnote 1,2@, we have shown that an OES-system, based on a multiband CCD-spectrometer and operated with a home built software, can be used for run-to-run and real time process control. In this work, we show how we extended our software tool in order to improve data analysis. A MPCA (Multiway Principal Component Analysis) has been implemented that allows extraction of key numbers from spectral data simultaneously in time and wavelength. Key numbers are extracted for single processes as well as for run-to-run variations. As an example, the chamber conditions as a function of rf-hours and process mix is characterized by MPCA key numbers. It is shown, that the key numbers represent the cleanliness of the plasma chamber that depends on the process mix. Consequently, the key numbers can be used to establish an optimum product flow in the chamber in order to optimize wet clean cycles and control particle generation. Furthermore, we demonstrate, how fault detection, such as determination of gas flow variations or chamber leaks, can be achieved. The MPCA key numbers of misprocessed wafers show variations to processing of good wafers and can be correlated to certain equipment or process faults. However, the establishment of a catalogue with spectral pattern of fault classifications, such as chamber leaks, is needed. Consequently, preventive maintenance is triggered in order to fix the observed equipment faults as soon as possible. @FootnoteText@ @footnote 1@ D. Knobloch et al, November 1998, AVS 45th International Symposium, Baltimore @footnote 2@ D. Knobloch et al, October 1999, AVS 46th International Symposium, Seattle

2:20pm **PS1+MS-WeA2 Sensors and Control in Plasma Processing**, ***J.C. Arnold***, *M.J. Hartig, C.F. Pfeiffer, J.A. Rivers, M.L. Johnson,* Motorola Semiconductor Products Sector **INVITED**

Even with the entrance of such processes as CMP and electrochemical deposition into the mainstream of semiconductor manufacturing, plasma processes remain among the most complex processes in the fab as well as among the most difficult to sustain. Furthermore, plasma deposition, etching, and cleaning processes are so numerous in typical product flows that the potential economic impact of plasma tool or process breakdowns is tremendous. The impetus for application of advanced sensors and automatic controls to these processes has been clear for years; however, widespread deployment of these devices and techniques in high volume manufacturing has been elusive. In this presentation, we will examine reasons for the apparent weakness in the pace at which sensors and controls have been adopted. We will begin with consideration of the terms "sensor" and "control" as related to the current state of the art in plasma processing. We will evaluate some of the sensor and control industry's current offerings in the context of the sensor and factory CIM system's ability to provide the "Acquisition - Analysis - Action" chain of three characteristics which we believe to be essential for adding value in the manufacturing environment. Finally, we will offer some end user perspectives on how changes in the business relationships between sensor and software vendors, capital equipment suppliers, and device manufacturers would facilitate more rapid and effective transfer of new techniques from the research lab to the production floor.

3:00pm **PS1+MS-WeA4 Run-to-Run and Real Time Process Control of Plasma Processes using an Inductive Antenna with Microsecond Resolution**, ***J. Mathuni***, *F.H. Bell, D. Knobloch,* Infineon Technologies AG, Germany

Equipment and process stability during the fabrication process of integrated circuits is one of the main issues in current and future production lines. This is particularly mandatory for plasma processes. Intelligent run-to-run and real time control using plasma sensors help to prevent wafer scratches or misprocessing and to monitor chamber drifts, e.g. caused by damaged reactor walls or polymer coating on chamber walls during wet cleans. We have implemented the real time control of plasma processes using an in house developed antenna that measures the electric

field of the plasma with microsecond resolution. Introduction of this sensor in our fabrication lines was challenged by two factors, namely, the development of robust and low cost hardware and easy to use software including process and equipment related control algorithm. The latter needs special attention, since the time resolution in the range of microseconds results in a very high amount of data making intelligent data reduction techniques mandatory. The measurement technique requires a dielectric material between plasma and sensor that can be easily realized using the quartz endpoint window of the plasma chamber. The benefit of this sensor is demonstrated for applications such as arcing detection, a phenomenon that may occur during microseconds and results in yield killing particle generation, and process parameter dependencies, such as B-field and power analysis. As a result, preventive maintenance is automatically triggered by sensor data. Since the sensor allows electric field measurements with nanosecond resolution, analysis of pulsed plasmas could be a further application.

3:20pm **PS1+MS-WeA5 Improved Utility of Microwave Energy for Semiconductor Plasma Processing through RF System Stability Analysis and Enhancement**, ***P.W. Rummel,*** *T. Grotjohn,* Michigan State University, US

The bulk of today's semiconductor plasma processing equipment utilizes RF energies at frequencies from 50 KHz to 60 MHz for deposition, etching, cleaning and various other processes. One of the impediments to utilizing microwave energy for these processes is the inherent instability often encountered with systems operating at frequencies of .5 to 2.45 GHz. Systems with plasma loads excited by resonant antennas, impedance matched by resonant circuits or cavities, and powered by generators of various source impedances are invariably unstable over some operating conditions. For microwave systems, this instability typically manifests itself as a propensity for the plasma to extinguish or rapidly change to a lower density as the impedance matching device is adjusted to minimize reflected power to the microwave generator. This paper shows why this instability exists and how a microwave driven plasma system can be modified to achieve better stabilization. A Matlab Simulink model and a state-model control analysis are used to identify system parameters that affect system stability and to predict the results of modifying those parameters towards the goal of improving stability. A plasma system utilizing a microwave cavity plasma reactor operating at 2.45 GHz. is first characterized to develop the models, and then modified to improve stability and illustrate the models' predictions. A high correlation between predicted and measured system stability validates the method of using a control analysis to model plasma system stability.

3:40pm **PS1+MS-WeA6 Modeling and Real-time Control of RF Diode Sputtering for GMR Thin Film Deposition**, ***S. Ghosal,*** *R.L. Kosut, J.L. Ebert, L. Porter,* SC Solutions, Inc.*; D.J. Brownell,* Nonvolatile Electronics, Inc.*; H.N.G. Wadley,* University of Virginia, usa

This presentation describes the development and implementation of real-time control of rf diode sputter deposition resulting in significantly reduced wafer-to-wafer variation in device properties. Giant magnetoresistive (GMR) materials have very important applications which include technologies such as hard disk read-heads, computer memory, and sensors. One common configuration for thin-film sensors made by NVE is the GMR multi-layer consisting of sixteen metallic layers with individual layer thickness ranging from 15 to 40 @Ao@. For maximum GMR, the acceptable variation in layer thickness from one deposition cycle to another is very small (0.5 @Ao@ for the critical CuAgAu conducting layer). Before this work, there was considerable variation in GMR properties from wafer to wafer, despite no change in the nominal values of layer thickness. Sensitivity studies using a steady-state physical model (integrating plasma, sputter and atom transport processes) showed deposition thickness falling out of acceptable range with relatively small changes in rf power, chamber temperature, pressure, and electrode spacing. Careful experiments showed that while three of the four variables were controlled relatively well, there was significant variation (>1%) in total rf power delivered due to transients at the onset of the plasma. A controller was designed to compensate for transient fluctuations by turning off the plasma based on the time-integrated DC bias voltage at the target. This approach keeps the total rf energy input into the plasma constant for individual layers deposited. As a result of implementing this controller, the standard deviation (wafer-to-wafer) in average GMR % and in sheet resistance were both reduced by more than half. Additionally, guided by the integrated physical model, within-wafer uniformity was considerably improved by optimal electrode spacing and target shaping.

4:00pm **PS1+MS-WeA7 Productivity Solutions for Eliminating Within-Wafer and Wafer-to-Wafer Variability in a Silicon Etch Process through Plasma and Surface Diagnostics**, ***E.A. Edelberg,*** *L.B. Braly, V. Vahedi, J. Daugherty,* Lam Research Corporation*; S.J. Ullal, A.R. Godfrey, E.S. Aydil,* University of California, Santa Barbara*; H.K. Chiu, H.J. Tao,* Taiwan Semiconductor Manufacturing Corp.

Various plasma and surface diagnostics were used to understand the root causes that lead to within-wafer and wafer-to-wafer variability in critical dimension (CD) loss in Si etch applications. It is found that the conditions of the reactor walls can play a significant role in determining the plasma properties and therefore the figures of merit of the etching process. Etch products from the wafer can adsorb and build up on the walls of the chamber leading to changes in the wall properties. These changes can lead to drifts in the plasma properties and cause wafer-to-wafer variability of the etch process. It is demonstrated that such drifts can be avoided by cleaning the walls of the reactor using Fluorine-containing plasmas in between wafers. We demonstrate that a fundamental understanding of the chemistry and composition of the deposited materials on the walls of the chamber and their relation to the gas phase species can be used to develop and optimize appropriate reactor wall cleaning processes. A multiple pass downstream Fourier transform infrared (FTIR) spectrometer is used to quantitatively measure the concentration of gas phase species such as SiCl@sub 4@ and SiF@sub 4@ in the reactor exhaust. In addition, a novel diagnostic technique based on the principles of multiple total internal reflection FTIR spectroscopy is used to measure, in situ, the presence and composition of material deposited or removed from the walls of the chamber. In particular, during Si etching processes with Cl@sub 2@/O@sub 2@ plasmas, the deposited films were found to be the byproducts of the etching reactions and contain Si, O and Cl. We show that performing a short plasma chamber clean with the appropriate chemistry between each wafer can reduce the wafer-to-wafer variability of both etch rate and CD bias. By performing an in situ clean after every wafer during a 0.13 micron gate etching process the wafer-to-wafer repeatability is reduced to 2nm (at 3 sigma).

4:20pm **PS1+MS-WeA8 Source Optimization for Magnetron Sputter-Deposition of NbTiN Tuning Elements for SIS THz Detectors**, ***N.N. Iosad,*** Delft University of Technology, The Netherlands*; B.D. Jackson, J.R. Gao,* Space Research Organization of the Netherlands*; S.N. Polyakov,* Moscow State University*; P.N. Dmitriev,* Russian Academy of Sciences*; T.M. Klapwijk,* Delft University of Technology, The Netherlands

NbTiN is one of the most promising materials for use in the tuning circuits of Nb-based superconductor-isolator-superconductor (SIS) mixers for operating frequencies above the gap frequency of Nb (about 700 GHz). Device development requires stable and reproducible film properties. In this manuscript we compare the properties of NbTiN and NbN films obtained with a DC magnetron sputtering source using balanced and unbalanced magnetic trap configurations. This experiment shows that reducing the effectiveness of the magnetic trap by changing the magnet configuration is equivalent to reducing the sputtering pressure from the prospective of the film properties. We find that the properties of the films are not stable throughout the target life-time. Sputtering source with balanced configuration shows degradation of the NbN film properties as the target gets grooved for the fixed applied power and sputtering pressure. In contrast unbalanced sputtering source shows opposite behavior for the NbTiN films. We also show that it is possible to optimize the configuration of the magnetron magnets to produce stable and reproducible NbTiN films under the same gas pressure and applied power throughout the target lifetime.

4:40pm **PS1+MS-WeA9 Multiwavelength In-Situ Ellipsometry for Optical Coatings Fabrication: Optimal Control Strategies and Results**, ***A. Hofrichter,*** *D. Kouznetsov, P. Bulkin, B. Drevillon,* Ecole Polytechnique, France

There is an increasing interest in adopting ellipsometric control for the manufacturing of optical filters. Ellipsometry does not relay on the amplitude of reflected signal, has very high sensitivity to both, thickness and complex refractive index, and can be used directly to probe growing surface, thus it is neither limited to transparent films nor depends on stability of light source. In comparison with such traditional techniques, as quartz crystal monitor and transmission/reflection spectrometer or laser interferometer, it is free of most their problems. However, interpretation of ellipsometric data is much more complicated and usually prevents application of ellipsometers for real-time process control in industrial environment. We present a robust algorithm for feed-back control of the PECVD deposition, based comparison of pre-computed ellipsometric

trajectories with real-time data stream. Such approach allows to stop growth of each layer with high accuracy without performing complicated real-time inversion of ellipsometric data. Using our Integrated Distributed Electron Cyclotron Resonance (IDECR) PECVD reactor we performed depositions of multilayer and gradient optical coatings with good agreement with design. The next step will be inclusion of dinamic corrections of gas flows based on real-time determination of refractive index profile.

5:00pm **PS1+MS-WeA10 Low Open Area Endpoint Detection of Plasma Etching Processes - Limitations and Signal to Noise Characterization***, **B.E. Goodlin**, D.S. Boning, H.H. Sawin,* MIT*; M. Yang,* Texas Instruments, Inc.

In low open area contact and via etches, endpoint detection has proven very challenging in manufacturing, despite apparent successes in research and development. In our current studies, we are looking into critical issues preventing successful implementation of endpoint detection in a manufacturing environment. In particular, we have characterized two major limitations to endpoint detection inherent in many oxide etching processes. 1) Wafer Edge Limitations - Depending on processing conditions, the wafer edge contributes between 1% to 6% open area to the etch, and thus cannot be neglected in the endpoint detection scheme for etches where the patterned area is <10% open area. 2) Interferometry Limitations - When using optical emission spectroscopy, reflections from the wafer surface and the top electrode can lead to a significant source of noise that is very difficult to remove and can easily lead to false identification of endpoint. In addition to looking at limitations inherent in typical processes, we have also quantitatively compared performance of various sensors that have been proposed for endpoint detection. S/N was characterized for 4 different levels of open area (100%, 20%, 0.7%, 0.14%) for optical emission spectroscopy (OES), residual gas analysis (RGA), and RF Impedance sensors. Our findings indicated that the RGA had the best S/N capability at 0.14% open area, but the simple monochromator OES system was a close second, with good capability at 0.7%. Lastly, we have compared performance of multivariate OES systems with single wavelength monochromator systems and found that the monochromator showed greater capability for low open area endpoint detection. After revisiting some of the multivariate algorithms, it was discovered that the S/N improvements previously claimed for multivariate algorithms have been overstated. In some cases multivariate algorithms can actually decrease S/N.

Dielectrics
Room 312 - Session DI+EL+MS-ThM

Ultrathin Dielectrics and Interfaces
Moderator: Y.J. Chabal, Bell Laboratories, Lucent Technologies

8:20am **DI+EL+MS-ThM1 Oxidation of Clean and H-passivated Silicon by Molecular and Atomic Oxygen**, ***X. Zhang,*** Rutgers University; *Y.J. Chabal,* Bell Laboratories, Lucent Technologies; *E. Garfunkel,* Rutgers University; *S.B. Christman, E.E. Chaban,* Bell Laboratories, Lucent Technologies

The need for uniform and ultra-thin silicon oxides in microelectronics requires a fundamental understanding of the initial oxidation of both clean and H-passivated (HF-etched) silicon in oxygen. We have undertaken a systematic infrared absorption study of molecular O@sub 2@ and atomic O oxidation of H-passivated flat and vicinal Si(111) and Si(100) surfaces. Using an IR transmission geometry for full access to Si-O stretch (900-1250 cm@super -1@) and Si-H bending (600-850 cm@super -1@) modes, we can directly observe the incorporation of oxygen even after H-desorption under ultra-high vacuum conditions. Furthermore, hydrogen at steps can be spectrally distinguished from H on terraces, thus making it possible to correlate the kinetics of H elimination with oxide formation as a function of surface structure. We find that upon 1 Torr exposure at 300@super o@C, the bonding of step hydrogen is preferentially altered on the H/Si(111) surface, with dihydride steps being the most reactive. Yet, the rate of oxidation does not scale with the step density, indicating that direct oxidation of terraces takes place simultaneously. For the Si(100) surface, we contrast the oxidation of the HF-etched (atomically rough surface) with that of the smooth H-Si(100)-(2x1) surface prepared in HHV and that of the clean Si(100)- (2x1) surface in order to extract the mechanism for molecular O@sub 2@ dissociation.

8:40am **DI+EL+MS-ThM2 New Oxidation Process Using Collimated Hyperthermal Ozone Beam**, ***T. Nishiguchi,*** *Y. Morikawa, M. Miyamoto,* Meidensha Corporation, Japan; *H. Nonaka, A. Kurokawa, S. Ichimura,* Electrotechnical Laboratory, Japan

As the electronic devices are scaled down, using more reactive process gas than molecular oxygen is required to fabricate an ultra-thin highly reliable Si dioxide film for the gate oxide in MOSFET. We used ozone as an oxidant gas and achieved the enhanced initial oxidation rate, resulting in lower temperature oxidation process. In our experiments using highly concentrated ozone gas, more than 3nm Si dioxide film was obtained within 30 minutes under the conditions of 873K of Si temperature and 10Pa of ozone pressure, where the oxidation hardly proceeds by molecular oxygen. In the present study, we carried out the laser ablation of solid ozone in order to obtain collimated ozone beam on the purpose of applying ozone beam to new oxidation processes such as local oxidation of patterned Si surface (e.g. oxidation of a bottom part of a trench). We irradiated a KrF pulsed excimer laser light to highly concentrated solidified ozone that was adsorbed on the sapphire plate cooled down to 30-60K by cryocooler in an UHV chamber. We could obtain collimated ozone beam (within 20° spread) whose supply (typically 10@super 16@ molecules per laser pulse), concentration (typically 70%) and translational energy (3eV maximum) were controlled through the laser ablation conditions such as the laser fluence. Not only the local oxidation but also even lower temperature process is expected using this high-translational-energy (hyperthermal) ozone beam. We will demonstrate the initial oxidation profile for the first 1000 laser shots by Auger Electron Spectroscopy and discuss the applicability of this ozone beam to the semiconductor process.

9:00am **DI+EL+MS-ThM3 Nondestructive Investigation of the Si/SiO2 Interface by Spectroscopic Ellipsometry, Reflectance Difference Spectroscopy, Second Harmonic Generation, and X-ray Photoelectron Spectroscopy**, ***J.F.T. Wang,*** *J.W. Keister, Y.M. Lee, G. Lucovsky, J.E. Rowe, D.E. Aspnes,* North Carolina State University

We report results of a systematic study with various nondestructive techniques of buried interfaces between Si and thin gate oxides thermally grown at 700C and rapid-thermal-annealed at temperatures to 900C. The objectives are to understand the optical properties, the step structure, and the nature of the chemical bonding of the interface and to determine the limits to which the various nondestructive probes, alone and in combination, can provide this information. We examine in particular data obtained as a function of heat treatment and surface orientation (miscuts 2, 4, 8, 10 degrees off (001) toward the nearest (111); (113); (111); and (110)), with emphasis on the vicinal (001) orientations. The RD spectra of all as-oxidized vicinal (001) samples decrease by nearly a factor of 5 for the 900C RTA, indicating step-density reduction and a net smoothing of the interface. Except for the 2 deg sample, which shows basically no signal, these spectra become essentially identical to the spectra of chemically etched, H-terminated vicinal (001) surfaces. All such spectra have the appearance of RD lineshapes obtained on (113) surfaces, which are nominally dominated by double-height steps. The ellipsometric data differ mainly in overlayer thickness, but interface information can be extracted through least-squares analysis assuming interface spectra of Si in amorphous and +1 and +2 charge states. To assist in this analysis we orthogonalize the fitting parameters to determine which combinations are best determined by the data. The results indicate that the best reference data are those obtained on H-terminated (111) surfaces. The interface XPS spectra become much more consistent after rapid thermal annealing, with the (001) and (111) spectra being dominated by Si in +2 and +1 charge states, respectively, as expected. This provides further evidence of a reduction in roughness with annealing.

9:20am **DI+EL+MS-ThM4 Core-level Photoemission of Interface States on SiO@sub 2@/Si: Substrate Orientation Effects**, ***J.E. Rowe,*** Army Research Office; *J.W. Keister, J.F.T. Wang,* North Carolina State University; *G.J. Jackson, T.E. Madey,* Rutgers University; *D.E. Aspnes,* North Carolina State University

High resolution soft X-ray photoelectron spectroscopy (SXPS) with synchrotron radiation is used to study the interface of mis-cut SiO@sub 2@/Si(100) [i.e. stepped interface] of device quality ultrathin gate oxides. Our studies were performed on thin oxides grown by thermal oxidation in pure O@sub 2@ at a temperature of 600@degree@C and pressure of ~760 Torr. Our data can be well described by five different Si species due to Si in different oxidation states which are usually labeled Si@super 0@, Si@super +1@, Si@super +2@, Si@super +3@, and Si@super +4@. We have studied a number of samples prepared as described above and find that the energies relative to the Si0 peak are 0.95 eV, 1.80 eV, 2.50 eV, and 4.00 eV for the Si@super +1@, Si@super +2@, Si@super +3@, and Si@super +4@ peaks respectively. For this study, we define the transition region as the region containing Si in intermediate oxidation states (Si@super +1@, Si@super +2@, Si@super +3@). We find a transition-region Si suboxide concentration of 1.3 x 10@super 15@ cm@super -2@ assuming an escape depth of ~7 @Ao@ at a photon energy of 200 eV for samples annealed after growth at temperatures of ~900 @degree@C . This transition region is that in excess of the density ~1 monolayer of Si@super +1@ expected for the most abrupt SiO@sub 2@/Si(111) interface in terms of the Si(111) layer density of 7.8 x 10@super 14@ cm@super -2@. The I@sub 1@ interface peak is largest for (111) and decreases substantially for (113), (110), and for stepped (100) substrates. The total interface density appears to be lowest for Si(100) with a modest step density introduced by a 2@degree@ mis-cut. The step-dependent behavior is consistent with that reported using second harmonic generation. The total concentration of suboxide derived from SXPS data is dependent on the uniformity of SiO@sub 2@ films as well as data modeling, i.e., fitting of the data; both will be discussed.

9:40am **DI+EL+MS-ThM5 Spectroscopic and Electrical Characterization of the Evolution of Chemical Oxides Into Ultrathin Gate Oxides**, ***J. Eng, Jr.,*** *R.L. Opila, J.M. Rosamilia, J. Sapjeta, Y.J. Chabal, B.E. Weir, P. Silverman, T. Boone, R.L. Masaitis, T. Sorsch, M.L. Green,* Bell Labs, Lucent Technologies

The goal of this study is to understand how the structure of wet chemical oxides change during oxidation, and to determine whether the quality of ultrathin oxides is sensitive to the type of of wet chemical treatments. Four wet chemical treatments were examined: 1. standard RCA, with an SC1 step (ammonium hydroxide and peroxide) followed by an SC2 step (hydrochloric acid and peroxide), 2. modified RCA, with an HF etch between the SC1 and SC2, 3. ozonated water, and 4. HF. X-ray photoelectron spectroscopy (XPS) and infrared spectroscopy (IR) have been used to probe the structure and composition of the wet chemical oxides. IR probes the long range order in the films, while XPS probes the local Si stoichiometry. Both techniques show that the ozone oxide has the highest quality. Despite large differences in the initial quality of the wet chemical oxides, rapid thermal oxidation of the chemical oxides produces oxide films that are spectroscopically similar. Electrical properties of the oxides will correlated with the spectroscopic studies.

10:00am **DI+EL+MS-ThM6 Studies on Accurate Determination of the Physical Thickness of nm Gate Oxides and its Correlation with the Electric Thickness**, ***D.W. Moon**, H.K. Kim, H.J. Lee, H.M. Jo,* Korea Research Institute of Standards and Science, Korea*; H.S. Jang, H. Hwang,* Kwangju Institute of Science and Technology, Korea

Accurate Determination of nm gate oxides is critical for the development of nanoelectronic devices as well as for CMOS device scaling beyond 100 nm. In semiconductor industries, the thickness of gate oxides has been measured by ellipsometry. However, the accuracy has been not evaluated especially for gate oxides thinner than 10 nm. Recently, TEM and spectrometric ellipsometry(SE) have been used to measure the physical thickness of nm gate oxides and the electric methods such as I-V an C-V have been modified to include quantum effects. In this work, to estimate the uncertainty and improve the accuracy of the methods used for gate oxides thickness determination, TEM, SE and Medium Energy Ion Scattering Spectroscopy(MEIS) were used to determined the physical thickness of 6 gate oxides from 9 nm thick to 1.5 nm native oxide thick. MEIS can analyze the composition and structure of ultrathin films with atomic layer depth resolution. It was investigated that MEIS can be a reference for gate oxide thickness determination down to 1-2 nm. The difference of the physical thickness determined with TEM, SE and MEIS were discussed and compared with the electric thickness determined by I-V and C-V methods. For the gate oxides studied, the thickness determined by the Si MEIS peak was 1.5 nm thicker than that by the O MEIS peak. The thickness determined by SE and TEM was between the two values, while SE gave ~0.5 nm higher thickness than TEM. However, with the interlayer thickness, TEM thickness approached that of Si MEIS peak thickness. The electric thickness determined with I-V and C-V was close to that of Si MEIS peak thickness within 0.2nm. The thickness by SE is quite sensitive to the refractive index value used for fitting, especially for gate oxides thinner than 5nm. Based on this multi-disciplinary approach, it will be discussed how to provide standards for nm gate oxides approaching the limit of CMOS and how to transfer the standards to SE which is widely used in semiconductor process lines.

10:20am **DI+EL+MS-ThM7 Bonding of Nitrogen in Silicon Oxynitride Films**, ***R.L. Opila**, J. Eng, Jr., Y.J. Chabal, K.T. Queeney,* Bell Laboratories, Lucent Technologies*; J.P. Chang,* University of California, Los Angeles

Silicon oxynitride is a promising candidate to replace silicon dioxide in the next generation of microelectronic devices, but key aspects of the nitrogen chemistry in this material remain unresolved. This talk describes a twofold approach for understanding nitrogen bonding in these materials. The first approach employs surface analytical techniques, including photoelectron spectroscopy, infrared spectroscopy and near edge x-ray absorption fine structure, to study how oynitride precursors, suchas as nitric acid, nitromethane, and ammonia, react with silicon surfaces. The second approach uses the previous analytical techniques, along with electron spin resonance spectroscopy, to compare the nitrogen bonding states in silicon oxynitride and silicon nitride films prepared by thermal growth and ion implantation. Significant differences in the distribution of nitrogen bonding states and point defects are observed and correlated with the method of film preparation.

10:40am **DI+EL+MS-ThM8 Photoemission Investigation of Nitrogen Incorporation at the Si/SiO@sub 2@ Interface**, *J.E. Rowe,* Army Research Office*; **J.W. Keister,*** North Carolina State University

Monolayer incorporation of nitrogen at the Si/SiO@sub 2@ interface enhances the reliability and electrical characteristics of this nearly perfect interface for ultrathin SiO2 layers.@footnote 1@ In this paper we demonstrate that the Si(100)/SiO@sub 2@ interface is chemically sensitive to the nitrogen concentration. The nitrogen (1s) Soft X-ray Photoemission Spectroscopy (SXPS) peak was measured for varying degrees of N incorporation using the Advanced Light Source synchrotron at LBL National Lab. The broad width of the N(1s) SXPS peak lineshape is consistent with a large degree of final-state, Gaussian phonon broadening, and is comparable to O(1s) line. However, unlike the O(1s) line which is not especially chemically sensitive, the N(1s) line shows a clearly measureable, interface peak shift@footnote 2@ with increasing N incorporation. The average interface peak binding energy is ~0.75 eV greater than that recently reported for thick "bulk" films of Si3N4 with Al-K" XPS. To a lesser degree, the peak shape is seen to change as well. In particular, the peak width minimizes near to the value ~1.0 ML N incorporation, which is also the level at which devices interfaces perform best electrically. @FootnoteText@ @footnote 1@ G. Lucovsky, A. Banerjee, B. Hinds, B. Claflin, K. Koh, H. Yang. J. Vac. Sci Technol. B 15(4) 1074-1079 (1997). @footnote 2@ J. W. Keister, J. E. Rowe, J. J. Kolodziej, H. Niimi, H.-S. Tao, T. E. Madey, G. Lucovsky. J. Vac. Sci Technol. A 17(4) 1250-1257 (1999).

11:00am **DI+EL+MS-ThM9 Investigation of Fluorine in Dry Ultrathin Silicon Oxides**, ***G. Vereecke**, E. Röhr, R.J. Carter, T. Conard, H. Dewitte, M.M. Heyns,* IMEC, Belgium

As critical dimensions of integrated circuits continue to decrease, insulators with dielectric constants higher than silicon dioxide will be introduced in capacitors and transistors. However an ultrathin (< 1 nm) silicon oxide layer will generally be needed at the interface between Si and high-k layers. In cluster tools integrating surface preparation and dielectric deposition, vapor HF chemistries are envisaged to etch the native oxide prior to oxide growth. This HF etch leaves F on the surface of the Si wafer, which gets incorporated into the growing oxide. In addition, the silicon subsurface has also been proposed as a source of the F found in these oxides. The presence of F may be beneficial or detrimental for the properties of these layers depending on application, F location, and layer thickness. We have evaluated the sources of F in ultrathin oxides grown by UV/O2 at room temperature in an experimental vapor phase cleaning tool. Surface pretreatment was either by in-situ HF/methanol vapor process or by ex-situ wet HF dip followed by a DIW rinse. Evidence was found for F cross-contamination from the tool gaspanel when the HF etch step was performed in-situ. After correcting for this, F atomic concentrations in oxides grown on vapour HF and wet HF treated surfaces were of about 5 % and 2 %, respectively. The former would lower the dielectric constant of the layer if homogeneously distributed. The level of F contributed by the subsurface was estimated with oxides grown on wet HF treated surfaces in a specially built quartz chamber with no F contamination. No F was detected in these oxides, which indicates that the level of subsurface F is lower than previously reported. Ultrathin oxides continued to grow when exposed to air. This raises concern about their stability during the deposition and annealing of high-k layers. XPS results suggest that this is related to the exchange of labile F groups in the films.

11:20am **DI+EL+MS-ThM10 Studies on Electrical Properties of Ultrathin Oxides of Silicon Grown by Wet Oxidation at Low Water Vapor Pressure**, ***V.K. Bhat**, K.N. Bhat, A. Subrahmanyam,* Indian Institute of Technology, India

The rapid downscaling of the device dimension has increased the interest in the ultrathin (< 5 nm) oxides of silicon. Ultrathin oxides with thickness uniformity and good electrical properties are required for the silicon submicron devices. In general, the dry oxidation is being followed to grow these ultarthin oxides. Wet oxidation is not considered for the growth of ultrathin oxides of silicon because of the following reasons: i) high growth rate associated with the conventional wet oxidation at 1 atm. water vapor pressure and ii) large density of electron trapping centres present in the wet oxide. In the present study we report the results on the electrical properties of ultrathin oxides of silicon grown by wet oxidation at low (0.04 atm.) water vapor pressure. Ultrathin oxide of silicon is grown at 900°C on n-type single crystal silicon, single side polished, (100) oriented and having 1-10 @ohm@ cm resistivity (procured from M/s Wacker GmbH, Germany). The grown ultrathin oxides are characterized for their electrical properties by fabricating MOS tunnel diodes (aluminum is thermally evaported with a metal mask on to the ultrathin oxide). The capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) charcteristics of the MOS tunnel diodes are studied. The interafce state density (D@sub it@) and the density of the fixed oxide charge (Q@sub f@) are being calculated. The grown ultrathin oxide thickness is estimated from the measured C-V characteristics and are in the range 2.5-5.0 nm. The oxide growth rate is found to be linear. The charge trapping characteristics of the ultrathin oxides are studied by using consatnt current stress (CCS) technique. The decrease in the gate voltage is observed with the stress time. This observation may be attributed to the positive charge trapping in the oxide during the CCS. The charge trapping is found to be oxide thickness dependent and it decreases with the decrase in the oxide thickness.

11:40am **DI+EL+MS-ThM11 Properties of SiO@sub 2@ Thin Films Deposited at Low Temperature on SiGe and Si Samples in O@sub 2@/TEOS Helicon Plasmas**, ***A. Goullet**, D. Goghero, V. Fernandez, A. Granier,* Institut des Matériaux Jean Rouxel, France*; F. Meyer,* Université de Paris XI, France*; G. Turban,* Institut des Matériaux Jean Rouxel, France

Silicon dioxide thin films are deposited at low pressure (< 5mTorr) and temperature (<200° C) on Si@sub 1-x@Ge@sub x@ epi-layers and silicon substrates in oxygen rich O@sub 2@/TEOS helicon plasmas. The growth of SiO@sub 2@ films and the evolution of the interfacial layer under applied radio frequency bias voltage (0, -100, -200 V) are investigated using a UV-

Visible phase modulated ellipsometer (1.5-5 eV). The structural properties of the films are studied using infrared transmission spectroscopy, wet chemical etching and spectroscopic ellipsometry. Very thin (<10 nm) SiO@sub 2@ films deposited in the same conditions are investigated by X-ray photoelectron spectroscopy and spectroscopic ellipsometry to gain better insight of the oxide/semiconductor interface. The ion energy is found to be a significant parameter both for film properties and deposition rate. Use of radio frequency bias is effective in producing high quality SiO@sub 2@ films but an amorphized transition layer is detected in this case as evidenced by ellipsometric data modeling. The increase in the ion energy is also responsible for the presence of an additional oxidation state which appears on the Ge 3d XPS peak. Complementary capacitive C(V) measurements of grown oxides have been performed using metal-oxide-semiconductor samples. An increase in the fixed oxide charge and interface state densities as a function of the applied bias voltage is observed for silicon substrates whereas the electrical properties of the films deposited on Si@sub 1-x@Ge@sub x@ are rather insensitive to the deposition conditions.

Manufacturing Science and Technology
Room 304 - Session MS-ThM

Advanced Modeling and Control for IC Manufacturing

Moderator: S.S. Shankar, Intel Corporation

8:20am **MS-ThM1 Simulation of Transient Enhanced Diffusion of B in Si**, ***G.S. Hwang***, *W.A. Goddard III,* California Institute of Technology

Ever shrinking device dimensions requires the formation of ultrashallow junctions with high concentrations of electrically active dopants and box-like profiles in order to maximize drive currents while minimizing short channel effects. To control such junction properties it is necessary to understand quantitatively (i) the underlying mechanisms of transient enhanced diffusion (TED) of dopants and (ii) the dynamics of defect/dopant clustering during implantation and postimplantation annealing. We present a systematic approach to address such issues in which we combine (i) kinetic Monte Carlo (kMC) mesoscale simulations capable of describing the length and time scales of TED with (ii) quantum mechanics [density functional theory (DFT)] calculations of the fundamental atomic level processes and (iii) experimental validation. In recent years much effort has been devoted to understanding the TED of B in Si; however, most studies have been performed using moderate energy (~40 keV) Si@super +@ implants into MBE-grown B-doped layers. The dominant mechanisms of the B TED based on this previous work may not be dominant for the low energy (10@super 20@ cm@super -3@) inherent to ultrashallow junction fabrication. In this talk, we will present (i) new mechanisms of B clustering and (ii) strain-induced defect-defect and defect-dopant interactions, and discuss how crucial it is to have such detailed information for accurately predicting the doping profiles in ultrashallow junction processing. We will also address several unresolved issues in the low-energy and high-concentration regime: (i) the validity of '+1' model, (ii) the surface proximity effect, and (iii) the role of defect/dopant clustering in determining junction profiles.

8:40am **MS-ThM2 New Physics for Models of Transient Enhanced Diffusion**, *M.Y.L. Jung,* ***E.G. Seebauer***, University of Illinois, Urbana-Champaign

As device dimensions continue to shrink, the constraints on processing imposed by Mother Nature become ever more stringent. The optimization of chemical kinetics and mass transport is therefore playing an increasingly important role in defining and widening process windows. Here we discuss TCAD modeling of transient-enhanced diffusion (TED) after ion implantation during ultrashallow junction formation by rapid thermal annealing. TED has long been modeled using a large set of reaction-diffusion equations for the dopant, point defects, and extended defects. However, current commercial and public-domain SUPREM-based software mishandles several important aspects of the reaction-diffusion network. For example, many of the diffusivities are inappropriately parameterized. Also, the software lacks a self-consistent, time-dependent treatment of Poisson's equation and therefore miscalculates the electric-field-driven drift of charged defects. There are further problems: even the best TED models neglect important effects of the nearby free surface and of intense illumination. For example, there is no incorporation of near-surface band bending, of changes in charged defect concentration during illumination, or of enhancement of point defect motion though local energy dumping by e-h recombination. This talk outlines how such effects can be incorporated and discusses conditions under which they are likely to be important.

9:00am **MS-ThM3 Fast-Ramp Annealing for Reducing Implant-Induced Transient Enhanced Diffusion**, ***M.Y.L. Jung***, *R. Gunawan, R.D. Braatz, E.G. Seebauer,* University of Illinois, Urbana-Champaign

Some experimental evidence has accumulated in recent years to support the use of "spike anneal" temperature trajectories with very fast heating and cooling rates for making ultrashallow junctions by ion implantation. Improved device properties have been claimed using heating rates of 400 C/s or more. This procedure supposedly optimizes junction depth and sheet resistance by reducing transient-enhanced diffusion (TED) of the dopant. However, the theoretical justification for using such fast ramps has been weak. Since the design and use of fast-ramp annealing tools will require substantial investments by equipment manufacturers and IC manufacturers alike, it is important to confirm by TCAD modeling the existence and potential magnitude of such effects. TED has long been modeled using a large set of reaction-diffusion equations for the dopant, point defects, and extended defects. However, current commercial and public-domain SUPREM-based software mishandles or ignores several important aspects of the reaction-diffusion network. We briefly discuss how we have fixed these problems, focusing in particular how proper incorporation of surface oxidation or nitridation kinetics closely couples the gas ambient in the annealer to dopant motion down near the junction within the Si bulk. We then show how variations in heating and cooling rates can be used to favor or disfavor important reaction-diffusion pathways within the overall system of effects that governs TED. In particular, we point out how the widely-used contant-temperature annealing step near 500 C for pyrometer calibration actually influences subsequent profile evolution in a profound way.

9:20am **MS-ThM4 Dynamic Simulation: Guiding Manufacturing from Process Mechanisms to Factory Operations**, ***G.W. Rubloff***, University of Maryland **INVITED**

Dynamics plays a critical role in the behavior and performance of semiconductor manufacturing from the unit process level to full factory operations, yet major gaps exist in our ability to simulate the consequences of this dynamics. At the process level, process models can provide a reasonable description of steady-state process behavior, but the realities of semiconductor equipment dictate that both total process times and thermal histories depend on the dynamics of the equipment and control systems, as well as on the raw process itself. We have developed physically-based dynamic simulation strategies which accurately reflect time-dependent behavior of equipment, process, sensor, and control systems, and we have used them to understand and optimize equipment systems and process recipes. Another dimension of dynamics appears in the behavior of cluster tools, where the tool architecture, process module populations, and scheduling algorithms add further dynamics to tool behavior. We have integrated reduced-order process models, reflecting dynamic unit process simulations, with discrete event simulations of cluster tool performance to enable co-optimization of process recipes, cluster tool configurations, and their scheduling algorithms. Finally, we have incorporated these integrated models into factory-level operational models to facilitate the evaluation of factory-level performance as a function of process, equipment, and logistics choices. These simulation strategies seem attractive in terms of their ability to represent dynamics, from continuous parameter dynamic recipes at the unit process level, to discrete-event dynamics associated with scheduling and throughput at the factory level.

10:00am **MS-ThM6 Integrated Metrology with Run to Run Control**, ***P.R. Solomon***, *P.A. Rosenthal, S. Bosch-Charpenay, J. Xu, W. Zhang,* On-Line Technologies, Inc. **INVITED**

The semiconductor industry is moving to adopt copper/low-k interconnect technology, smaller critical dimensions and 300 mm wafers. Many of these changes require tightening of the process specifications. Introducing these changes while maintaining product quality and reducing costs is a formidable challenge. Especially important are low-k dielectrics, chemically amplified resist, FSG and BPSG films that require control of their chemical composition as well as thickness. Integrated metrology with run-to-run control can facilitate the introduction of these new technologies because of its ability to improve process control while at the same time reducing manufacturing costs. Such benefits can be achieved for most current process steps as well. This paper will review some early success stories for Epi silicon and CMP processes. The integrated metrology for Epi employs an FTIR based film thickness monitor with model based analysis, integrated onto the cooldown chamber of the cluster tool for 100 % multi-point

measurement and control. The FTIR is also applicable to the monitoring of thin film chemical composition. While FTIR has been widely used in R&D environments, its application to mainstream production metrology and process monitoring on product wafers has historically been limited by: 1) the optical complexity of film stacks used in production, 2) sample-dependent backside reflection artifacts caused by substrates which are transparent in the infrared, and 3) the lack of robust models of the chemically variable optical constants of modern IC materials. These limitations have been eliminated in a series of recent FTIR technology advances. The paper considers these recent advances, how the technology is integrated with the processing tools, the operation of the system, the improvement in the product and the cost of ownership. The paper will also examine the metrology available for integration and the future course for making such technology widely available, including standards for integration and methods for delivering the technology.

10:40am **MS-ThM8 W CVD Thickness Metrology and Run-to-Run Control using Mass Spectrometry**, ***Y. Xu***, *T. Gougousi, R. Sreenivasan, G.W. Rubloff, J.N. Kidder, E. Zafiriou,* University of Maryland

For a H2/WF6 CVD process for selective W deposition in an Ulvac cluster tool, mass spectrometry has been used to observe HF product generation and H2 depletion. HF signal was proportional to the deposited W thickness to about 7%, providing an in-situ thickness metrology as a candidate to drive run-to-run thickness control. To assess this possibility, a systematic temperature drift of -50C per wafer was introduced, which in the absence of control would cause the film thickness to decrease by 40-50% over a ten wafer lot. Using a robust control algorithm to maintain a constant integrated HF mass spec signal by adjusting the nominal deposition time, the effect of the temperature drift on deposited film thickness was largely compensated, and the W film thickness was maintained within 10% of the target value. The metrology accuracy was limited by the low (about 3%) reactant conversion rate of the process, coupled with significant background signals. Since blanket W CVD processes as employed in manufacturing achieve much higher conversion efficiencies (40-50%), we anticipate considerable improvement in the efficacy of metrology and control in these situations. Our results, and their projection to realistic manufacturing scenarios, present an encouraging opportunity to use in-situ chemical sensing for process metrology and control.

11:00am **MS-ThM9 Feedback Control of Morphology During III-V Semiconductor Growth by Molecular Beam Epitaxy@footnote 1@**, ***R.L. Kosut***, *J.L. Ebert, S. Ghosal,* SC Solutions*; R. Caflisch,* University of California, Los Angeles*; M. Gyure, J.J. Zinck,* HRL Laboratories

This paper addresses the modeling and control of epitaxial growth of III-V semiconductor material by Molecular Beam Epitaxy. In layer-by-layer growth mode, oscillations and envelope decay in the specular intensity of the reflection high energy electron diffraction (RHEED) pattern have been correlated to the instantaneous density of steps on the surface. This allows for the possibility of in situ monitoring and control of surface morphology during growth. A control algorithm and strategy was first developed using a KMC simulation model of III-V growth together with dynamic thermal models of the effusion cells and cracker valves. The strategy discovered from the simulations was to control growth layer-to-layer which turns out to have two important features: (1) it is very robust to chamber variations and uncertainties, and (2) the resulting form of the system is well modeled as a discrete-time system where sample times are replaced by layer number. There is a vast body of control theory which can be applied to such systems. The control was implemented on the MBE system to control RHEED oscillations and decay rates in real-time during III-V growth in HRL Laboratories MBE chamber. The RHEED signals were used to estimate oscillation period which was compared to a reference and the error was used in a control algorithm to adjust, in real-time, the set-point temperature of the III material effusion cell. The RHEED signals were also used to estimate oscillation decay and then used to adjust the V material cracker valve opening. Simulations compared well with experimental data in both open and closed loop. Investigations are currently under way to use a photoemission (PE) sensor in place of the RHEED sensor. Hopefully results will be available at the time of the AVS conference. @FootnoteText@ @footnote 1@ Research supported by DARPA, Applied Computation & Mathematics Program.

11:20am **MS-ThM10 Data Requirements and Communication Issues for Advanced Process Control**, ***R.J.M. Markle***, *E.C.J. Coss, Jr,* AMD **INVITED**

Data streams and communication issues are the most critical areas for successful Advanced Process Control (APC) programs. These areas are vital for both APC run-to-run controllers and Fault Detection and Classification (FDC) systems used for high volume manufacturing applications in the semiconductor industry. All APC systems rely on data streams to make their process changes, to keep the process on target and in control, and to otherwise signal a need for engineering involvement to make similar corrective actions. The access to, communication of, and reliability and integrity of these data streams are essential to all APC programs. APC run-to-run controllers use the data to make changes in the process. FDC systems focus on predicting pending equipment- or process- related problems or detecting them quickly when they occur. The inability to access the needed data stream can prohibit the use of APC run-to-run controllers or FDC systems on critical process operations. Worse yet, the use of unreliable or corrupted data can cause undesirable consequences. In order to better capitalize on the improvements demonstrated with APC run-to-run controllers and FDC systems, end users have often had to create their own communication and data processing methods. The first decade of the 21st century will place increased demands on process and metrology equipment manufacturers, APC software and hardware suppliers, and APC programmers. Improvements in these areas through the use of industry standards and best known methods could greatly accelerate the APC field. Wafer-to-wafer and within wafer process control could be essential for 300 millimeter wafer and large flat panel processing will need these improvements. We will discuss examples that Advanced Micro Devices (AMD) experienced in Fab25 within the past year. The case studies relate to complex but necessary methods to get the data we need for a FDC system and the role of metrology data on APC run-to-run controllers. Data and communication requirements for the next three to five years will also be discussed. The increased demands on current process and metrology systems will increase as we begin to use new and alternative technologies to support more advanced APC strategies.

Dielectrics
Room 312 - Session DI+EL+MS-ThA

High K Dielectrics: Perovskites
Moderator: J.N. Kidder, University of Maryland

2:00pm **DI+EL+MS-ThA1 High Density Thin Film Ferroelectric Nonvolatile Memories**, ***R. Ramesh,*** University of Maryland **INVITED**

Over the past two years, we have focused considerable effort on understanding the deposition and characterization of conducting barrier layers for the direct integration of ferroelectric capacitors on a poly-Si plug. Our specific focus has been on the materials science of the barrier layers to understand the role of crystallinity and process parameters on the structural and chemical integrity of the barrier layers during the subsequent growth of the ferroelectric capacitor stack. We are using the PZT system with conducting oxide electrodes as a prototypical test system for which at least two different conducting barrier materials systems have been successfully developed. Using both epitaxial and polycrystalline capacitors on these conducting barriers as test vehicles, we have been carrying out systematic studies on the effect of composition, point defect chemistry, strain and other processing variables on the structural integrity and ferroelectric properties. A novel aspect of our work is the use of scanning electric force microscopy techniques to understand the microscopic influence of film microstructure on the ferroelectric properties. In this presentation, we will present results of our progress on the process integration, device properties, specifically, polarization switching and relaxation dynamics and microscopic observations of ferroelectric properties and time dependent changes ; stress effects on fundamental properties.This work is supported by the NSF-MRSEC under Grant No. DMR- 96-32521 and by Bellcore.

2:40pm **DI+EL+MS-ThA3 Process Window Extension of TiN Diffusion Barrier using Pre-oxidation of Ru and RuO@sub x@ Film for (Ba,Sr)TiO@sub 3@ Dielectric Film**, *H.J. Kim, S. Kim,* Hyundai Electronics Industries Co. Ltd., Korea

(Ba,Sr)TiO@sub 3@(BST) thin film and other high dielectric oxides have attracted considerable attention due to their possible application in dynamic random access memories. However, serious integration issues are faced with in many cases because BST films need to be grown at rather high deposition or post-annealing temperatures of above 600°C in an oxidizing ambient. Deterioration of capacitor performance may result from interdiffusion and oxidation. Therefore, a diffusion barrier for oxygen should be developed for high-density DRAM device. In order to extend the process window of conventional sputtered TiN diffusion barrier and find out a proper electrode, in this experiment, the effect of pre-annealing method on the oxidation behavior of TiN barrier during 2 step annealing for BST dielectric film. Rapid thermal annealing in oxygen ambient (RTO) and N@sub 2@O plasma oxidation was respectively introduced to form a thin RuO@sub x@ layer and bind between oxygen and Ru at the surface of each Ru and RuO@sub x@ film. It is expected that a thin RuO@sub x@ layer be formed at the surface of each film by RTO and N@sub 2@O plasma. This can be retarded the oxygen indiffusion through Ru and RuO@sub x@ layer at high temperature due to complex diffusion paths and strongly stuffed along the grain boundaries as well as matrix. Two steps annealing for BST dielectric film is recently introduced to minimize the oxidation of diffusion barrier. In this work, a role of thin RuO@sub x@ oxidized layer formed at the surface of each Ru and RuO@sub x@ film by different pre-annealing methods prepared with/without BST deposition is investigated during two steps annealing.

3:00pm **DI+EL+MS-ThA4 Atomic Polarization and Screening Charge by Variable Temperature Scanning Probe Microscopy of Ferroelectric Surfaces**, ***S.V. Kalinin,*** *D.A. Bonnell,* University of Pennsylvania

Atomic force microscopy (AFM), electrostatic force microscopy (EFM), scanning surface potential microscopy (SSPM) and piezoresponse imaging (PRI) are applied to the BaTiO3 (100) phase transition. The imaging mechanism for non-contact microscopies (EFM and SSPM) based on an analytical solution for potential and field above the surface is discussed. The PRI imaging mechanism on a ferroelectric surface is analyzed in terms of the solution of the combined electrostatic-piezoelectric indentation problem. The relationship between SPM signal and screened and unscreened charge density is established. Quantification of force and force gradient-distance dependencies indicate that polarization bound charge is screened on this surface when imaged in ambient environments. The absolute value of the measured potential difference between domains of opposite polarity suggests that surface adsorbates play the governing role in surface potential. This conclusion is corroborated by a direct measurement of the phase transition and by observations of domain wall motion. The influence of tip shape effects and mobile surface charges on effective domain wall width is also discussed. The contribution of electrostatic forces to piezoresponse contrast is extracted from force-distance measurements and its influence of the local hysteresis loops is estimated. Considerations regarding the polarization switching by the tip are presented. Based on the experimental observations for this and other systems the dominant role of electromechanical vs. electrostatic effects in PRI imaging mechanism is established.

3:20pm **DI+EL+MS-ThA5 Film-formation Mechanisms, Microstructure, and Properties of BST Thin Films Grown By MOCVD**, ***Y. Gao,*** Pacific Northwest National Laboratory **INVITED**

A review of MOCVD BST thin films will be presented, focusing on precursor chemistry, film-formation mechanisms, and relationship between film processing, microstructure and dielectric properties. In particular, the precursor chemistry and film-formation r eactions have been studied using isotopic labeling experiments (@super 18@O@sub 2@). The precursor chemistry was found to strongly depend on substrate materials. In an oxygen ambient, at least four different reaction processes involved the removal of carb on from the precursor ligands on oxide covered Pt(111). Time-of-flight secondary ion mass spectrometry reveals both M@super 18@O and M@super 16@O (M= Ba, Sr, Ti) in the BST films, indicating that the oxygen in the BST films originates from both the gas ph ase oxidants (@super 18@O), and the precursor ligands (@super 16@O). The ligand substitution by gas phase O@sub 2@ plays a more prominent role in the film-formation at lower temperatures. On the other hand, the reactive oxygen radicals produced by micr owave plasma involved more in breaking the O-C bonds than substituting the precursor ligands for the film formation, resulting in larger surface roughness. Use of the 50%@super 18@O@sub 2@-50%N@sub 2@@super 16@O mixture results in a reduction of @super 18@O incorporation in the BST films, indicative of the direct involvement of N@sub 2@O in the film-formation reactions. The mechanistic studies are essential for understanding the BST precursor properties, and provide useful information to correlate the fil m m icrostructure, step coverage, and dielectric properties with the precursor properties. In addition, the study shows that precursor reactivities strongly affect the step coverage on the 3D structure, but little effect on the microstructure, surface morphology, and dielectric properties of the stoichiometric BST films. These properties strongly depend on the film composition, substrate material, and growth temperature.

4:00pm **DI+EL+MS-ThA7 Epitaxial (Ba,Sr)TiO@sub 3@ on MgO for Room Temperature Microwave Phase Shifters**, ***C.L. Chen,*** *J. Shen, S.Y. Chen, C.W. Chu,* University of Houston*; F.W. Van Keuls, F. Miranda,* NASA Glenn Research Center*; J.C. Jiang,* Louisiana State University

Single crystalline ferroelectric Ba@sub 0.6@Sr@sub 0.4@TiO@sub 3@ thin films were epitaxially grown on (001) MgO by using pulsed laser ablation. Microstructure studies from x-ray diffraction and electron microscopy suggest that the as-grown films are c-axis oriented with their interface relationship of @sub BSTO@//@sub MO@. Edge dislocations were found through the entire interface in every 8 unit cell length. Microwave property measurements indicated that the room temperature coupled microwave phase shifter have achieved with phase shift over 200@super o@ at 23.675 GHz and a figure of Merit of about 55@super o@/dB. The room temperature dielectric constant and loss tangent were found to be 1688 and 0.008 and the tunability was 33% with 2.5V/µm. The result suggests that the performance of microwave phase shifter based on the epitaxial ferroelectric thin films on (001) MgO are closed to the practical applications in the wireless rf communications.

4:20pm **DI+EL+MS-ThA8 High Temperature Etch Processing for FeRAM MFM Capacitor Stack Fabrication**, ***L.G. Jerde,*** *A. Cofer, R.A. Ditizio, S. Marks, J.A. Meyer, K.A. Olson, S.P. DeOrnellas,* Tegal Corporation

The unique materials utilized in FeRAM MFM capacitor stacks present numerous integrated device fabrication challenges, particularly in the patterning of these materials and the capacitor stacks that utilize them. Many of these patterning challenges are due to the intrinsic involatility of the reaction products formed when etching the elemental constituents of the FeRAM materials (i.e., Pt, Ir, Pb, Zr, Sr and Bi). These challenges have been successfully met for several years by utilizing photoresist etch masks in conjunction with the plasma etch technologies of low pressure, high density and dual frequency. While this technological approach is extendible

for the foreseeable future of FeRAM capacitor stack definition, the intrinsic involatility of their etch reaction products has recently sparked wide spread interest in utilizing high temperature etch processes to meet the as yet undefined future requirements for these applications. Although there are benefits to this high temperature approach, there are also risks. Among these risks are a number of key considerations that must be dealt with to successfully develop and implement high temperature etch process solutions for FeRAM applications. The first set of these considerations is related to the requirement that the etch tool provides reliable wafer, as opposed to wafer chuck, temperature and temperature uniformity control. In view of the industry trend toward single mask, full stack processes, another set of considerations is the requirement that the etch tool be able to rapidly vary the wafer temperature to accommodate the optimum temperature for each of the FeRAM materials being used. Yet another set of considerations are those related to wafer temperature limitations imposed by the Perovskite structure transition temperature, device damage and thermal budget. We will discuss and illustrate these considerations and present selected high temperature etch process results for various FeRAM films and stacks.

Manufacturing Science and Technology
Room 304 - Session MS-ThA

Advanced Modeling for IC Manufacturing

Moderator: E.G. Seebauer, University of Illinois, Urbana-Champaign

2:00pm **MS-ThA1 Challenges in Modeling & Simulation of Semiconductor Equipment & Processes**, ***A.K. Das,*** Applied Materials Inc. **INVITED**

Modeling & simulation of semiconductor manufacturing equipment & processes is an inherently multi-disciplinary effort drawing from such diverse fields as plasma physics/chemistry and heat and mass transfer. Over the past few years, significant strides have been made to address and incorporate several of these phenomena, and enable optimization of chamber geometry and processes through modeling. However, many of these physical phenomena occuring in processing equipment are not even well understood or characterized. Obtaining self-consistent models that combine the influences of different phenomena or different aspects of processes is perhaps the major hurdle between where we are now and taking comprehensive reactor models (or the Virtual Reactor) mainstream. There are several issues that must be resolved before comprehensive reactor models may become commonplace. The computer model must be able to handle stiff chemistry-equations and the resulting numerical convergence problems. In plasma modeling, the sheath must be resolved properly to predict the ion flux and energy at the wafer surface. The extension of fluid models into the transition regime must be incorporated in the commercial codes. Finally ways must be explored to combine the reactor level model with the device/feature level. Currently setting up a model may be very time-consuming due to the lack of smart grid generation tools. The proliferation of modeling to the common engineer cannot happen without streamlining and minimizing the grid-generation effort. Lastly, there is a lack of fundamental or often tool-specific data necessary to accurately simulate these processes. Most of the reaction mechanisms/pathways of relevance to real processes are not well understood. A long-term sustained research effort is required from chip-makers, equipment companies, academia, national laboratories and commercial software developers to overcome these shortcomings.

2:40pm **MS-ThA3 Modeling of Oxide CMP and Polish Pad Conditioning**, ***L. Jiang,*** Intel Corp., US*; H. Simka, S.S. Shankar, J. Su, K. Kumar, V. Murali,* Intel Corp.

A model for the mechanical and chemical aspects of oxide CMP is presented. We combined both contact mechanics and slurry flow in a physical model (Jiang & Shankar 1999) and compared the simulation results to recent studies on oxide CMP. Pad asperity deformation and slurry flow between asperities are modeled simultaneously. Dissolution and polish rates of oxide are modeled based on silica hydrolysis kinetics and calibrated with experimental data. Mechanisms of pad glazing and conditioning effect on polish rate are also discussed with a review of literature data. Pad glazing is a result of mechanical (cyclic polish stress) and chemical actions (oxidation of surface during polish). Pad degradation effects on polish rate over the wafer scale are predicted by combining pad fatigue model with mechanics/flow simulations. Relative motions between pad, wafer, and individual conditioner heads are simulated to predict pad conditioning effectiveness and pad age.

3:00pm **MS-ThA4 Mechanical Properties of a Cu-Ta Interface by Molecular Dynamics**, *P. Heino,* ***E. Ristolainen,*** Tampere University of Technology, Finland

During last few years, the electrical and mechanical properties of copper have received a lot of interest in the electronics community, mainly because of its low electrical resistance. Last year at AVS1999@footnote 1@ we discussed mechanical properties of nanoscale copper connection and concentrated on pure copper. In this work we study the microstructure and strength of the copper interface. To prevent diffusion of copper into silicon, a barrier is needed. Furthermore, the barrier-copper system should be immiscible. It seems that tantalum is used most often as a barrier metal, and it has the needed properties. Here we study the copper-tantalum interface by means of molecular dynamics method and embedded atom potential. In the model the cross term potential has been optimized to reproduce the experimental (small and positive) heat of alloy formation. The interface is formed by depositing Cu on different single crystal Ta surfaces. The microstructure and properties under shear of the resulting interface are analyzed. @FootnoteText@@footnote 1@P. Heino, P. Holloway and E. Ristolainen: Strength of Nanoscale Copper Under Shear, Accepted for publication, J. Vac. Sci. Tech. A (2000).

3:20pm **MS-ThA5 Integrating Process Models, Equipment Logistics, and Factory Flow for Manufacturing Systems Optimization**, ***L. Henn-Lecordier,*** University of Maryland, US*; M.-Q. Nguyen, B. Conaghan, P. Mellacheruvu, J.W. Herrmann, G.W. Rubloff,* University of Maryland

Technology change, yield learning, and market shifts all produce notable factory dynamics, yet anticipating the operational consequences of process changes and optimizing the overall system remains largely an ad hoc procedure. We have developed a heterogeneous simulation environment (HSE) which integrates process and operational dynamics from the unit process to full factory flow. Process models are incorporated as response surfaces which determine cycle times in corresponding equipment modules. In turn, the operational behavior of multiple modules on cluster tools is investigated through discrete event simulation for specific cluster tool architecture, module population, and scheduling algorithms. Finally, process and cluster tool models are incorporated into factory-level discrete event simulations (Factory Explorer). Management of process, equipment, and factory parameters, as well as model execution, is carried out through a simulation supervisor and its graphical user interface. These integrated models enable tradeoff analysis involving specific process parameters, cluster tool configuration and logistics, and factory flow as a function of tool populations. We have studied the specific example of a W plug process sequence, involving clean, PVD TiN liner deposition, and W CVD fill. Results indicate notable cycle time advantage for individualized cluster tool sequencing optimized for the chosen process parameters, as compared to using routine dispatching rules. The HSE also reveals the factory level operations consequences of re-entrant flow, where the dimensions of different interconnect levels produce different throughputs for different levels. Thus, the HSE presents a potentially valuable tool for rapid optimization in the presence of factory dynamics, usable by operations, equipment, and process engineers.

3:40pm **MS-ThA6 Plasma Reactor Simulation to Improve Film Deposition Uniformity**, ***K. Bera,*** *K. Liu,* Applied Materials, Inc.

A capacitively coupled plasma discharge has been simulated for an industrial reactor to investigate the uniformity of the film deposition profile on the wafer. The gap width between the powered cathode and the ceramic wafer pedestal is very small compared to the radius of the cathode. Non-uniform grid is used to resolve the sheath in the plasma for this reactor configuration. Silane is fed as a feed gas from the showerhead into the chamber at low pressure. The spatial distributions of electron, ion and radical densities, electron temperature and ion energy are obtained using Plasma Reactor Simulator (PRSim) code. The spatial distributions of radical flux and ion energy on the wafer are useful for the prediction of thin-film deposition rate. The effect of the distance of wall dielectric from the wafer edge on the surface process is also investigated. A mixture of silane and nitrous oxide is fed in the chamber to investigate the effect of silane dilution on the process. The present study is used to identify the reactor design condition to achieve uniform film deposition rate on the wafer.

4:00pm **MS-ThA7 First Principles Modeling of Gas-Surface Interactions in Low Pressure CVD Processes**, ***H. Simka,*** *S.S. Shankar,* Intel Corp.*; J.-R. Hill, S. Mumby,* Molecular Simulations, Inc.

Understanding and optimization of low-pressure CVD systems typically necessitate knowledge of interactions between gas-phase species and

surface at the molecular level. A physically-based approach to model these interactions is presented. The approach is based on ab-initio quantum chemistry investigations of molecular and surface properties, as well as binding between reactive gas-phase precursors with atoms on the growth surface. Application of the method to low-pressure CVD of silicon nitride using dichlorosilane (DCS) and ammonia will be illustrated. Energetics of the gas-surface interactions are calculated using density-functional theory (DFT), with the surface represented by H-terminated clusters involving the active centers. Energy values obtained using DFT methods for this system are typically more accurate compared to those obtained using semi-empirical methods. For example, the activation barrier for gas-phase decomposition of DCS to SiHCl and HCl calculated using the PM3 semi-empirical method is 45 kcal/mole, which is significantly lower than values obtained using DFT and more accurate ab-initio methods such as G2 (65 to 68 kcal/mole). Other comparisons illustrating further limitations of the semiempirical method for modeling of gas-surface interactions will be presented. Reactivity of several surface sites in the cluster model is investigated. Adsorption energies of several gas-phase species are calculated; accuracy of the several DFT methods used is evaluated and will be discussed.

4:20pm **MS-ThA8 Etching of Silicon in HBr Plasmas for High Aspect Ratio Features**, ***H.H. Hwang,*** ELORET Corp.*; G.S. Mathad, R. Ranade,* Infineon Technologies, Inc.*; M. Meyyappan,* NASA Ames Research Center

Acquiring straight wall etching is a continuing goal in the semiconductor processing industry. Achieving a vertical wall with no bowing becomes extremely critical as dimensions decrease to less than 0.1 µm. Undercutting must be minimized in order to obtain closely spaced features of this size. Etching typically requires aspect ratios on the order of 20:1 (depth:width) and often higher than 50:1. At these small feature sizes and large aspect ratios, neutral shadowing becomes increasingly more important. Fewer neutral radicals which can passivate the substrate surface can enter the trench opening, which leads to a decreased etch rate and can limit the maximum obtainable aspect ratio (AR). In pure chlorine, for example, it is difficult to achieve ARs of more than 5:1. To date, however, most modeling efforts have not focused on the specific problems encountered in high aspect ratio etching. We will present results for etching silicon in HBr plasmas using a previously developed feature profile evolution simulation using a level set method (SPELS). We will compare calculated average etch rates, total etched depth, and RIE lag effects (etch rate dependence on feature size) in high aspect ratio trenches to experimental measurements. The measurements were made in a parallel plate, capacitively-coupled, magnetically enhanced reactor. We will also present comparisons in etch rates for different feature sizes (0.2 µm, 0.175 µm, and 0.15 µm). Comparisons of simulated etched profiles and experimentally obtained SEMS will also be presented.

4:40pm **MS-ThA9 Contamination Removal from Wafer with Deep Trenches**, ***H. Lin,*** *A.A. Busnaina, I.I. Suni,* NSF and CAMP (New York Center for Advanced Materials Processing, at Clarkson University)

The International Technology Roadmap for Semiconductors shows the requirement for high aspect ratio (depth/width) trenches in DRAM trench capacitor technology. Cleaning high aspect ratio deep trenches is challenging because of the need to rinse or remove contaminants from the bottom of trench. In this work, based on the experimental and numerical study of blanket wafer cleaning, contamination removal from wafer with topography is studied using physical modeling. The rinsing flow and contaminant transport in the geometry are modeled by solving the governing momentum and mass conservation equations with associated boundary conditions. The rinsing of patterned wafer is accomplished using an oscillating flow past a series of high ratio rectangular trenches. The modeling results of flow past a series of trenches show a good agreement with the experimental results of Perkins. Oscillating flow rinse is found to be more efficient than steady flow rinse using the same average rinsing velocity. The effects of the aspect ratio, trenches size, and oscillating flow frequency on cleaning efficiency are presented.

5:00pm **MS-ThA10 In Situ Metrology for Cu Electroplating**, ***G. Barna,*** Texas Instruments, US

This presentation will describe the use of the RTA (Technic, Inc.) system for control of a Cu plating bath in a SC productization environment. This tool is a robust, in-situ sensor that analyzes all the components of the bath by a variety of electroanalytical techniques. It consists of a probe that stays continually immersed in the main bath module of the plater, with the appropriate electronics and PC controller located within 25 ft. of the probe. A complex factory calibration scheme provides accurate measurements. The internally generated reference electrode and the rigorous electrochemical cleaning procedures provide long-term repeatability and reliability. Measurements of all 5 components are performed in ~ 15 minutes, making repeated measurements easy. Long-term sensor stability has been demonstrated. After a year of continuous use, this sensor has required no recalibration and virtually no maintenance. Bath control is greatly facilitated by the accuracy, repeatability and reliability of this sensor. Its CoO is minimal, there is no need for any standards or test solutions and its cleanroom footprint is no larger than a PC. Further development of this system, aimed to provide information over and above simple bath control, will also be described.

Manufacturing Science and Technology
Room 304 - Session MS-FrM

Langmuir Award/Ultra Clean Society and Contamination Free Manufacturing

Moderator: A. Diebold, Sematech

8:20am **MS-FrM1 Surfaces, Interfaces, and Chemical Reactions in Semiconductor Technology and Manufacturing**, ***G.W. Rubloff***[1], University of Maryland **INVITED**

Atomic-scale properties and chemical reactivity of surfaces and interfaces constitute the science upon which semiconductor technology advances. Since thin film growth, etching, and modification occur as dynamic sequences of surface or interfacial reaction steps, surface reaction phenomena indeed determine the morphology, topography, microstructure, and chemical/physical properties of microelectronic structures, as well as their resulting functionality in devices, circuits, and systems. The surface science community brings an invaluable set of research strategies to understand, control, and advance semiconductor technology, particularly in combining vacuum technology and highly controlled process conditions together with surface, interface, gas phase, and thin film materials characterization. These synergies are proving effective as well in addressing key issues in semiconductor manufacturing.

9:00am **MS-FrM3 The Application of In-situ Monitor of Extremely Rarefied Particle-clouds Grown Thermally Above Wafers by using Laser Light Scattering Method to the Development of the Mass-production Conditions of the Tungsten Thermal CVD**, ***N. Ito***, *T. Moriya, F. Uesugi,* NEC Corporation, Japan*; S. Moriya, M. Aomori, Y. Kato,* Tokyo Electron Ltd., Japan*; M. Tachibana,* Tokyo Electron Yamanashi Ltd., Japan

It is successfully demonstrated that the scattered-light intensity by thermally grown particle-clouds above wafers in the real tungsten (W) CVD chamber has a good correlation both with the surface roughness of the W-CVD film measured by the atomic force microscopy (AFM) and with the raw material gas-flow ratio SiH@sub 4@/WF@sub 6@. In addition, since our in-situ particle monitor above wafers can detect particle-clouds consisting of particles less than 10nm in size, the appearance and the motion of particle-clouds corresponding to the transient variation of the ratio SiH@sub 4@/WF@sub 6@ at the conversion of gases and/or at the change of the flow rate can be observed. On the basis of these results, the mass-production conditions of particle-free and smooth surface of W-films are clarified with short Cycle Time. The traditional ways of developing the mass-production CVD conditions need many monitor-wafers and are time consuming, because both clarification of the suppression conditions of gas-phase particles by the in-situ particle monitor in vacuum exhaust lines and confirmation by the wafer-level visual inspection are indispensable. Moreover, the sensitivities of in-situ particle monitor at an exhaust line and the wafer-level inspection machine become insufficient to develop process conditions, as reduction of design rule for LSI proceeds. Therefore, application of the in-situ particle monitor above wafers to the development of mass-production conditions is notable method to minimize the non-product wafers and to realize short Cycle Time.

9:20am **MS-FrM4 Standard Practice for Temperature Calibration of the Silicon Substrate in Temperature Programmed Desorption Analysis**, ***T. Matsunaga***, Matsushita Inc., Japan*; N. Yabumoto,* NTT Adv. Tech. Co., Japan*; N. Hirashita,* Oki Electric Ind. Co., Ltd., Japan*; H. Okumura,* Toray Res. Center, Inc., Japan*; M. Nishiduka,* Toshiba Corp., Japan*; I. Nishiyama,* NEC Corp., Japan*; M. Matsuura,* Mitsubishi Corp., Japan*; M. Morita,* Osaka Univ., Japan*; A. Shimazaki,* Toshiba Corp.*; T. Jimbo,* Hitachi, Ltd.*; T. Ajioka,* NTT Electronics Corp.

Ultra Clean Society (UCS)'s Equipment Standardization Working Group proposed a standard practice covering temperature calibration of the silicon substrate, ranging from 400 to 1000°C, for temperature programmed desorption (TPD) analysis. Although TPD has been widely used to characterize materials and fabrication processes in ULSI devices, the temperature is not accurate enough to develop reliable fabrication processes. The desorption temperature was found to differ over 100°C between interlaboratory TPD measurements. In order to solve this problem, the ramping temperature of TPD instrument was calibrated to silicon substrate temperature by this proposed standard practice, which consists of heating silicon calibration materials at a controlled rate in TPD instrument, measuring characteristic desorption peak temperatures, and quadratic calibration fitting to the standard temperatures. The calibration materials are (1) CaC@sub 2@O@sub 4@.H@sub 2@O dropped on a Si wafer and dried, (2) Ar and (3) H ion implanted into Si wafers. The standard temperatures of the characteristic desorption, associated with decomposition, structural transformation and lamination of silicon, were determined by special TPD instrument with the highest isothermal space around the specimen among the interlaboratory. The precision of this practice was determined in an interlaboratory test in which 4-5 laboratories participated using two instrumental models. This test using a few common specimens proved that the average standard deviation, measured in different laboratories for all the measurements with ramping rates of 10, 30 and 60°C /min, was estimated to be 6.0°C between 400 and 1000°C.

9:40am **MS-FrM5 Standardization of the Method to a Disiloxane Concentration in Monosilane Gas using Atmospheric Pressure Ionization Mass Spectrometer**, ***M. Kitano***, Tohoku Univ., Japan*; Y. Sakakibara,* NTT Adv. Tech. Corp., Japan*; Y. Ishihara,* Nippon Sanso Corp., Japan*; Y. Kunii,* Kokusai Electric Co., Ltd., Japan*; K. Hasumi,* Hitachi Tokyo Electronics Co., Ltd., Japan*; I. Matsuda,* Syowa Denko K.K., Japan*; A. Ohki,* Osaka Sanso Kogyo Ltd., Japan*; Y. Shirai,* Tohoku Univ., Japan

Ultra clean society (UCS)'s process gas measurement standardization working group proposed, using atmospheric pressure ionization mass spectrometer (APIMS) which has two ionization compartments to measure the disiloxane(SiH@sub 3@-O-SiH@sub 3@) in monosilane(SiH@sub 4@) gas at concentrations between 10ppb to 1000ppb. In this standard, SiH@sub 4@ with SiH@sub 3@-O-SiH@sub 3@ of unknown concentration is introduced into the second ionization compartment. Ar@super +@ ion generated by corona discharge in the first ionization compartment is sent out to the second ionization compartment. And Ar@super +@ ion reacts with SiH@sub 3@-O-SiH@sub 3@ in the SiH@sub 4@ gas to exchange ion, and SiH@sub 3@-O-SiH@sub 3@ ion are generated in large amount. SiH@sub 3@-O-SiH@sub 3@ is detected with mass number of 77. Using relative ion intensity of SiH@sub 3@-O-SiH@sub 3@ and calibration curve acquired by follow method, SiH@sub 3@-O-SiH@sub 3@ concentration is determined. H@sub 2@O of a known concentration firstly adsorbed into the stainless steel tube. This tube is purged out using SiH@sub 4@ gas. Adsorbed H@sub 2@O reacts with SiH@sub 4@, and SiH@sub 3@-O-SiH@sub 3@ is generated. Adsorbed H@sub 2@O volume and generated total disiloxane volume are in a proportion of one to one. So that the amount of disiloxane in SiH@sub 4@ gas can be quantitatively calculated. The determination limit, which was defined as 3 times of the standard deviation of SiH@sub 3@-O-SiH@sub 3@ concentration in purified SiH@sub 4@ gas was found to be 10ppb. For verification of calibration curve, calibration curves, which were prepared at different timings and different places by different people, showed good agreement of over 80%. Moreover, it is proved that calibration curve of SiH@sub 3@-O-SiH@sub 3@ in SiH@sub 4@ can be substituted by that of H@sub 2@O in Ar which is corrected with a correction coefficient.

10:00am **MS-FrM6 A Wide Range Vacuum Sensor Fabricated by MEMS**, *H. Miyashita,* ***Y. Kitamura***, *H. Watanabe,* ANELVA Corporation, Japan*; M. Esashi,* Tohoku University, Japan

A wide range capacitive vacuum sensor has been developed by microelectromechanical system (MEMS) technology. Use of MEMS technology has many advantages such as ability to miniaturization of the sensor, mass production, cost reduction etc. when compared to the conventional mechanical processes. The reason is that MEMS process is very similar to that of semiconductor device fabrication processes. The sensor is comprised of an SD2 glass and a silicon substrate. The length, width and thickness of the sensor is 20mm, 20mm, and 1.4mm, respectively. The fabricated vacuum sensor has two silicon diaphragms with 4mm x 4mm and 1mm x 1mm dimensions, and the thickness of the diaphragms is 7μm. Since the deflection of a diaphragm depends on the diaphragm size, the sensor measures a wide range of pressure. The smaller diaphragm shows linear characteristics of electrostatic capacitance at the pressures below 40,000Pa. The larger diaphragm shows linear characteristics of electrostatic capacitance at the pressures below 200Pa. The developed sensor is able to measure pressure in the range of 0.04Pa to 40,000Pa. This is achieved by using an electrical circuit which converts electrostatic capacitance into voltage over three orders. The same technology is applicable to the fabrication of vacuum sensors that measure pressures in other ranges by changing the size of the diaphragms. Moreover, the number of diaphragms in a sensor also can be increased to

[1] **Gaede-Langmuir Award Winner**

enhance the pressure-monitoring region without increasing the fabrication processing steps.

10:40am **MS-FrM8 The Effect of Molecular Weight of Organic Contaminants on their Adsorption on Si-wafers**, ***Y. Wakayama,*** Tohoku University, Japan*; S. Kobayashi, T. Ishii,* Taisei Corporation, Japan*; S. Sugawa, T. Ohmi,* Tohoku University, Japan

It is well known that organic contaminants adsorbed on silicon wafer surface degrade the performance of ULSI devices. However, there have been no reports on relation of adsorption behavior of organic contaminants to the silicon or silicon oxide surfaces and their molecular weight. In this study, we have found that the amount of adsorbates on a silicon oxide suface depends on the molecular weight of organic substances. In order to investigate the adsorption behavior of organic contaminants on silicon oxide surfaces, we used solid waxes with aliphatic hydrocarbons, polyvinyl chloride sheets with phthalic esters and silicone sealing materials containing cyclosiloxanes with different molecular weights(Mw) as a contamination source. Each of these materials was separately stored in a closed vessel with a wafer with oxide film for 24 hours. The above organic adsorbates on the oxide surface were analyzed by thermally desorbed and gas chromatography-mass spectroscopy. It was found from our data that as the molecular weight of the organic compounds on the oxide suface increases the amount of adsorbates from oxide surface increases as well and reaches a maximum. Thereafter the amount gradually decreases down to the detection limit of the instruments. It is thought that the phenomenon is related in some way to the balance between the heat of adsorption of organic substances and the vapor pressure. Because, The heat of adsorption that determines the adsorption ability of organic compounds on Si-wafer increases with increase of Mw. On the other hand, the vapor pressure of organic compounds that also determine their rates of adsorption on Si-wafer decreases with increase of Mw.

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