Wednesday Morning, October 4, 2000

Dielectrics
Room 312 - Session DI+EL+MS-WeM

Low K Dielectrics
Moderator: J.A. Kelber, University of North Texas

8:20am **DI+EL+MS-WeM1 Ultra Low k Mesoporous Silica Dielectrics for Semiconductor Interconnects**, ***S. Baskaran***, *J. Liu, X. Li, C. Coyle, J. Birnbaum, G.C. Dunham, G.E. Fryxell,* Pacific Northwest National Laboratory*; C. Jin,* International SEMATECH **INVITED**

The semiconductor industry is currently targeting new intermetal dielectric (IMD) films with dielectric constants (k) less than 2.5 for interconnect applications in the 100 nm technology node, and films with k less than 2.0 for the 70 nm technology node. To meet extreme low k needs for advanced on-chip interconnects, films with incorporated porosity will most certainly be required. Porous dielectric films with k values less than 2.2 ("ultra low k") are not easily synthesized using conventional vacuum based technology such as chemical vapor deposition. A simple approach to nanoporous dielectric films involves spin-on deposition of formulations consisting of silicate, polymeric, or hybrid organosilicate precursors with thermally degradable pore-formers. Ultra low k mesoporous silica films have been synthesized with molecularly templated porosity using this approach. Molecularly organized nanostructured aggregates between 2 and 10 nm in size can function as templates for pore formation in spin coated sol-gel silicate films. The use of a structurally organized template during synthesis results in a uni-modal pore size distribution in the final film. In this paper, we present information on precursor chemistry for designing mesoscale porosity, pore architecture and surface chemistry, and the critical dielectric and mechanical properties for mesoporous silica films. Using formulations developed at PNNL, mesoporous films have also been prepared at SEMATECH on production-size wafers, and evaluated. Copper single-damascene one-level test structures were built using mesoporous silica as the intermetal dielectric. No major structural failures were observed after chemical mechanical planarization on both blanket films and patterned wafers, indicating relatively good mechanical integrity for a highly porous structure. With controlled film synthesis and dehydroxylation conditions, mesoporous silica films with k@super 2@ 2.0 and elastic modulus of 4.0 GPa have been synthesized at PNNL. The results of the one-level metal screening tests at SEMATECH combined with properties obtained at PNNL indicate that mesoporous molecularly-templated silicate films hold promise as ultra low k intermetal dielectrics.

9:00am **DI+EL+MS-WeM3 Deposition of Thermal Stable Amorphous Carbon Nitride Thin Films with Low Dielectric Constant by ECR-CVD**, *X.W. Liu,* National Tsing Hua University, Taiwan, ROC, Taiwan,ROC*; J.H. Lin,* National Tsing Hua University, Taiwan, ROC*;* ***H.C. Shih****,* National Tsing Hua University, Taiwan, ROC, Taiwan,ROC

Amorphous carbon nitride thin films with low dielectric constants and high thermal stability were synthesized on silicon by using an electron cyclotron resonance chemical vapor deposition (ECR-CVD) system in which a rf bias was applied to the silicon substrate and a mixture of C@sub 2@H@sub 2@, N@sub 2@ and Ar was used as precursors. The dielectric constants of our amorphous carbon nitride thin films were found as low as 2.4 at 1 MHz. The thermal stability of the films has been improved by the incorporation of nitrogen to the carbon film. The basic structure, composition and electronic properties of these films were analyzed by Fourier transformation infrared (FTIR) spectroscopy, Raman spectroscopy, X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and field emission scanning electron microscopy (FE-SEM) and dielectric constant measurements.

9:20am **DI+EL+MS-WeM4 Impact of Hydrogen Addition on the Deposition Rate of SiOF Films Prepared by High Density Plasma CVD**, *Y.W. Teh,* Nanyang Technological University, Singapore*; T.C. Ang,* Chartered Semiconductor Manufacturing, Singapore*;* ***K.S. Wong****,* Nanyang Technological University, Singapore*; K.H. See, S.Y. Loong, Y.C. Wong,* Chartered Semiconductor Manufacturing, Singapore

Fluorinated Silicon Dioxide film (SiOF) has been considered as the more successful first generation interlevel low-k dielectric material. However, the impact of hydrogen addition on SiOF film properties are not extensively studied. In this paper, we present a spectroscopic study of the chemical bonding in SiOF film grown with silane gas added to the standard precursors using the techniques of ellipsometry and infrared (IR) absorption spectroscopy. These SiOF films have been prepared by high density plasma (HDP) chemical vapor deposition at substrate temperature at about 420°C. Addition of hydrogen through silane gas feed is found to control deposition rate and the fluorine doping concentration of the SiOF films. The addition of SiH4 does not lead to the incorporation of hydrogen in detectable quantities in the SiOF films. This phenomenon may be attributed to the strong mutual attraction between hydrogen and fluorine radicals in the HDP. The decrease of refraction index at 632.8nm and the frequency decrease of the dominant IR active bond-stretching vibration at ~1085cm@super -@@super 1@ were found to be approximately linear with increase in fluorine concentrations. The silane added to the process gas mixture has been found to play an active role in the SiOF film formation process both in the surface reactions and the chemical bonding properties. Our results show that with an optimized silane flow rate, the film stability of the SiOF towards moisture attack is significantly improved. In addition, a high deposition rate can be achieved together with comparable fluorine incorporation in the film as compared to the standard non-silane precursors.

9:40am **DI+EL+MS-WeM5 Solid-state Nuclear Magnetic Resonance of Low Dielectric Constant Si:O:C:H Films**, ***P.-Y. Mabboux****, K.K. Gleason,* Massachusetts Institute of Technology

Adding organic content to SiO@sub 2@ is an evolutionary pathway to low dielectric films with k @<=@ 3.0. Alternate names for these materials include carbon-doped oxides, organosilicate glasses (OSG), and Si:O:C:H films. Both spin-coating and chemical vapor deposition (CVD) processes have been developed for this class of low-k films. Fourier transform infrared spectroscopy (FTIR) and x-ray photoelectron spectroscopy (XPS) have only a limited ability to distinguish variations in Si:O:C:H film chemistry. In this work, solid-state nuclear magnetic resonance (NMR) is shown to have sufficient sensitivity to determine the network structure of low dielectric constant Si:O:C:H films. Characterization of Si:O:C:H films by @super 1@H, @super 13@C, and @super 29@Si magic-angle spinning NMR will be demonstrated. Because of its wide range of chemical shifts, @super 29@Si NMR is particularly useful to elucidate new details regarding the composition and structure of these low dielectric constant films. Up to ten different environments can be resolved in some of the films. Many of the observed chemical bonding configurations have been previously observed in bulk organosilicate glasses. The NMR results can be expressed in terms of a connectivity number, which is simply the average number of bonds between network forming atoms. The connectivity number may provide a means to correlate with the mechanical properties. Fundamental understanding of structure-property-processing relationships will facilitate the engineering of the molecular architecture required for successful integration of Si:O:C:H dielectric films.

10:00am **DI+EL+MS-WeM6 A New Simple and Accurate Method to Measure Intra-Metal Capacitance of Low-K Fluorinated Silicon Dioxide**, *K.S. Wong,* ***Y.W. Teh****,* Nanyang Technological University, Singapore*; T.C. Ang, S.Y. Loong, W.B. Loh, Y.C. Wong,* Chartered Semiconductor Manufacturing, Singapore

An accurate and simple technique for intra-metal capacitance measurement is presented. This on-chip technique is based on a test structure design that utilizes only interdigitated capacitors sandwiched between metal plates. Compared to other techniques which utilize transistors in addition to the unknown interconnect capacitance to be characterized, this new technique requires only capacitors and thus much simpler processing and shorter cycle times but with the same level of accuracy. With this test structure design, no reference capacitor is needed. Capacitance voltage (C-V) method is commonly used for intra-metal capacitance measurement. However, the measurement accuracy is often compromised by probe-induced stray capacitance. In this paper, a new measurement technique that can eliminate this stray capacitance is reported. This new technique uses multiple probe configurations to obtain 3 capacitance values and these values can be used to eliminate the probe-induced stray capacitance and obtain the actual intra-metal capacitance. Results show much better accuracy than the conventional C-V measurement. Comparisons between the new technique, the conventional C-V measurement and the Charge-Base Capacitance Measurement (CBCM) techniques are made. Our results based on the new technique show great improvement in the measurement accuracy over the conventional technique. In addition, our results are consistent with the results obtained from the CBCM technique which requires the use of transistors and thus more complex processing and longer cycle times. In this paper, the different measurement techniques were evaluated on high-density plasma chemical vapor deposition (HDP-CVD) fluorinated silicon dioxide (SiOF) inter-level dielectric (IMD) films in 0.18um technology.

10:20am **DI+EL+MS-WeM7 DC and RF Characteristics of Advanced MIM Capacitors for MMIC's Using Thin and Low Temperature PECVD Si@sub 3@N@sub 4@ Dielectric Layers**, ***C.R. LIM***, *J.H. LEE, S.W. Paek, K.W. Chung,* LG-ELITE, Republic of Korea

In this work, we show the excellent DC and RF characteristics of MIM (metal-insulator-metal) of PECVD Si@sub 3@N@sub 4@ thin film deposited at 85°C. The breakdown field strength of MIM capacitors with 490 Å Si@sub 3@N@sub 4@ was larger than 4.1 MV/cm which indicates the excellent quality of the deposited Si@sub 3@N@sub 4@ film. The main capacitance of unit area extracted by RF (radio frequency) measurements was 1240 pF/mm@super2@. So, its high capacitance enables us to reduce the size of MIM to a quarter size compared with the conventional MIM having 2000 Å Si@sub 3@N@sub 4@. In spite of its thin thickness of dielectrics, RF characteristics showed good performance. Above all, it was fabricated at low temperature, so we were able to develop the process of MIM fabrication using dielectric lift-off. At this point, the thickness adapted in dielectric lift-off process was about 1000 Å for adjusting capacitance to a designed capacitance.

10:40am **DI+EL+MS-WeM8 Rapid Prototyping by Local Deposition of Siliconoxide and Tungsten Nanostructures for Interconnect Rewiring**, *H.D. Wanzenboeck, S. Harasek, H. Langfischer, A. Lugstein,* ***E. Bertagnolli****,* Vienna University of Technology, Austria

The local deposition of dielectric material and metal wires as typically used for rewiring of interconnect layers has been demonstrated to be a promising approach for rapid prototyping of integrated circuits. With an ion beam induced surface reaction dielectric structures were fabricated with a selected geometric configuration in dimensions ranging from several hundred Âµm down to the deep sub-Âµm scale displaying the potential application in interconnect modification. A focused Ga ion beam at 50 kV acceleration voltage was applied to induce the surface decomposition of gaseous precursors. A dynamic adsorption state was achieved characterized by the equilibrium between influx through a nozzle system and the outlet through the vacuum pump. Siliconoxide was obtained by using siliconorganic compounds and oxygen as precursor adsorbed on the surface at a total pressure typically between 10E-5 to 10E-6 Torr. Conductive W-structures were obtained using W(CO)6. The suitability for practical applications in microelectronics has been demonstrated by measuring the electrical properties of deposited dielectrics using test vehicles with a metal-insulator-metal (MIM) capacitor setup. The thickness of the dielectric layer was varied between 70 nm and 1.4 Âµm. The resistivity and capacitance of FIB deposited dielectrics was found to vary with deposition parameters such as exposure time and scanning rate of the ion beam. A chemical characterization of the fabricated dielectric layers has been performed. The electrical properties of locally deposited dielectrics were correlated with the material composition of the deposited material. The suggested optimized deposition process can provide improved dielectrics suitable as interline and interlayer insulator for a complex microelectronic interconnect architecture.

Dielectrics
Room 312 - Session DI+EL+MS-WeA

Alternate Gate Dielectrics
Moderator: R. Ramesh, University of Maryland

2:00pm **DI+EL+MS-WeA1 Materials Considerations for High-K Gate Dielectrics for Scaled CMOS**, ***G.D. Wilk,*** Lucent Technologies*; R.M. Wallace,* University of North Texas **INVITED**

Many materials systems are currently under consideration as potential replacements for SiO@sub 2@ as the gate dielectric material for sub-0.13 µm CMOS technology. A systematic consideration of the required properties of gate dielectrics, however, indicates that the key issues for selecting a high-k dielectric are permittivity and band offset, thermodynamic stability, crystal structure, and compatibility with the current or expected materials to be used in processing for CMOS devices. Many dielectrics satisfy some of these criteria, but very few materials actually satisfy all. A review of current work and literature in the area of high-k gate dielectrics is given, and some conclusions are drawn for various systems based on reported results and fundamental materials considerations.

2:40pm **DI+EL+MS-WeA3 New High k Thin Films with Improved Physical and Electrical Properties**, ***Y. Kuo,*** *J. Donnelly, J. Tewg,* Texas A&M University

When the minimum device dimension is shrunk to 100 nm, the conventional silicon oxide cannot fulfill many requirements of the device.@footnote 1@ For example, the thin gate dielectric layer (e.g., < 1.2 nm) will have a high leakage current and cannot stop the boron penetration. The dielectric constant of silicon oxide (e.g., 4.0) is too low for the small-size storage capacitor cell. Therefore, it is urgent to develop a new kind of thin film dielectric that has a high dielectric constant (high k) and can satisfy all stringent material, process, and device requirements. Metal oxides are ideal candidates for the gate dielectric application because their compositions are simple and their k values are high enough to last for next several generations of devices. In addition to the high interface states, a metal oxide has the problem of high leakage current, which is caused by the polycrystalline phase formation during the high temperature process.@footnote 2,3@ In this paper, we present new results on high k metal oxides that have high amorphous-to-polycrystalline transition temperatures. By adding a third element into tantalum oxide, e.g., Ti, Cu, and Mo, the film can exist in the amorphous phase in an extended temperature range. The leakage current at a high temperature is lowered. Material and electrical characteristics of the new film, e.g., by x-ray diffraction, ellipsometer, current-voltage and capacity-voltage curves, will be shown and discussed. The influence of the deposition process, i.e., reactive co-sputtering, to film properties will also be presented. These new high k dielectrics have the potential of being used as gate dielectrics in future MOS devices. @FootnoteText@ @footnote 1@ International Technology Roadmap for Semiconductors, 1999 ed., SIA, etc. @footnote 2@ S. R. Jeon, S. W. Han, and J. W. Park, J. Appl. Phys. 77, 5978, 1995. @footnote 3@ R. B. van Dover, R. M. Fleming, L. F. Schneemeyer, G. B. Alers, and D. J. Werder, IEDM, 823, 1998.

3:00pm **DI+EL+MS-WeA4 Chemical and Microstructural Separation of Homogeneous Plasma Deposited (ZrO@sub2@)@subx@(SiO@sub2@)@sub(1-x)@ films (x @<=@ 0.5) into SiO@sub2@ and ZrO@sub2@ Phases after Rapid Thermal Annealing in Ar at 900°C**, ***B. Rayner,*** *R. Therrien, G. Lucovsky,* North Carolina State University

Zr-silicate alloys along the pseudo-binary join from SiO@sub2@ to ZrO@sub2@ have attracted interest as high-k dielectrics for Si CMOS devices with equivalent oxide thickness extending to 0.6 nm. In this study alloy films were deposited on HF-last and pre-oxidized and/or nitridized Si(100) by remote plasma enhanced chemical vapor deposition using Zr(IV)-t-butoxide. Film and interface chemical composition, local atomic bonding, and film morphology were studied by Auger electron spectroscopy, Fourier transform infrared absorption, X-ray diffraction, and Rutherford back-scattering. These studies identified two alloy regimes: (i) SiO@sub2@-rich compositions to the compound silicate, ZrSiO@sub4@ (x = 0.5), where properties may be suitable for high-k applications, e.g., films are amorphous on deposition and remain so up to at least 800°C, and (ii) ZrO@sub2@-rich compositions in which films are either partially or totally crystalline on deposition, or after relatively low temperature (< 600°C) anneals. Alloys in the SiO@sub2@-rich regime are chemically-ordered as-deposited at ~350°C with predominantly Si-O-Si and Zr-O-Si bonds, but after annealing in Ar at 900°C for 60 s, separate chemically and microstructurally into SiO@sub2@ and ZrO@sub2@ phases. The ZrO@sub2@ phase is crystalline at the ZrSiO@sub4@ composition. This separation may limit integration of these films into devices which incorporate polycrystlline-Si gate electrodes requiring dopant activation at temperatures > 900°C. Capacitance-voltage and current-voltage characteristics will be presented for as-deposited and annealed films to illustrate the effects of chemical phase separation and crystallization in defining maximum post deposition processing temperatures.

3:20pm **DI+EL+MS-WeA5 A Study of ZrO@sub2@ and Zr-silicate Thin Film for Gate Oxide Applications**, ***S.-W. Nam,*** Yonsei University & Samsung Electronics Co., Korea*; J.-H. Yoo, H.-Y. Kim, D.-H. Ko,* Yonsei University, Korea*; S.-H. Oh, C.-G. Park,* Pohang University of Science and Technology (POSTECH), Korea*; H.-J. Lee,* Stanford University

We investigated the microstructures and electrical properties of ZrO@sub2@ and Zr-silicate thin films deposited by reactive DC magnetron sputtering on Si substrate for gate dielectric application. The films deposited on Si with various deposition conditions and annealing treatments were analyzed by spectroscopic elipsometry, XRD, AFM and XPS. The refractive index of the ZrO@sub2@ thin films increased upon annealing. The ZrO@sub2@ film deposited at low temperature and low power showed amorphous structure, which the films deposited at high temperature and high power showed crystalline structures. The growth of the interfacial oxide between ZrO@sub2@(or Zr-silicate) and Si substrate was observed by cross sectional HR-TEM. C-V and I-V measurements of the MOSCAP structures showed that the accumulation capacitance value and the leakage current level decreased upon annealing in O@sub2@ gas ambient, which is explained by the formation of the interfacial SiO@sub2@ layer.

3:40pm **DI+EL+MS-WeA6 Ultra-thin Zirconium Oxide Films Deposited by Rapid Thermal CVD for MOSFET Applications**, ***Y. Lin,*** *J.P. Chang,* University of California, Los Angeles

The increasingly tighter process specifications for the next generation microelectronic devices dictate the usage of metal oxides such as zirconium oxide as insulators for better process control and a more reliable dielectric/silicon interface.@footnote 1@ Zirconium t-butoxide is used with O@sub 2@ in this work to deposit zirconium oxide in a RTCVD system. The deposition temperature can be rapidly ramped to and controlled at 400-600°C, and the physical properties of the ZrO@sub 2@ films are characterized by XPS, XRD, AFM, TEM, and spectroscopic ellipsometry to determine the film compositions, chemical states, film microstructures, morphology, thickness, and index of refraction. Amorphous and nearly stoichiometric ZrO@sub 2@ has been deposited with less than 0.2nm variation in thickness across a 4" wafer. The dielectric constant is 3-4 times greater than that of SiO@sub 2@. Leakage current of a ZrO@sub 2@ film with an effective oxide thickness of 10 Å is three orders of magnitude lower than that of a 10Å thermal SiO@sub 2@ film. Post-deposition annealing at 500-700°C is shown to be effective in removing the majority of the incorporated carbon and further reduce the leakage current. However, there exists an optimal carbon doping level where carbon effectively passivates the electrically active defects and reduces the leakage current. We propose a simple kinetic model to describe the heterogeneous reactions responsible for the film deposition. NMOS transistors are fabricated and tested to determine the dielectric constant, leakage current, I-V and C-V characteristics of the zirconium oxide films. Moreover, stress induced leakage current and time dependent dielectric breakdown will also be detailed to assess the material reliability for its applications in microelectronics. @FootnoteText@ @footnote 1@G. D. Wilk, and R. M. Wallace, "Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon," Appl. Phys. Lett., 74(19), 2854(1999).

4:00pm **DI+EL+MS-WeA7 High-quality Ultrathin Fluorinated Silicon Nitride Gate Dielectric Films Prepared by Plasma Enhanced Chemical Vapor Deposition Employing NH@sub 3@ and SiF@sub 4@**, ***H. Ohta,*** *M. Hori, T. Goto,* Nagoya University, Japan

The silicon nitride (SiN@sub x@) film attracts much attention as scaled gate dielectric films in next generation@super ,@s ULSI. However, the conventional SiN@sub x@ film has a poor interface with silicon and is leaky due to a high trap density in the film. Recently, we have developed ultrathin fluorinated SiN@sub x@ films formed by ECR-PECVD employing NH@sub 3@/SiF@sub 4@. It is known that the average bond energy (5.73eV) of Si-F is higher than that of Si-H (3.18eV). Therefore, it is

expected that the Si-F bond in the film should have improved the quality of gate dielectric film. In this study, we have investigated properties of ultrathin SiN@sub x@ films (4nm) formed at 350°C. These films (fluorinated SiN@sub x@ films) contain fewer hydrogen atoms than the conventional SiN@sub x@ films formed by ECR-PECVD employing NH@sub 3@/SiH@sub 4@. As-deposited fluorinated SiN@sub x@ films indicated the excellent hysteresis loop (20mV) in the C-V curve, and reduced the leakage current by several orders of magnitude than the thermal SiO@sub 2@ in the identical equivalent oxide thickness (EOT). These film properties and the surface reactions for the SiN@sub x@ film formation with good quality are discussed on the basis of results of the in-situ XPS, in-situ FT-IR RAS, FT-IR, and thermal desorption mass spectroscopy (TDS). As a result, the control of fluorine concentration in the SiN@sub x@ films was found to be a key factor for forming the fluorinated SiN@sub x@ films with high quality at low temperatures. The fluorinated SiN@sub x@ is very effective for ultrathin gate dielectric films in next generation@super ,@s ULSI.

4:20pm **DI+EL+MS-WeA8 Elimination of Carbon Impurities in the Metalorganic Chemical Vapor Deposition (MOCVD) of Titanium Dioxide on Silicon**, ***M. Yoon***, *A.C. Tuan, V.K. Medvedev,* University of Washington*; J.W. Rogers, Jr.,* Pacific Northwest National Laboratory

A novel process has been developed for the deposition of titanium dioxide thin films on p-type Si(100) with high quality interfacial characteristics and the absence of carbon. Elimination of carbon contaminants in the titanium dioxide film and at the interface between the oxide and silicon is important because the presence of impurities can severely degrade the electrical properties of the device. This novel process consists of three stages of deposition in an ultra-high vacuum chamber. Initially, a continuous titanium layer is deposited on silicon using a titanium sublimator. This titanium layer is then oxidized using a gas phase oxygen source to form a TiO@sub x@ buffer layer. Subsequently, a titanium dioxide thin film is deposited by MOCVD using titanium tetrakis-isopropoxide (TTIP) at low temperature (below 650K). Auger electron spectroscopy (AES) analysis at each stage of growth shows no evidence of carbon contamination either within the titanium dioxide layer or at the TiO@sub 2@/Si interface. Additional AES measurements suggest that the titanium layer grows on silicon according to the Stranski-Krastanov mode, which permits uniform growth. A carbon-free titanium dioxide thin film was successfully deposited on silicon using this novel process.

4:40pm **DI+EL+MS-WeA9 Microscopic Understanding of the Interface for the Heteroepitaxy of Crystalline Oxides on Silicon**, ***S. Gan***, *D.E. McCready, D.J. Gaspar, Y. Liang,* Pacific Northwest National Laboratory

With SiO@sub 2@ approaching its fundamental limit as the gate dielectric in the existing Si-based CMOS technology, searching for alternative gate oxides with high dielectric constants is crucial for the next generation of devices. Recent work showed crystalline oxides such as SrTiO@sub 3@ (STO) is promising as an alternative to SiO@sub 2@ in MOS capacitors. One of the most important issues is how to integrate it into the existing Si-based technology, the first step of which is the growth of epitaxial oxides on Si substrates. Here we present our recent results on the study of the oxide-silicon interface, which plays a critical role in growing high-quality STO films. Employing scanning tunneling microscopy (STM), x-ray photoelectron spectroscopy (XPS), low-energy electron diffraction (LEED), we characterized the interfacial structure of each template layer (Sr and SrO) grown on Si in situ. The results revealed that the strontium covered silicon surfaces exhibit a series of reconstructions, including a (2x1) structure that provides the most stable interface for the growth of oxides. In addition, we used time-of-flight second ion mass spectrometry (TOF-SIMS) and x-ray diffraction (XRD) to investigate the interfacial chemistry and film structure. By combining these techniques, we correlated the interface structures with film properties, which allowed us to identify suitable interfacial templates for optimized growth. @FootnoteText@ Pacific Northwest Laboratory is a multiprogram national laboratory operated by Battelle Memorial Institute for the U.S. Department of Energy under Contract DE-AC06-76RLO 1830.

5:00pm **DI+EL+MS-WeA10 Formation of Ultrathin Yttrium Silicate by Thermal Oxidation of Yttrium on Silicon**, ***M.J. Kelly***, *J.J. Chambers, D. Niu, G.N. Parsons,* North Carolina State University

We show that direct thermal oxidation can be used to form thin (<50@Ao@) high-k metal silicate layers directly on crystalline silicon. Bulk thermodynamics indicates that several high-k metal oxides (including oxides of Hf, Zr, Al, Y, La, etc.) will be stable with respect to silicon dioxide formation when the oxide is in contact with silicon. However, most low temperature approaches (PVD, CVD, or MBE) for metal oxide deposition on silicon involve elementary reaction steps that include metal-silicon bond formation before oxidation, resulting in uncontrolled interface layers between the metal oxide and silicon. We can utilize this mechanism to form yttrium silicate films on silicon by first sputtering thin (<10@Ao@) metal films on silicon, vacuum annealing at 300-600Â°C to form a silicide, then oxidizing at 600-900Â°C. XPS, medium energy ion scattering, and IR indicate film composition is close to yttrium orthosilicate (Y2O3Â·SiO2) with some excess Y2O3, depending on anneal conditions. Oxidation kinetics (determined from thicknesses measured by TEM) indicate an initial fast oxidation rate (due to oxidation of metal silicide), followed by a slower process (due to oxidation of underlying silicon). CV analysis of 42@Ao@ films show oxide equivalent thickness ~12@Ao@, consistent with dielectric constant ~14. Leakage is <1A/cm2 at 1V in accumulation. IR and XPS indicate that films do not phase separate when annealed up to 900Â°C for 20 minutes. Thin (<10@Ao@) silicon oxide and nitride interface layers have been formed in-situ by remote plasma exposure before metal deposition and their effect on interface reaction kinetics have been analyzed by XPS and MEIS. Interfacial oxide is observed to have a negligible effect on interface reactions, but results suggest interface nitrogen tends to block silicide formation before oxidation. These results give important insight into controlling interface structure for implementing high-k materials into silicon devices.

Dielectrics
Room 312 - Session DI+EL+MS-ThM

Ultrathin Dielectrics and Interfaces
Moderator: Y.J. Chabal, Bell Laboratories, Lucent Technologies

8:20am **DI+EL+MS-ThM1 Oxidation of Clean and H-passivated Silicon by Molecular and Atomic Oxygen**, ***X. Zhang,*** Rutgers University; *Y.J. Chabal,* Bell Laboratories, Lucent Technologies; *E. Garfunkel,* Rutgers University; *S.B. Christman, E.E. Chaban,* Bell Laboratories, Lucent Technologies

The need for uniform and ultra-thin silicon oxides in microelectronics requires a fundamental understanding of the initial oxidation of both clean and H-passivated (HF-etched) silicon in oxygen. We have undertaken a systematic infrared absorption study of molecular O@sub 2@ and atomic O oxidation of H-passivated flat and vicinal Si(111) and Si(100) surfaces. Using an IR transmission geometry for full access to Si-O stretch (900-1250 cm@super -1@) and Si-H bending (600-850 cm@super -1@) modes, we can directly observe the incorporation of oxygen even after H-desorption under ultra-high vacuum conditions. Furthermore, hydrogen at steps can be spectrally distinguished from H on terraces, thus making it possible to correlate the kinetics of H elimination with oxide formation as a function of surface structure. We find that upon 1 Torr exposure at 300@super o@C, the bonding of step hydrogen is preferentially altered on the H/Si(111) surface, with dihydride steps being the most reactive. Yet, the rate of oxidation does not scale with the step density, indicating that direct oxidation of terraces takes place simultaneously. For the Si(100) surface, we contrast the oxidation of the HF-etched (atomically rough surface) with that of the smooth H-Si(100)-(2x1) surface prepared in HHV and that of the clean Si(100)- (2x1) surface in order to extract the mechanism for molecular O@sub 2@ dissociation.

8:40am **DI+EL+MS-ThM2 New Oxidation Process Using Collimated Hyperthermal Ozone Beam**, ***T. Nishiguchi,*** *Y. Morikawa, M. Miyamoto,* Meidensha Corporation, Japan; *H. Nonaka, A. Kurokawa, S. Ichimura,* Electrotechnical Laboratory, Japan

As the electronic devices are scaled down, using more reactive process gas than molecular oxygen is required to fabricate an ultra-thin highly reliable Si dioxide film for the gate oxide in MOSFET. We used ozone as an oxidant gas and achieved the enhanced initial oxidation rate, resulting in lower temperature oxidation process. In our experiments using highly concentrated ozone gas, more than 3nm Si dioxide film was obtained within 30 minutes under the conditions of 873K of Si temperature and 10Pa of ozone pressure, where the oxidation hardly proceeds by molecular oxygen. In the present study, we carried out the laser ablation of solid ozone in order to obtain collimated ozone beam on the purpose of applying ozone beam to new oxidation processes such as local oxidation of patterned Si surface (e.g. oxidation of a bottom part of a trench). We irradiated a KrF pulsed excimer laser light to highly concentrated solidified ozone that was adsorbed on the sapphire plate cooled down to 30-60K by cryocooler in an UHV chamber. We could obtain collimated ozone beam (within 20° spread) whose supply (typically 10@super 16@ molecules per laser pulse), concentration (typically 70%) and translational energy (3eV maximum) were controlled through the laser ablation conditions such as the laser fluence. Not only the local oxidation but also even lower temperature process is expected using this high-translational-energy (hyperthermal) ozone beam. We will demonstrate the initial oxidation profile for the first 1000 laser shots by Auger Electron Spectroscopy and discuss the applicability of this ozone beam to the semiconductor process.

9:00am **DI+EL+MS-ThM3 Nondestructive Investigation of the Si/SiO2 Interface by Spectroscopic Ellipsometry, Reflectance Difference Spectroscopy, Second Harmonic Generation, and X-ray Photoelectron Spectroscopy**, ***J.F.T. Wang,*** *J.W. Keister, Y.M. Lee, G. Lucovsky, J.E. Rowe, D.E. Aspnes,* North Carolina State University

We report results of a systematic study with various nondestructive techniques of buried interfaces between Si and thin gate oxides thermally grown at 700C and rapid-thermal-annealed at temperatures to 900C. The objectives are to understand the optical properties, the step structure, and the nature of the chemical bonding of the interface and to determine the limits to which the various nondestructive probes, alone and in combination, can provide this information. We examine in particular data obtained as a function of heat treatment and surface orientation (miscuts 2, 4, 8, 10 degrees off (001) toward the nearest (111); (113); (111); and (110)), with emphasis on the vicinal (001) orientations. The RD spectra of all as-oxidized vicinal (001) samples decrease by nearly a factor of 5 for the 900C RTA, indicating step-density reduction and a net smoothing of the interface. Except for the 2 deg sample, which shows basically no signal, these spectra become essentially identical to the spectra of chemically etched, H-terminated vicinal (001) surfaces. All such spectra have the appearance of RD lineshapes obtained on (113) surfaces, which are nominally dominated by double-height steps. The ellipsometric data differ mainly in overlayer thickness, but interface information can be extracted through least-squares analysis assuming interface spectra of Si in amorphous and +1 and +2 charge states. To assist in this analysis we orthogonalize the fitting parameters to determine which combinations are best determined by the data. The results indicate that the best reference data are those obtained on H-terminated (111) surfaces. The interface XPS spectra become much more consistent after rapid thermal annealing, with the (001) and (111) spectra being dominated by Si in +2 and +1 charge states, respectively, as expected. This provides further evidence of a reduction in roughness with annealing.

9:20am **DI+EL+MS-ThM4 Core-level Photoemission of Interface States on SiO@sub 2@/Si: Substrate Orientation Effects**, ***J.E. Rowe,*** Army Research Office; *J.W. Keister, J.F.T. Wang,* North Carolina State University; *G.J. Jackson, T.E. Madey,* Rutgers University; *D.E. Aspnes,* North Carolina State University

High resolution soft X-ray photoelectron spectroscopy (SXPS) with synchrotron radiation is used to study the interface of mis-cut SiO@sub 2@/Si(100) [i.e. stepped interface] of device quality ultrathin gate oxides. Our studies were performed on thin oxides grown by thermal oxidation in pure O@sub 2@ at a temperature of 600@degree@C and pressure of ~760 Torr. Our data can be well described by five different Si species due to Si in different oxidation states which are usually labeled Si@super 0@, Si@super +1@, Si@super +2@, Si@super +3@, and Si@super +4@. We have studied a number of samples prepared as described above and find that the energies relative to the Si0 peak are 0.95 eV, 1.80 eV, 2.50 eV, and 4.00 eV for the Si@super +1@, Si@super +2@, Si@super +3@, and Si@super +4@ peaks respectively. For this study, we define the transition region as the region containing Si in intermediate oxidation states (Si@super +1@, Si@super +2@, Si@super +3@). We find a transition-region Si suboxide concentration of 1.3 x 10@super 15@ cm@super -2@ assuming an escape depth of ~7 @Ao@ at a photon energy of 200 eV for samples annealed after growth at temperatures of ~900 @degree@C . This transition region is that in excess of the density ~1 monolayer of Si@super +1@ expected for the most abrupt SiO@sub 2@/Si(111) interface in terms of the Si(111) layer density of 7.8 x 10@super 14@ cm@super -2@. The I@sub 1@ interface peak is largest for (111) and decreases substantially for (113), (110), and for stepped (100) substrates. The total interface density appears to be lowest for Si(100) with a modest step density introduced by a 2@degree@ mis-cut. The step-dependent behavior is consistent with that reported using second harmonic generation. The total concentration of suboxide derived from SXPS data is dependent on the uniformity of SiO@sub 2@ films as well as data modeling, i.e., fitting of the data; both will be discussed.

9:40am **DI+EL+MS-ThM5 Spectroscopic and Electrical Characterization of the Evolution of Chemical Oxides Into Ultrathin Gate Oxides**, ***J. Eng, Jr.,*** *R.L. Opila, J.M. Rosamilia, J. Sapjeta, Y.J. Chabal, B.E. Weir, P. Silverman, T. Boone, R.L. Masaitis, T. Sorsch, M.L. Green,* Bell Labs, Lucent Technologies

The goal of this study is to understand how the structure of wet chemical oxides change during oxidation, and to determine whether the quality of ultrathin oxides is sensitive to the type of of wet chemical treatments. Four wet chemical treatments were examined: 1. standard RCA, with an SC1 step (ammonium hydroxide and peroxide) followed by an SC2 step (hydrochloric acid and peroxide), 2. modified RCA, with an HF etch between the SC1 and SC2, 3. ozonated water, and 4. HF. X-ray photoelectron spectroscopy (XPS) and infrared spectroscopy (IR) have been used to probe the structure and composition of the wet chemical oxides. IR probes the long range order in the films, while XPS probes the local Si stoichiometry. Both techniques show that the ozone oxide has the highest quality. Despite large differences in the initial quality of the wet chemical oxides, rapid thermal oxidation of the chemical oxides produces oxide films that are spectroscopically similar. Electrical properties of the oxides will correlated with the spectroscopic studies.

10:00am **DI+EL+MS-ThM6 Studies on Accurate Determination of the Physical Thickness of nm Gate Oxides and its Correlation with the Electric Thickness**, ***D.W. Moon**, H.K. Kim, H.J. Lee, H.M. Jo,* Korea Research Institute of Standards and Science, Korea*; H.S. Jang, H. Hwang,* Kwangju Institute of Science and Technology, Korea

Accurate Determination of nm gate oxides is critical for the development of nanoelectronic devices as well as for CMOS device scaling beyond 100 nm. In semiconductor industries, the thickness of gate oxides has been measured by ellipsometry. However, the accuracy has been not evaluated especially for gate oxides thinner than 10 nm. Recently, TEM and spectrometric ellipsometry(SE) have been used to measure the physical thickness of nm gate oxides and the electric methods such as I-V an C-V have been modified to include quantum effects. In this work, to estimate the uncertainty and improve the accuracy of the methods used for gate oxides thickness determination, TEM, SE and Medium Energy Ion Scattering Spectroscopy(MEIS) were used to determined the physical thickness of 6 gate oxides from 9 nm thick to 1.5 nm native oxide thick. MEIS can analyze the composition and structure of ultrathin films with atomic layer depth resolution. It was investigated that MEIS can be a reference for gate oxide thickness determination down to 1-2 nm. The difference of the physical thickness determined with TEM, SE and MEIS were discussed and compared with the electric thickness determined by I-V and C-V methods. For the gate oxides studied, the thickness determined by the Si MEIS peak was 1.5 nm thicker than that by the O MEIS peak. The thickness determined by SE and TEM was between the two values, while SE gave ~0.5 nm higher thickness than TEM. However, with the interlayer thickness, TEM thickness approached that of Si MEIS peak thickness. The electric thickness determined with I-V and C-V was close to that of Si MEIS peak thickness within 0.2nm. The thickness by SE is quite sensitive to the refractive index value used for fitting, especially for gate oxides thinner than 5nm. Based on this multi-disciplinary approach, it will be discussed how to provide standards for nm gate oxides approaching the limit of CMOS and how to transfer the standards to SE which is widely used in semiconductor process lines.

10:20am **DI+EL+MS-ThM7 Bonding of Nitrogen in Silicon Oxynitride Films**, ***R.L. Opila**, J. Eng, Jr., Y.J. Chabal, K.T. Queeney,* Bell Laboratories, Lucent Technologies*; J.P. Chang,* University of California, Los Angeles

Silicon oxynitride is a promising candidate to replace silicon dioxide in the next generation of microelectronic devices, but key aspects of the nitrogen chemistry in this material remain unresolved. This talk describes a twofold approach for understanding nitrogen bonding in these materials. The first approach employs surface analytical techniques, including photoelectron spectroscopy, infrared spectroscopy and near edge x-ray absorption fine structure, to study how oynitride precursors, suchas as nitric acid, nitromethane, and ammonia, react with silicon surfaces. The second approach uses the previous analytical techniques, along with electron spin resonance spectroscopy, to compare the nitrogen bonding states in silicon oxynitride and silicon nitride films prepared by thermal growth and ion implantation. Significant differences in the distribution of nitrogen bonding states and point defects are observed and correlated with the method of film preparation.

10:40am **DI+EL+MS-ThM8 Photoemission Investigation of Nitrogen Incorporation at the Si/SiO@sub 2@ Interface**, *J.E. Rowe,* Army Research Office*; **J.W. Keister,*** North Carolina State University

Monolayer incorporation of nitrogen at the Si/SiO@sub 2@ interface enhances the reliability and electrical characteristics of this nearly perfect interface for ultrathin SiO2 layers.@footnote 1@ In this paper we demonstrate that the Si(100)/SiO@sub 2@ interface is chemically sensitive to the nitrogen concentration. The nitrogen (1s) Soft X-ray Photoemission Spectroscopy (SXPS) peak was measured for varying degrees of N incorporation using the Advanced Light Source synchrotron at LBL National Lab. The broad width of the N(1s) SXPS peak lineshape is consistent with a large degree of final-state, Gaussian phonon broadening, and is comparable to O(1s) line. However, unlike the O(1s) line which is not especially chemically sensitive, the N(1s) line shows a clearly measureable, interface peak shift@footnote 2@ with increasing N incorporation. The average interface peak binding energy is ~0.75 eV greater than that recently reported for thick "bulk" films of Si3N4 with Al-K" XPS. To a lesser degree, the peak shape is seen to change as well. In particular, the peak width minimizes near to the value ~1.0 ML N incorporation, which is also the level at which devices interfaces perform best electrically. @FootnoteText@ @footnote 1@ G. Lucovsky, A. Banerjee, B. Hinds, B. Claflin, K. Koh, H. Yang. J. Vac. Sci Technol. B 15(4) 1074-1079 (1997). @footnote 2@ J. W. Keister, J. E. Rowe, J. J. Kolodziej, H. Niimi, H.-S. Tao, T. E. Madey, G. Lucovsky. J. Vac. Sci Technol. A 17(4) 1250-1257 (1999).

11:00am **DI+EL+MS-ThM9 Investigation of Fluorine in Dry Ultrathin Silicon Oxides**, ***G. Vereecke**, E. Röhr, R.J. Carter, T. Conard, H. Dewitte, M.M. Heyns,* IMEC, Belgium

As critical dimensions of integrated circuits continue to decrease, insulators with dielectric constants higher than silicon dioxide will be introduced in capacitors and transistors. However an ultrathin (< 1 nm) silicon oxide layer will generally be needed at the interface between Si and high-k layers. In cluster tools integrating surface preparation and dielectric deposition, vapor HF chemistries are envisaged to etch the native oxide prior to oxide growth. This HF etch leaves F on the surface of the Si wafer, which gets incorporated into the growing oxide. In addition, the silicon subsurface has also been proposed as a source of the F found in these oxides. The presence of F may be beneficial or detrimental for the properties of these layers depending on application, F location, and layer thickness. We have evaluated the sources of F in ultrathin oxides grown by UV/O2 at room temperature in an experimental vapor phase cleaning tool. Surface pretreatment was either by in-situ HF/methanol vapor process or by ex-situ wet HF dip followed by a DIW rinse. Evidence was found for F cross-contamination from the tool gaspanel when the HF etch step was performed in-situ. After correcting for this, F atomic concentrations in oxides grown on vapour HF and wet HF treated surfaces were of about 5 % and 2 %, respectively. The former would lower the dielectric constant of the layer if homogeneously distributed. The level of F contributed by the subsurface was estimated with oxides grown on wet HF treated surfaces in a specially built quartz chamber with no F contamination. No F was detected in these oxides, which indicates that the level of subsurface F is lower than previously reported. Ultrathin oxides continued to grow when exposed to air. This raises concern about their stability during the deposition and annealing of high-k layers. XPS results suggest that this is related to the exchange of labile F groups in the films.

11:20am **DI+EL+MS-ThM10 Studies on Electrical Properties of Ultrathin Oxides of Silicon Grown by Wet Oxidation at Low Water Vapor Pressure**, ***V.K. Bhat**, K.N. Bhat, A. Subrahmanyam,* Indian Institute of Technology, India

The rapid downscaling of the device dimension has increased the interest in the ultrathin (< 5 nm) oxides of silicon. Ultrathin oxides with thickness uniformity and good electrical properties are required for the silicon submicron devices. In general, the dry oxidation is being followed to grow these ultarthin oxides. Wet oxidation is not considered for the growth of ultrathin oxides of silicon because of the following reasons: i) high growth rate associated with the conventional wet oxidation at 1 atm. water vapor pressure and ii) large density of electron trapping centres present in the wet oxide. In the present study we report the results on the electrical properties of ultrathin oxides of silicon grown by wet oxidation at low (0.04 atm.) water vapor pressure. Ultrathin oxide of silicon is grown at 900°C on n-type single crystal silicon, single side polished, (100) oriented and having 1-10 @ohm@ cm resistivity (procured from M/s Wacker GmbH, Germany). The grown ultrathin oxides are characterized for their electrical properties by fabricating MOS tunnel diodes (aluminum is thermally evaported with a metal mask on to the ultrathin oxide). The capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) charcteristics of the MOS tunnel diodes are studied. The interafce state density (D@sub it@) and the density of the fixed oxide charge (Q@sub f@) are being calculated. The grown ultrathin oxide thickness is estimated from the measured C-V characteristics and are in the range 2.5-5.0 nm. The oxide growth rate is found to be linear. The charge trapping characteristics of the ultrathin oxides are studied by using consatnt current stress (CCS) technique. The decrease in the gate voltage is observed with the stress time. This observation may be attributed to the positive charge trapping in the oxide during the CCS. The charge trapping is found to be oxide thickness dependent and it decreases with the decrase in the oxide thickness.

11:40am **DI+EL+MS-ThM11 Properties of SiO@sub 2@ Thin Films Deposited at Low Temperature on SiGe and Si Samples in O@sub 2@/TEOS Helicon Plasmas**, ***A. Goullet**, D. Goghero, V. Fernandez, A. Granier,* Institut des Matériaux Jean Rouxel, France*; F. Meyer,* Université de Paris XI, France*; G. Turban,* Institut des Matériaux Jean Rouxel, France

Silicon dioxide thin films are deposited at low pressure (< 5mTorr) and temperature (<200° C) on Si@sub 1-x@Ge@sub x@ epi-layers and silicon substrates in oxygen rich O@sub 2@/TEOS helicon plasmas. The growth of SiO@sub 2@ films and the evolution of the interfacial layer under applied radio frequency bias voltage (0, -100, -200 V) are investigated using a UV-

Visible phase modulated ellipsometer (1.5-5 eV). The structural properties of the films are studied using infrared transmission spectroscopy, wet chemical etching and spectroscopic ellipsometry. Very thin (<10 nm) SiO@sub 2@ films deposited in the same conditions are investigated by X-ray photoelectron spectroscopy and spectroscopic ellipsometry to gain better insight of the oxide/semiconductor interface. The ion energy is found to be a significant parameter both for film properties and deposition rate. Use of radio frequency bias is effective in producing high quality SiO@sub 2@ films but an amorphized transition layer is detected in this case as evidenced by ellipsometric data modeling. The increase in the ion energy is also responsible for the presence of an additional oxidation state which appears on the Ge 3d XPS peak. Complementary capacitive C(V) measurements of grown oxides have been performed using metal-oxide-semiconductor samples. An increase in the fixed oxide charge and interface state densities as a function of the applied bias voltage is observed for silicon substrates whereas the electrical properties of the films deposited on Si@sub 1-x@Ge@sub x@ are rather insensitive to the deposition conditions.

Dielectrics
Room 312 - Session DI+EL+MS-ThA

High K Dielectrics: Perovskites
Moderator: J.N. Kidder, University of Maryland

2:00pm **DI+EL+MS-ThA1 High Density Thin Film Ferroelectric Nonvolatile Memories**, ***R. Ramesh,*** University of Maryland **INVITED**

Over the past two years, we have focused considerable effort on understanding the deposition and characterization of conducting barrier layers for the direct integration of ferroelectric capacitors on a poly-Si plug. Our specific focus has been on the materials science of the barrier layers to understand the role of crystallinity and process parameters on the structural and chemical integrity of the barrier layers during the subsequent growth of the ferroelectric capacitor stack. We are using the PZT system with conducting oxide electrodes as a prototypical test system for which at least two different conducting barrier materials systems have been successfully developed. Using both epitaxial and polycrystalline capacitors on these conducting barriers as test vehicles, we have been carrying out systematic studies on the effect of composition, point defect chemistry, strain and other processing variables on the structural integrity and ferroelectric properties. A novel aspect of our work is the use of scanning electric force microscopy techniques to understand the microscopic influence of film microstructure on the ferroelectric properties. In this presentation, we will present results of our progress on the process integration, device properties, specifically, polarization switching and relaxation dynamics and microscopic observations of ferroelectric properties and time dependent changes ; stress effects on fundamental properties.This work is supported by the NSF-MRSEC under Grant No. DMR- 96-32521 and by Bellcore.

2:40pm **DI+EL+MS-ThA3 Process Window Extension of TiN Diffusion Barrier using Pre-oxidation of Ru and RuO@sub x@ Film for (Ba,Sr)TiO@sub 3@ Dielectric Film**, *H.J. Kim, S. Kim,* Hyundai Electronics Industries Co. Ltd., Korea

(Ba,Sr)TiO@sub 3@(BST) thin film and other high dielectric oxides have attracted considerable attention due to their possible application in dynamic random access memories. However, serious integration issues are faced with in many cases because BST films need to be grown at rather high deposition or post-annealing temperatures of above 600°C in an oxidizing ambient. Deterioration of capacitor performance may result from interdiffusion and oxidation. Therefore, a diffusion barrier for oxygen should be developed for high-density DRAM device. In order to extend the process window of conventional sputtered TiN diffusion barrier and find out a proper electrode, in this experiment, the effect of pre-annealing method on the oxidation behavior of TiN barrier during 2 step annealing for BST dielectric film. Rapid thermal annealing in oxygen ambient (RTO) and N@sub 2@O plasma oxidation was respectively introduced to form a thin RuO@sub x@ layer and bind between oxygen and Ru at the surface of each Ru and RuO@sub x@ film. It is expected that a thin RuO@sub x@ layer be formed at the surface of each film by RTO and N@sub 2@O plasma. This can be retarded the oxygen indiffusion through Ru and RuO@sub x@ layer at high temperature due to complex diffusion paths and strongly stuffed along the grain boundaries as well as matrix. Two steps annealing for BST dielectric film is recently introduced to minimize the oxidation of diffusion barrier. In this work, a role of thin RuO@sub x@ oxidized layer formed at the surface of each Ru and RuO@sub x@ film by different pre-annealing methods prepared with/without BST deposition is investigated during two steps annealing.

3:00pm **DI+EL+MS-ThA4 Atomic Polarization and Screening Charge by Variable Temperature Scanning Probe Microscopy of Ferroelectric Surfaces**, ***S.V. Kalinin,*** *D.A. Bonnell,* University of Pennsylvania

Atomic force microscopy (AFM), electrostatic force microscopy (EFM), scanning surface potential microscopy (SSPM) and piezoresponse imaging (PRI) are applied to the BaTiO3 (100) phase transition. The imaging mechanism for non-contact microscopies (EFM and SSPM) based on an analytical solution for potential and field above the surface is discussed. The PRI imaging mechanism on a ferroelectric surface is analyzed in terms of the solution of the combined electrostatic-piezoelectric indentation problem. The relationship between SPM signal and screened and unscreened charge density is established. Quantification of force and force gradient-distance dependencies indicate that polarization bound charge is screened on this surface when imaged in ambient environments. The absolute value of the measured potential difference between domains of opposite polarity suggests that surface adsorbates play the governing role in surface potential. This conclusion is corroborated by a direct measurement of the phase transition and by observations of domain wall motion. The influence of tip shape effects and mobile surface charges on effective domain wall width is also discussed. The contribution of electrostatic forces to piezoresponse contrast is extracted from force-distance measurements and its influence of the local hysteresis loops is estimated. Considerations regarding the polarization switching by the tip are presented. Based on the experimental observations for this and other systems the dominant role of electromechanical vs. electrostatic effects in PRI imaging mechanism is established.

3:20pm **DI+EL+MS-ThA5 Film-formation Mechanisms, Microstructure, and Properties of BST Thin Films Grown By MOCVD**, ***Y. Gao,*** Pacific Northwest National Laboratory **INVITED**

A review of MOCVD BST thin films will be presented, focusing on precursor chemistry, film-formation mechanisms, and relationship between film processing, microstructure and dielectric properties. In particular, the precursor chemistry and film-formation r eactions have been studied using isotopic labeling experiments (@super 18@O@sub 2@). The precursor chemistry was found to strongly depend on substrate materials. In an oxygen ambient, at least four different reaction processes involved the removal of carb on from the precursor ligands on oxide covered Pt(111). Time-of-flight secondary ion mass spectrometry reveals both M@super 18@O and M@super 16@O (M= Ba, Sr, Ti) in the BST films, indicating that the oxygen in the BST films originates from both the gas ph ase oxidants (@super 18@O), and the precursor ligands (@super 16@O). The ligand substitution by gas phase O@sub 2@ plays a more prominent role in the film-formation at lower temperatures. On the other hand, the reactive oxygen radicals produced by micr owave plasma involved more in breaking the O-C bonds than substituting the precursor ligands for the film formation, resulting in larger surface roughness. Use of the 50%@super 18@O@sub 2@-50%N@sub 2@@super 16@O mixture results in a reduction of @super 18@O incorporation in the BST films, indicative of the direct involvement of N@sub 2@O in the film-formation reactions. The mechanistic studies are essential for understanding the BST precursor properties, and provide useful information to correlate the fil m m icrostructure, step coverage, and dielectric properties with the precursor properties. In addition, the study shows that precursor reactivities strongly affect the step coverage on the 3D structure, but little effect on the microstructure, surface morphology, and dielectric properties of the stoichiometric BST films. These properties strongly depend on the film composition, substrate material, and growth temperature.

4:00pm **DI+EL+MS-ThA7 Epitaxial (Ba,Sr)TiO@sub 3@ on MgO for Room Temperature Microwave Phase Shifters**, ***C.L. Chen,*** *J. Shen, S.Y. Chen, C.W. Chu,* University of Houston*; F.W. Van Keuls, F. Miranda,* NASA Glenn Research Center*; J.C. Jiang,* Louisiana State University

Single crystalline ferroelectric Ba@sub 0.6@Sr@sub 0.4@TiO@sub 3@ thin films were epitaxially grown on (001) MgO by using pulsed laser ablation. Microstructure studies from x-ray diffraction and electron microscopy suggest that the as-grown films are c-axis oriented with their interface relationship of @sub BSTO@//@sub MO@. Edge dislocations were found through the entire interface in every 8 unit cell length. Microwave property measurements indicated that the room temperature coupled microwave phase shifter have achieved with phase shift over 200@super o@ at 23.675 GHz and a figure of Merit of about 55@super o@/dB. The room temperature dielectric constant and loss tangent were found to be 1688 and 0.008 and the tunability was 33% with 2.5V/μm. The result suggests that the performance of microwave phase shifter based on the epitaxial ferroelectric thin films on (001) MgO are closed to the practical applications in the wireless rf communications.

4:20pm **DI+EL+MS-ThA8 High Temperature Etch Processing for FeRAM MFM Capacitor Stack Fabrication**, ***L.G. Jerde,*** *A. Cofer, R.A. Ditizio, S. Marks, J.A. Meyer, K.A. Olson, S.P. DeOrnellas,* Tegal Corporation

The unique materials utilized in FeRAM MFM capacitor stacks present numerous integrated device fabrication challenges, particularly in the patterning of these materials and the capacitor stacks that utilize them. Many of these patterning challenges are due to the intrinsic involatility of the reaction products formed when etching the elemental constituents of the FeRAM materials (i.e., Pt, Ir, Pb, Zr, Sr and Bi). These challenges have been successfully met for several years by utilizing photoresist etch masks in conjunction with the plasma etch technologies of low pressure, high density and dual frequency. While this technological approach is extendible

for the foreseeable future of FeRAM capacitor stack definition, the intrinsic involatility of their etch reaction products has recently sparked wide spread interest in utilizing high temperature etch processes to meet the as yet undefined future requirements for these applications. Although there are benefits to this high temperature approach, there are also risks. Among these risks are a number of key considerations that must be dealt with to successfully develop and implement high temperature etch process solutions for FeRAM applications. The first set of these considerations is related to the requirement that the etch tool provides reliable wafer, as opposed to wafer chuck, temperature and temperature uniformity control. In view of the industry trend toward single mask, full stack processes, another set of considerations is the requirement that the etch tool be able to rapidly vary the wafer temperature to accommodate the optimum temperature for each of the FeRAM materials being used. Yet another set of considerations are those related to wafer temperature limitations imposed by the Perovskite structure transition temperature, device damage and thermal budget. We will discuss and illustrate these considerations and present selected high temperature etch process results for various FeRAM films and stacks.

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