Plasma Science and Technology
Room 311 - Session PS2-MoA

Plasma Etching of Conductors

Moderator: A. Kornblit, Bell Laboratories, Lucent Technologies

2:00pm **PS2-MoA1 Gate Engineering for sub 50 nm CMOS Devices**, ***J. Foucher,*** CNRS/LTM, France; *G. Cunge,* CEA/LETI, France; *D. Fuard, R.L. Inglebert, L. Vallier, O. Joubert,* CNRS/LTM, France

In less than ten years, we will be approaching the limits of the CMOS technology with typical gate transistor length of less than 30 nm. In the past, gate etch processes have been optimised to provide perfectly straight sidewalls while maintaining the selectivity to the ultra-thin gate oxide (less than 2 nm). Recently, a new approach has been proposed in which the process is tuned to obtain a silicon-based gate whose dimension is smaller at the bottom than at the top of the gate (notched gate). This new approach opens up the possibility of making gates with dimensions smaller than the ultimate resolution of the lithography. In this paper we discuss the mechanisms involved in the fabrication of notched gate. Experiments have been conducted on a very powerful plasma etch system dedicated to advanced studies. It consists in a Decoupled Plasma Source (DPS) from Applied Materials modified to host in situ diagnostics such as UV-visible ellipsometry, mass spectrometry, fast injection Langmuir probe and X-ray photoelectron spectroscopy (XPS). Oxide masked a-si gates are etched using a modified etch recipe allowing a lateral erosion of silicon to be obtained at bottom of the gate. This can be achieved by tuning the thickness and composition of the passivation layer formed on the silicon sidewalls (sidewall passivation layer engineering). The robustness of the sidewall passivation layer is reinforced in the first part of the process while, on the other hand, plasma conditions are tuned in the second part of the process to suppress the passivation layer. In a last step, lateral erosion of the silicon sidewall is possible at the location where no passivation layer has been formed. XPS data of the passivation layer formed at the different process steps will be shown as well as some details on the control of the notch depth. Finally some results showing gate dimension in the 20 nm range will be shown.

2:20pm **PS2-MoA2 Fabrication of 80 nm PN-poly/metal Gate on Ultra-thin 1.5 nm Oxynitride**, ***K. Kinoshita***, *S. Saito, Y. Saito, M. Narihiro, M. Ueki, H. Wakabayashi, Y. Ochiai, T. Mogami, Y. Hayashi,* NEC Corporation, Japan

A PN-poly/metal gate is thought to be the promising technology to embedded LSIs beyond 0.13 µm design rule. This paper describes about the 80 nm PN-poly/metal gate fabrication technique on ultra-thin 1.5 nm gate oxynitride. Mix & match resist pattern by a point-beam EB system (JEOL, JBX-9300FS) for sub-0.1 µm pattern, and a usual KrF lithography system for wider pattern were developed over CVD-SiO@sub 2@/W/barrier/PN-poly-Si/gate-oxynitride stack on "8 wafer. The resist mask was transferred to CVD-SiO@sub 2@ hard mask layer, and then the poly/metal stack etching were investigated with a single chamber of an ICP type etcher (AMAT, Silicon Etch Centura DPS). The use of N@sub 2@-rich N@sub 2@/SF@sub 6@/Ar gas system for W etching, and the use of HBr/Cl@sub 2@/O@sub 2@ gas system for TiN etching generated rectangular cross section. Then, the PN-Poly-Si layer was etched by HBr/O@sub 2@ gas system. There existed the important correlation between relative oxygen density change by an optical actinometry and the PN-poly-Si etching. As the O@sub 2@ flow increased, the oxygen density increased, and the local etching to the silicon substrate through the thin gate oxynitride effectively suppressed. However, the excess O@sub 2@ flow brought etching stop on P-poly-Si region. XPS analysis for the etched P-Si wafer showed that the thicker oxide formation on the P-Si wafer etched at the etching stop condition. These results indicated that the P-Si surface oxidation brought both the high etching selectivity and the etching stop. The thinner the gate oxynitride, the narrower the process margins. Finally, good device characteristics were achieved.

2:40pm **PS2-MoA3 Etch Rate Enhancement and Surface Roughening during W/Poly Si Stack Gate Etching Process**, ***H. Morioka***, *M. Nakaishi, T. Ishida,* Fujitsu Limited, Japan

W/Poly Si stack structure is one of the most promising candidates for gate electrodes of ULSI in the next generation because of its low sheet resistance and compatibility with self-aligned contact process. But most etching processes of W/Poly Si stack gate have some distinctive problems closely related to W and W etching byproduct, such as non-uniform etch rate enhancement, serious RIE-lag, and profile anomalies. We examined the catalytic effect of W and W etching byproducts on W/Poly Si stack gate etching. Our experiments were performed on a high-density plasma etcher. The chemistry was halogen-base and oxygen was used as an additional gas, which is sometimes utilized for increasing W etching selectivity to poly Si by inhibiting Si etching. An etching sample was poly Si or SiO@sub 2@ wafer on which a W chip was attached in the center. The W chip, which was the only source of W and W etching byproduct, was etched together with the sample wafer in the reaction chamber. The etch rates were measured as a function of distance from the W chip, and the surface roughness was measured by AFM. In this experiment, we found that W and W etching byproducts enhanced the etch rate of poly-Si and SiO@sub 2@, and the enhancement depended on distance from the W chip. The etch rate was maximum near the W chip. Besides, AFM observation revealed the increase of etch pits along grain boundaries on etched poly Si surface, and the increase of roughness of etched SiO@sub 2@ surface when they were etched with the W chip. These facts suggest that W etching byproducts and their fragments decomposed in the plasma are deposited on the sample surface and vary the etching characteristics.

3:00pm **PS2-MoA4 A Drift of Selectivity Depending on Chamber Seasonings in a Poly-Si/Oxide Etching Process using Inductively Coupled Plasma**, ***K. Miwa***, Fujitsu VLSI Ltd., Japan; *T. Mukai, M. Nakaishi,* Fujitsu Ltd., Japan

Chamber seasonings after plasma cleanings are useful to stabilize reactor conditions. However, etch-selectivities of poly-Si to oxide with the same recipe were found to drift depending on seasoning methods. After bare-Si wafers were etched with an ICP of HBr/O2 as Si-seasoning, over-etch rates of oxides with the ICP slightly raised and decreased to stop as Si-seasoning time was longer. In cases of blanket-oxide wafers were etched as Oxide-seasoning, over-etch rates of oxides hardly drifted. Over-etch rates of poly-Si were nearly constant after the Si-seasoning or the Oxide-seasoning. Consequently, the etch-selectivity of poly-Si to oxide drifted after the Si-seasoning. Optical emission intensity of SiBr/He in the over-etch plasma increased with increase of Si-seasoning time. Over-etch rates of oxides also drifted as functions of O2 flow rate and Bias Power to the bottom electrode of the ICP-Etcher. The Deposition formed on the oxides during over-etchings after the Si-seasoning were identified as sub-oxides of Si using X-ray Photoelectron Spectroscopy (XPS). These results suggest that etch-rates of oxides are enhanced and decreased by etch-products such as SiBrx (x=1, 2, 3) in the over-etching plasma derived from the deposition on the reactor wall. The deposition would be formed during the Si-seasoning. When SiBrx coverages of the oxide surface are smaller than saturated coverage, the over-etch rates of oxides would be enhanced due to formation of silicon-oxybromide assisted with incident ions toward the surface. In cases of SiBrx coverages are larger than saturated coverage, excess SiBrx react with Oxygen atoms in the plasma to deposit sub-oxides of Si on the oxide surface. The sub-oxides would inhibit or stop the over-etching of oxides.

3:20pm **PS2-MoA5 Novel Dry Etch Chemistries for Metals**, ***A. Orland***, Auburn University; *R. Blumenthal,* Auburn University, usa

Magentic metals are the principle components of the read/write heads and magnetic media of the data storage industry and are even finding their way into semiconductor processing. Although "lift-off" techniques, ion milling and non-specific plasma etches have proven adequate for the fabrication today's devices. These methods are simply not capable of fabricating the structures that will be required for the next generation of devices. Many promising chemistries have failed when involatile products form instead of the desired volatile products. This is likely the case for the etching of Fe and Co with CO/NH@sub 3@, where the formation of low vapor pressure dimeric species, such as Fe@sub 2@CO@sub 9@ (as opposed to the high vapor pressure monomeric species, FeCO@sub 5@) may be responsible for the low etch rates that have been previously reported in literature. Modification of the CO/NH@sub 3@ chemistry with the addition of methane, acetone, and/or H@sub 2@ to the mixture will be reported. Addition of these species is intended to result in both methyl and acetyl substitutions on the metal, which are known to inhibit the formation of undesirable, non-volatile, dimeric metal complexes. Other results will include the investigation of new chemistries, such as cyclopentadienyl-carbonyl- chemistries, which will explore entirely new classes of possible volatile metal products. In-situ monitoring with supersonic pulse, plasma sampling mass spectrometry will yield information about all chemical species (both monmeric and dimeric) in the plasma environment, hence, it will provide a basis for understanding the chemical mechanisms of both successful and unsuccessful new etch chemistries.

3:40pm **PS2-MoA6 Experimental and Modeling Results for Process Scaling from 200 mm to 300 mm Wafers**, ***S.C. Siu***, *D. Cooperberg, V. Vahedi, R. Patrick,* Lam Research Corporation

As the wafer fabrication industry begins to move from 200 mm to 300 mm wafers, the need arises to transfer existing processes both to larger wafers and to larger process chambers. Transferring a 200 mm baseline process to a 300 mm chamber is not trivial, but it is critical for quick ramp up from development to production. For next generation process chambers that can handle both 200 mm and 300 mm wafers, such as those from Lam Research Corporation, process scaling to larger wafers is less complicated because the chamber is fixed, but there are still issues which need to be understood. A successful process transfer will result in enormous savings in time and resources that can be better used to fine tune processes for 300 mm wafers, instead of re-establishing a 300 mm baseline process. Zeroeth order scaling principles previously derived and published by Lieberman and Lichtenberg@footnote 1@ are examined in this paper, and their applicability to practical process scale up are determined. Plasma parameters important in conductor etching, such as ion density, radical concentration, and sheath potential, were measured in a Lam Research 200 mm etch chambers and compared with measurements made in the next generation 300 mm etch chambers. Preliminary results show good agreement between the scaling predictions and plasma measurements. Modeling results show that reactor scaling parameters are application dependent. Scaling parameters for ion dominated etching may differ from those in which etch rate and profile evolution are more dependent on radical concentrations (e.g. resist trim, aluminum etch in chlorine). Additionally, predictions for process scaling may be dependent on the relative importance of radical depletion mechanisms (e.g. wall recombination, reaction, volume loss, pumping effects). @FootnoteText@@footnote 1@M. A. Lieberman and A. J. Lichtenberg, Principles of Plasma Discharges and Materials Processing, John Wiley & Sons, Inc. (New York, 1994), chapter 10.

4:00pm **PS2-MoA7 Improving Al Etch Processing in a High Density Plasma Reactor with a Faraday Shield**, ***D.A. Outka***, *S.C. Siu, N. Williams,* Lam Research Corp.

As etch geometries become smaller, the uniformity of the reactor environment becomes increasingly important in achieving consistent results within a wafer and from wafer-to-wafer. This study examines the addition of a Faraday shield (FS) to an HDP (high-density plasma) reactor to aid in achieving this goal. The effect of the FS on Al etching is examined with wafer-level, plasma, and electrical diagnostics. The FS is an electrostatic shield inserted between the RF coil and the plasma. With this shield there is approximately a 10% reduction in the Al and oxide etch rates depending upon the RF power. Langmuir probe measurements indicate that this reduction is due mainly to a decrease in the plasma density. Electrical measurements of the impedance of the load with a RF probe were also performed and the results compared with a circuit model. These results also indicate a reduced coupling between the RF coil and the plasma. Based upon these results the impact of adding a FS to a commercial etch tool in terms of wafer performance and productivity is discussed.

4:20pm **PS2-MoA8 Transfer Etch Profile Control for 248 nm Bilayer Thin Film Imaging**, ***S. Halle***, *R. Wise, J. Brown,* IBM Microelectronics*; O. Genz,* Infineon Technologies Corporation*; A. Thomas, T. Dyer,* IBM Microelectronics*; A.P. Mahorowala, M. Angelopoulos,* IBM T.J. Watson Research Center*; S. Johnston,* Lam Research Corporation

The technique of bilayer thin film imaging and transfer etch is expected to play an important role for extending 248 nm lithographic patterning to 135 nm and below feature sizes. Previous studies have demonstrated the utility of an O@sub 2@/SO@sub 2@ process in a poly TCP reactor to anisotropically etch the patterned resist through a novolak-like underlayer selective to a Si-containing imaging layer. In this study, both the width and profile control over a range of aspect ratios of a bilayer transfer etch for a 135 nm contact-like deep trench (DT) mask level and a equal line-space (LS) mask printed over severe topography, are examined. Transfer etch studies show that both the profile and the width of the etched feature can be controlled by both the ratio of O@sub 2@/SO@sub 2@ and the bias voltage in the TCP reactor to produce a zero bias vertical profile. The linewidth of the etched feature can be tailored with a positive or negative slope by either decreasing or increasing the ratio of O@sub 2@/SO@sub 2@, respectively, or decreasing or increasing the bias voltage, respectively. As the aspect ratio of the underlayer etch is varied from 5 to 8 in the DT level or as the feature is over-etched by 30%, the linewidth of the etched feature is unchanged. As the lithographic alignment of the LS mask level is incrementally varied with respect to a recessed trench from a previously patterned DT level, the transfer etch can be examined to aspect ratios >10, resulting in a minimum effective width of approximately 25 nm However, at the highest aspect ratios, the trajectory of the transfer etch is observed to be shifted from normal incidence by as much as 45 degrees. Semi-empirical models are used to examine the origin of the altered trajectory of the ions, by determining the relative contribution of ion shadowing from the geometric asymmetry of the transfer into the recess and of the charging effect from thin dielectric films along the sidewall.

4:40pm **PS2-MoA9 Conductor Stack Etching: Technology and Productivity**, ***R.A. Gottscho***, Lam Research Corporation **INVITED**

Conductor etching in the semiconductor industry includes front-end applications such as gate and shallow trench stacks as well as back-end interconnect structures. Future applications center around new materials for gate stacks, to accomodate decreasing voltages and dielectric thickness, and high-k dielectrics, to enable higher density and powerless storage. The technological requirements in gate stack etching center on within wafer critical dimension, CD, control; but, production considerations demand equal attention to wafer-to-wafer, lot-to-lot, and machine-to-machine CD uniformity. For within wafer CD uniformity, gas injection, pumping, plasma generation, and edge ring design all play important roles. However, the aspect ratio variations inherent in circuit design and doping variations within the stack or from stack-to-stack ultimately limit the process window. Waferless cleaning of the chamber and delivered power control provide effective means for minimizing CD variation during large volume production. To preserve the device integrity of ultra-thin gate oxides and maximize yield, novel pre-end-point detection is used with and highly selective over-etch processes. Shallow trench etching mechanisms appear identical to those governing gate stack etching, but by shifting the balance between etching and deposition, trench profiles can be tailored to meet demanding requirements for top rounding, bottom rounding, and side-wall-angle uniformity. In back-end etching, traditional trade-offs remain for resist mask stacks: vertical profiles without residues and charging damage. Hard mask metal etching offers wider process window but at higher cost. The primary focus in the back-end is output, to be gained by increased throughput and longer times between cleans. It is the latter that is driving innovative changes in reactor designs and materials.

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