Wednesday Afternoon, October 4, 2000

Manufacturing Science and Technology Room 304 - Session MS-WeA

Process Integration (Cu/Low-k/300mm)

Moderator: M. Surendra, IBM T.J. Watson Research Center

2:00pm MS-WeA1 Integration Challenges for Copper Metallization with Low-k Dielectrics, B.L. Chin, Applied Materials INVITED

The transition from AI metallization to Cu has been implemented during the past several years and successfully introduced into several device products. This has resulted in improvement in device chip speed due to the resistivity reduction. To further decrease the RC time delay and minimize cross talk between interconnect lines, the transition to low-k materials has been actively investigated but the implementation has not been as rapid or straightforward. The convergence of Cu metallization with low-k dielectric has been hampered by the difficulty in replacing the present SiO@sub2@ with a low-k material that meets all the film property requirements: mechanical, thermal and electrical compatibility. Key integration issues for the low-k material include dual damascene pattern definition, adhesion of the barrier/ seed and adequate planarization. A review of the various materials and technologies (PVD, CVD) to deposit the barrier/ seed will be presented along with the pre-clean methods to ensure low via resistance. A survey of the different barrier films and barrier testing will illustrate the need for evaluating not only out-diffusion of Cu into the dielectric but also the in-diffusion of other components from the dielectric (e.g. diffusion of F from FSG to Cu). The currently used Ta-based barriers will be compared with composite layered structures and new materials. The necessity for decreasing the seed layer thickness for electroplating fill has placed a greater demand on the step coverage and resultant interface properties. Recent advances in electroplating technology may resolve this issue and its impact on integration with low-k materials will be highlighted. These challenges will be further amplified with the introduction of porous low-k materials and may force the implementation of other technologies to satisfy the requirements for sub- 0.1 µm devices.

2:40pm MS-WeA3 Adventure of the first 300mm Pilot Line, M. Peschke, Semiconductor 300 GmbH&Co.KG, Germany INVITED

The transition in wafer size has always been a risky project in the past. Even for very sophisticated and wealthy companies it was a painful experience. Using the synergy of the know how and share the costs Infineon Technologies and Motorola announced in 1998 a Joint venture (Semiconductor 300) for a 300mm pilot line located in Dresden. Based on the standards provided by i300i and Selete (i.e. CIM/ Automation or FOUP requirements, process specifications), the equipment manufacturers could provide the simultaneous availability of all required tools. When SC300 started first test results were already available and the visibility "first sample of a working transistor" was already shown by Motorola. The factors to influence the productivity improvement of 30% per year, become smaller so the manufacturing effectiveness has to gain to keep the improvement rate. The focus was directed to reliability of the tools. whereas the process performance was assessed as a "must criteria". The equipment industry has grown tremendous in the last years so the financial strength and expertise has grown as well. All the new ideas of improvement which could not implemented in the existing tool set went into the design of the new generation. A key factor for the success of the SC300mm project has been the open relationship with the equipment suppliers. Jointly the tools were tested and stressed under manufacturing conditions. The technology which was used to ramp up the 300mm pilot line was a state of the art DRAM product. With the redundancy of a DRAM the impact of defect density is limited and so learning cycles were faster. With the help of the local infrastructure of the 200mm production line, which ran the same product, problems were solved faster. The success of the first 300mm pilot line nine month after tool installation, demonstrates the potential of the existing tool set.

3:20pm MS-WeA5 Cluster Formation on Copper Evaporated Onto Dow Cyclotene 3022, E. Sacher, D.-Q. Yang, S. Poulin, S. Rodrigues, L. Martinu, M. Meunier, Ecole Polytechnique, Canada

Dow Cyclotene 3022 is a low permittivity polymer used in the microelectronics industry. It is made through the Diels-Alder polymerization of bis-benzocyclobutene-terminated divinyl siloxane monomers. Key Cu integration issues concern the adhesion of patterned Cu lines and the stability of the Cu-polymer interface to metal diffusion. Photoacoustic FTIR and XPS have shown that the Cu atoms interact

asymmetrically with the aromatic rings of the Cyclotene to give weak bonding across the interface. XPS, XRD, AFM, TEM, spectroscopic ellipsometry, and other techniques, have shown that the Cu exists in the form of surface clusters. TEM micrographs, for example, show that a nominal 3.2 nm deposit exists in the form of irregular clusters with an average diameter estimated at 9 nm. This may be compared with an XPS estimate, based on an intensity comparison at two different orbital energies, which suggests that the clusters are spherical and about 7 nm in size. The weak bonding permits surface diffusion, which causes cluster coalescence on annealing, although there is no evidence, from any technique available to us, of diffusion into the bulk Cyclotene. The structure and properties of the Cu/Cyclotene interface will be compared with adhesion studies by microscratch and adhesive tape peel tests.

3:40pm MS-WeA6 FSG Film Characterization and Process Development for Copper/Damascene Technology, J.S. Martin, K.J. Taylor, J.D. Luttmer, A.R.K. Ralston, T.D. Bonifield, J.A. West, Texas Instruments, Inc.; C.T. Adams, K.-H. Chew, A. Bayman, B. van Schravendijk, Novellus Systems, Inc. The microelectronics industry is transitioning from wiring devices with aluminum and oxide-based interconnect structures to damascene-based integration, with both copper and low-k materials. Toward this end, we outline the process technology and material characterization for a fluorosilicate glass (FSG) developed specifically for copper/damascene technology, where both the via and metal line are embedded in FSG at six levels. We compare FSG deposited in both high density plasma (HDP) and standard PECVD reactors, for K values within the range 3.50 - 3.70. Fluorine loss and water absorption are appreciably less for HDP-FSG films. We note two additional issues for FSG processes and films. First, adhesion to subsequently deposited PECVD silicon nitride is problematic and delamination increases with thicker FSG films. Second, deposition temperature strongly influences in-film [F], but for systems without active wafer temperature control, wafer temperature, and hence in-film [F] depends on the substrate dopant concentration. We briefly outline our methods for actively controlling wafer temperature to ± 5°C during deposition and monitoring [F] in-line via X-ray fluorescence (XRF). HDP-FSG thin films are thus deposited with active temperature control, and in-film [F] is controlled to within ± 0.2 atomic percent, as measured by XRF. Most important, by systematically decreasing in-film [F] over a 25% range, we observe that K-value increases by 0.10 and adhesion to silicon nitride significantly improves. We view this as a viable FSG process, applicable at the 0.18 µm and 0.13 µm nodes.

4:00pm MS-WeA7 300mm Manufacturing Meterology Needs, R. Goodall, Sematech INVITED

PLEASE SEND US AN ABSTRACT. Thank you.

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