Thursday Afternoon, October 5, 2000

Manufacturing Science and Technology
Room 304 - Session MS-ThA

Advanced Modeling for IC Manufacturing

Moderator: E.G. Seebauer, University of Illinois, Urbana-Champaign

2:00pm **MS-ThA1 Challenges in Modeling & Simulation of Semiconductor Equipment & Processes**, ***A.K. Das,*** Applied Materials Inc. **INVITED**

Modeling & simulation of semiconductor manufacturing equipment & processes is an inherently multi-disciplinary effort drawing from such diverse fields as plasma physics/chemistry and heat and mass transfer. Over the past few years, significant strides have been made to address and incorporate several of these phenomena, and enable optimization of chamber geometry and processes through modeling. However, many of these physical phenomena occuring in processing equipment are not even well understood or characterized. Obtaining self-consistent models that combine the influences of different phenomena or different aspects of processes is perhaps the major hurdle between where we are now and taking comprehensive reactor models (or the Virtual Reactor) mainstream. There are several issues that must be resolved before comprehensive reactor models may become commonplace. The computer model must be able to handle stiff chemistry-equations and the resulting numerical convergence problems. In plasma modeling, the sheath must be resolved properly to predict the ion flux and energy at the wafer surface. The extension of fluid models into the transition regime must be incorporated in the commercial codes. Finally ways must be explored to combine the reactor level model with the device/feature level. Currently setting up a model may be very time-consuming due to the lack of smart grid generation tools. The proliferation of modeling to the common engineer cannot happen without streamlining and minimizing the grid-generation effort. Lastly, there is a lack of fundamental or often tool-specific data necessary to accurately simulate these processes. Most of the reaction mechanisms/pathways of relevance to real processes are not well understood. A long-term sustained research effort is required from chip-makers, equipment companies, academia, national laboratories and commercial software developers to overcome these shortcomings.

2:40pm **MS-ThA3 Modeling of Oxide CMP and Polish Pad Conditioning**, ***L. Jiang,*** Intel Corp., US*; H. Simka, S.S. Shankar, J. Su, K. Kumar, V. Murali,* Intel Corp.

A model for the mechanical and chemical aspects of oxide CMP is presented. We combined both contact mechanics and slurry flow in a physical model (Jiang & Shankar 1999) and compared the simulation results to recent studies on oxide CMP. Pad asperity deformation and slurry flow between asperities are modeled simultaneously. Dissolution and polish rates of oxide are modeled based on silica hydrolysis kinetics and calibrated with experimental data. Mechanisms of pad glazing and conditioning effect on polish rate are also discussed with a review of literature data. Pad glazing is a result of mechanical (cyclic polish stress) and chemical actions (oxidation of surface during polish). Pad degradation effects on polish rate over the wafer scale are predicted by combining pad fatigue model with mechanics/flow simulations. Relative motions between pad, wafer, and individual conditioner heads are simulated to predict pad conditioning effectiveness and pad age.

3:00pm **MS-ThA4 Mechanical Properties of a Cu-Ta Interface by Molecular Dynamics**, *P. Heino,* ***E. Ristolainen,*** Tampere University of Technology, Finland

During last few years, the electrical and mechanical properties of copper have received a lot of interest in the electronics community, mainly because of its low electrical resistance. Last year at AVS1999@footnote 1@ we discussed mechanical properties of nanoscale copper connection and concentrated on pure copper. In this work we study the microstructure and strength of the copper interface. To prevent diffusion of copper into silicon, a barrier is needed. Furthermore, the barrier-copper system should be immiscible. It seems that tantalum is used most often as a barrier metal, and it has the needed properties. Here we study the copper-tantalum interface by means of molecular dynamics method and embedded atom potential. In the model the cross term potential has been optimized to reproduce the experimental (small and positive) heat of alloy formation. The interface is formed by depositing Cu on different single crystal Ta surfaces. The microstructure and properties under shear of the resulting interface are analyzed. @FootnoteText@@footnote 1@P. Heino, P. Holloway and E. Ristolainen: Strength of Nanoscale Copper Under Shear, Accepted for publication, J. Vac. Sci. Tech. A (2000).

3:20pm **MS-ThA5 Integrating Process Models, Equipment Logistics, and Factory Flow for Manufacturing Systems Optimization**, ***L. Henn-Lecordier,*** University of Maryland, US*; M.-Q. Nguyen, B. Conaghan, P. Mellacheruvu, J.W. Herrmann, G.W. Rubloff,* University of Maryland

Technology change, yield learning, and market shifts all produce notable factory dynamics, yet anticipating the operational consequences of process changes and optimizing the overall system remains largely an ad hoc procedure. We have developed a heterogeneous simulation environment (HSE) which integrates process and operational dynamics from the unit process to full factory flow. Process models are incorporated as response surfaces which determine cycle times in corresponding equipment modules. In turn, the operational behavior of multiple modules on cluster tools is investigated through discrete event simulation for specific cluster tool architecture, module population, and scheduling algorithms. Finally, process and cluster tool models are incorporated into factory-level discrete event simulations (Factory Explorer). Management of process, equipment, and factory parameters, as well as model execution, is carried out through a simulation supervisor and its graphical user interface. These integrated models enable tradeoff analysis involving specific process parameters, cluster tool configuration and logistics, and factory flow as a function of tool populations. We have studied the specific example of a W plug process sequence, involving clean, PVD TiN liner deposition, and W CVD fill. Results indicate notable cycle time advantage for individualized cluster tool sequencing optimized for the chosen process parameters, as compared to using routine dispatching rules. The HSE also reveals the factory level operations consequences of re-entrant flow, where the dimensions of different interconnect levels produce different throughputs for different levels. Thus, the HSE presents a potentially valuable tool for rapid optimization in the presence of factory dynamics, usable by operations, equipment, and process engineers.

3:40pm **MS-ThA6 Plasma Reactor Simulation to Improve Film Deposition Uniformity**, ***K. Bera,*** *K. Liu,* Applied Materials, Inc.

A capacitively coupled plasma discharge has been simulated for an industrial reactor to investigate the uniformity of the film deposition profile on the wafer. The gap width between the powered cathode and the ceramic wafer pedestal is very small compared to the radius of the cathode. Non-uniform grid is used to resolve the sheath in the plasma for this reactor configuration. Silane is fed as a feed gas from the showerhead into the chamber at low pressure. The spatial distributions of electron, ion and radical densities, electron temperature and ion energy are obtained using Plasma Reactor Simulator (PRSim) code. The spatial distributions of radical flux and ion energy on the wafer are useful for the prediction of thin-film deposition rate. The effect of the distance of wall dielectric from the wafer edge on the surface process is also investigated. A mixture of silane and nitrous oxide is fed in the chamber to investigate the effect of silane dilution on the process. The present study is used to identify the reactor design condition to achieve uniform film deposition rate on the wafer.

4:00pm **MS-ThA7 First Principles Modeling of Gas-Surface Interactions in Low Pressure CVD Processes**, ***H. Simka,*** *S.S. Shankar,* Intel Corp.*; J.-R. Hill, S. Mumby,* Molecular Simulations, Inc.

Understanding and optimization of low-pressure CVD systems typically necessitate knowledge of interactions between gas-phase species and surface at the molecular level. A physically-based approach to model these interactions is presented. The approach is based on ab-initio quantum chemistry investigations of molecular and surface properties, as well as binding between reactive gas-phase precursors with atoms on the growth surface. Application of the method to low-pressure CVD of silicon nitride using dichlorosilane (DCS) and ammonia will be illustrated. Energetics of the gas-surface interactions are calculated using density-functional theory (DFT), with the surface represented by H-terminated clusters involving the active centers. Energy values obtained using DFT methods for this system are typically more accurate compared to those obtained using semi-empirical methods. For example, the activation barrier for gas-phase decomposition of DCS to SiHCl and HCl calculated using the PM3 semi-empirical method is 45 kcal/mole, which is significantly lower than values obtained using DFT and more accurate ab-initio methods such as G2 (65 to 68 kcal/mole). Other comparisons illustrating further limitations of the semiempirical method for modeling of gas-surface interactions will be presented. Reactivity of several surface sites in the cluster model is investigated. Adsorption energies of several gas-phase species are

calculated; accuracy of the several DFT methods used is evaluated and will be discussed.

4:20pm **MS-ThA8 Etching of Silicon in HBr Plasmas for High Aspect Ratio Features**, ***H.H. Hwang***, ELORET Corp.*; G.S. Mathad, R. Ranade,* Infineon Technologies, Inc.*; M. Meyyappan,* NASA Ames Research Center

Acquiring straight wall etching is a continuing goal in the semiconductor processing industry. Achieving a vertical wall with no bowing becomes extremely critical as dimensions decrease to less than 0.1 µm. Undercutting must be minimized in order to obtain closely spaced features of this size. Etching typically requires aspect ratios on the order of 20:1 (depth:width) and often higher than 50:1. At these small feature sizes and large aspect ratios, neutral shadowing becomes increasingly more important. Fewer neutral radicals which can passivate the substrate surface can enter the trench opening, which leads to a decreased etch rate and can limit the maximum obtainable aspect ratio (AR). In pure chlorine, for example, it is difficult to achieve ARs of more than 5:1. To date, however, most modeling efforts have not focused on the specific problems encountered in high aspect ratio etching. We will present results for etching silicon in HBr plasmas using a previously developed feature profile evolution simulation using a level set method (SPELS). We will compare calculated average etch rates, total etched depth, and RIE lag effects (etch rate dependence on feature size) in high aspect ratio trenches to experimental measurements. The measurements were made in a parallel plate, capacitively-coupled, magnetically enhanced reactor. We will also present comparisons in etch rates for different feature sizes (0.2 µm, 0.175 µm, and 0.15 µm). Comparisons of simulated etched profiles and experimentally obtained SEMS will also be presented.

4:40pm **MS-ThA9 Contamination Removal from Wafer with Deep Trenches**, ***H. Lin***, *A.A. Busnaina, I.I. Suni,* NSF and CAMP (New York Center for Advanced Materials Processing, at Clarkson University)

The International Technology Roadmap for Semiconductors shows the requirement for high aspect ratio (depth/width) trenches in DRAM trench capacitor technology. Cleaning high aspect ratio deep trenches is challenging because of the need to rinse or remove contaminants from the bottom of trench. In this work, based on the experimental and numerical study of blanket wafer cleaning, contamination removal from wafer with topography is studied using physical modeling. The rinsing flow and contaminant transport in the geometry are modeled by solving the governing momentum and mass conservation equations with associated boundary conditions. The rinsing of patterned wafer is accomplished using an oscillating flow past a series of high ratio rectangular trenches. The modeling results of flow past a series of trenches show a good agreement with the experimental results of Perkins. Oscillating flow rinse is found to be more efficient than steady flow rinse using the same average rinsing velocity. The effects of the aspect ratio, trenches size, and oscillating flow frequency on cleaning efficiency are presented.

5:00pm **MS-ThA10 In Situ Metrology for Cu Electroplating**, ***G. Barna***, Texas Instruments, US

This presentation will describe the use of the RTA (Technic, Inc.) system for control of a Cu plating bath in a SC productization environment. This tool is a robust, in-situ sensor that analyzes all the components of the bath by a variety of electroanalytical techniques. It consists of a probe that stays continually immersed in the main bath module of the plater, with the appropriate electronics and PC controller located within 25 ft. of the probe. A complex factory calibration scheme provides accurate measurements. The internally generated reference electrode and the rigorous electrochemical cleaning procedures provide long-term repeatability and reliability. Measurements of all 5 components are performed in ~ 15 minutes, making repeated measurements easy. Long-term sensor stability has been demonstrated. After a year of continuous use, this sensor has required no recalibration and virtually no maintenance. Bath control is greatly facilitated by the accuracy, repeatability and reliability of this sensor. Its CoO is minimal, there is no need for any standards or test solutions and its cleanroom footprint is no larger than a PC. Further development of this system, aimed to provide information over and above simple bath control, will also be described.

Author Index

Bold page numbers indicate presenter