Manufacturing Science and Technology
Room 304 - Session MS-MoA

Challenges in Semiconductor Manufacturing for the First Decade of the 21st Century

Moderator: C.R. Brundle, Applied Materials

2:00pm **MS-MoA1 Chips to Power the Peta-bit Network**, ***D. Eaglesham***[1], Lucent **INVITED**

The net continues to grow at a mind-boggling rate. 1999 was the first year that data traffic exceeded voice. Data traffic in North America continues to double every 6 months. This explosive growth is driven an apparently insatiable demand for bandwidth and continuing improvements in the underlying technology. Electronic switches are rapidly moving up the speed scale from Gb/s to 40 Gb/s, while wavelength multiplexing of these signals drives the capacity of a single fibre up from 10Gb/s, with experimental demonstrations in the multi-Terabit/s range. Bandwidth on a single fibre is likely to top out a little short of a Petabit/s within a few years. The basic technology for data manipulation remains the silicon switch. Transistor scaling has been responsible for much of our ability to move huge chunks of data. I will discuss the level of scaling required in the Pb/day era, and the new transistor structures required to overcome the key technical challenges facing CMOS scaling. I will also discuss the new technologies arising to deliver low-cost highly-integrated networking chips, in particular SiGe BiCMOS technologies. Finally, I will describe an assortment of new technologies including MEMS, and integrated waveguides and modulators, that are starting to change the very core of the network.

2:40pm **MS-MoA3 SOI or USJ?: Laminated Electronics for "Post-Roadmap" CMOS**, ***M.I. Current***, *S.W. Bedell, I.J. Malik, F.J. Henley,* Silicon Genesis **INVITED**

The many challenges that are projected in the ITRS99 study for fabrication of high-performance planar CMOS transistors on bulk Si for gate dimensions smaller than 60-50 nm (expected in year 2006-2008) clearly point to major changes in standard transistor design, materials and fabrication techniques. Various forms of laminated electronic substrates, beginning with Silicon-on-Insulator (SOI), provide a means to relax some of the process and materials constraints on bulk Si devices. SOI substrates also provide new design options, such as dual-gated channels and high-mobility buried channels. New technologies are now available to bond and cleave electronic materials layers with atomic layer control and surface roughness approaching 1 Å (RMS) without the need for CMP or other damage removal and polishing processes. The design and fabrication of complex laminated electronics "master slice" substrates, which can provide for integrated fabrication of opto-electronic circuits, will be illustrated with examples for such components as dual-gate CMOS, compliant substrates for III-V film growth and optical switching and coupling pathways.

3:20pm **MS-MoA5 The Viability of sub-50nm CMOS Technology**, ***G. Timp***, *J. Bude, F. Baumann, D. Muller, Y. Kim, M.L. Green, T. Sorsch, D.M. Tennant, R. Kleiman,* Bell Laboratories, Lucent Technologies*; W. Timp,* Massachusetts Institute of Technology*; P. Silverman, B.E. Weir,* Bell Laboratories, Lucent Technologies **INVITED**

The complexity of an integrated circuit (IC), measured by the number of transistors incorporated into the circuit, is constrained by power dissipation. The viability of sub-50nm CMOS technology, which promises to incorporated nearly a billion MOS transistors into one circuit, is contingent upon the drive current performance of the MOSFET as well as the off-state leakage current. We are obliged to pursue improvements in the drive performance to derate the power supply voltage, thereby reducing power dissipation while improving reliability. The drive current of a MOSFET is dictated by both the thickness of the SiO@sub 2@ gate dielectric and by carrier scattering in the channel. Reducing the thickness of the gate oxide increases the drive current by increasing the carrier density in the channel through an increase in the gate capacitance. However, the gate leakage current due to direct, quantum mechanical tunneling through the oxide renders SiO@sub 2@ thickness' less than 1.3nm impractical because the off-state leakage current becomes intoleralbe.@footnote 1@ Consequently, the drive performance for t@sub ox@>1.3nm is limited by ballistic transport in the channel. We have shown that ballistic transport (with transmittance T>0.80) can be achieved at room temperature in a silicon MOSFET operating with transverse electric fields at the inversion layer in the semiconductor >1MV/cm, provided that the deleterious effect of interface roughness scattering is mitigated by optimizing the transverse field and minimizing the channel length and interface roughness. This optimum illustrates the futility of alternative, high @kappa@ gate dielectrics that give rise to a channel mobility less than that found at the equivalent SiO@sub 2@ thickness or operate at higher transverse fields, and indicates that a more sophisticated design of the source, drain and channel doping profiles will be required to satisfy the drive specifications. @FootnoteText@ @footnote 1@ D. Muller et al., Nature, 399 (1999) 758.

4:00pm **MS-MoA7 Technology for Wired and Wireless Networks**, ***S. Subbanna***, *B. Meyerson,* IBM Microelectronics **INVITED**

In the first decade of this century, we can expect to see extraordinary growth in the availability of information bandwidth. Telecommunications providers and/or service providers will be expanding their capacity to provide increasing numbers and types of services at an ever cheaper rate. This will drive demand for high-speed wired and wireless ICs, and for the seamless connection of both. This talk will focus on the silicon-based process technology, packaging, and design infrastructure requirements for rapid development and supply of cost-effective solutions. In particular the manufacturing advantages of using a silicon (CMOS) base for this technology will be expounded. One technology that unites the cost-effective CMOS base with a high-performance RF NPN bipolar transistor is Silicon-germanium (SiGe) BICMOS. SiGe BICMOS has been used to combine many different RF and digital functions on a single chip. The drive for RF system-on-a-chip is great due to requirements of power, space, and weight reduction for cellular phones. We will discuss design of the SiGe BICMOS technology for manufacturability, as well as issues associated with bringing our 0.5, 0.25, and 0.18um technologies to production. The issues associated with use of CMOS technologies for RF applications will also be discussed, as well as tooling implications and requirements (which are slightly different than CMOS). The issues associated with simulation of (semiconductor) processes and device performance for SiGe BICMOS will also be discussed. We will also discuss challenges for improvement of yield and manufacturability of these technologies. We will also review the limits on silicon technology performance in the light of these new developments.

4:40pm **MS-MoA9 Process Integration Challenges in a Copper/Low-K World**, ***R.A. Powell***, Novellus Systems **INVITED**

It is generally agreed that the wiring of GigaHertz-class ICs will be a multilevel interconnect stack of Cu lines electrically insulated from each other by low-k interlevel dielectrics and assembled using a Damascene process flow. Significant progress has already been made on unit processes needed for 0.10-0.13 µm technology, including deposition of conformal barrier/seed layers by ionized PVD or CVD, bottom-up filling of vias and trenches using additive-enhanced Cu electroplating, and deposition and patterning of CVD and spin-on dielectrics having dielectric constant in the range $2 < k < 3$. On the other hand, integrating these unit processes together without losing the intrinsic material benefits of Cu and low-k dielectrics is a major challenge and requires a balance between performance, reliability and cost. The present talk illustrates how the distinctive physical and chemical properties of Cu and low-k dielectrics are influencing integration schemes as well as presenting new opportunities for process equipment and metrology suppliers. Examples will include issues of wafer-scale and micro-scale Cu contamination; the impact of water vapor exposure and degassing on low-k dielectric performance and film adhesion; and the development of reactive pre-cleaning and annealing methods to deal with the non-passivating nature of the Cu surface.

[1] **Featured Speaker - Science and Technology in the 21st Century**

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