Incorporating Principles of Industrial Ecology
Room 304 - Session IE-TuA

Green Manufacturing

Moderator: P.M. Beauchamp, Jet Propulsion Laboratory

2:00pm **IE-TuA1 Challenges in Bringing Green Manufacturing Technologies to the Clean Room Floor**, ***S. Raoux,*** Applied Materials **INVITED**

The semiconductor industry is undertaking major research and development efforts to reduce the environmental impact of its manufacturing processes. In particular, technologies have been introduced to eliminate atmospheric emissions of global warming compounds, reduce solid waste and conserve energy and water resources. At each technology node, semiconductor fabrication processes are amenable to change, and implementation of sustainable manufacturing practices should be favored. However, the stringent requirements of the semiconductor fabrication process render the introduction of novel manufacturing techniques a challenge. In this talk, we present innovative concepts that have been developed and integrated within semiconductor fabrication tools. Emphasis is placed on point-of-use (POU) solutions and environmental engineering using plasma technologies. We review the requirements that must be met by green technologies to be integrated to a complex manufacturing environment. We also present arguments to demonstrate that environmentally benign manufacturing methods can be developed and implemented in an economically viable way.

2:40pm **IE-TuA3 Eliminating Perfluorocompound Gas Emissions from CVD Chamber Cleans**, ***P.J. Maroulis,*** *A.D. Johnson, W.R. Entley,* Air Products and Chemicals, Inc. **INVITED**

Perfluorocompond (PFC) gases such as CF4, C2F6, and NF3 are used extensively in semiconductor manufacturing processes. The largest volume use for these gases is for chamber cleaning following chemical vapor deposition (CVD). PFCs have long atmospheric lifetimes and absorb strongly in the infrared region of the electromagnetic spectrum where the earth's atmosphere would otherwise be transparent. Because of their infrared absorbances and persistence, PFCs are suspected of contributing to global warming. Through the World Semiconductor Council (WSC) the global semiconductor industry has voluntarily committed to reduce its cumulative emissions of perfluorocompounds. For the U.S., Europe, and Japan, PFC emissions will be reduced to 90% of 1995 levels by 2010 with some companies announcing even more aggressive reduction targets. Based on industry growth projections, substantial reductions for individual processes will be necessary to achieve these targeted levels. Both process optimization of traditional C2F6 based in situ cleans and substitution of NF3 for C2F6 in situ cleans are effective strategies for reducing the environmental impact of installed CVD tools. For new CVD tools, the manufacturers of semiconductor process equipment have developed and introduced a new remote NF3 cleaning technology that essentially eliminates PFC emissions. The combination of these three strategies, optimization of traditional C2F6 based in situ cleans, the substitution of NF3 for C2F6 in in situ cleans, and the implementation of the remote clean technology, has effectively solved the semiconductor industry's PFC issue. This presentation will contain data demonstrating the effectiveness of these strategies. In essentially all cases, perfluorocompounds emissions have been reduced by 50% to >99%.

3:20pm **IE-TuA5 Meeting IBM's PFC Emission Goals: Using the IBM In Situ Dilute NF@sub 3@/He Plasma Clean in Production on the Applied Materials 200 mm P5000 Lamp-Heated CVD Toolset**, ***C.M. Hines,*** IBM Microelectronics*; W.R. Entley, R.V. Pearce, A.D. Johnson,* Air Products and Chemicals, Inc.

The major use of perfluorocompounds (PFCs) in semiconductor manufacturing is for residue removal following thin film deposition in chemical vapor deposition (CVD) chambers. One promising strategy to reduce PFC emissions in CVD chambers is the use of alternative clean gases that have lower global warming potentials and inherently higher utilization efficiencies (the percentage of the PFC that is consumed during the clean process) than the traditionally used carbon based PFCs, CF@sub 4@ and C@sub 2@F@sub 6@. Using this strategy, IBM developed a one-step in situ dilute nitrogen trifluoride/helium (NF@sub 3@/He) clean to replace the process of record (POR) C@sub 2@F@sub 6@-based cleans used in their Applied Materials (AMAT) 200mm Precision 5000 lamp-heated (DxL) CVD chambers. Successful implementation of the dilute NF@sub 3@/He clean into production is considered key to IBM meeting its PFC reduction goals. Using quadrupole mass spectrometry (QMS) and Fourier transform infrared (FTIR) spectroscopy the process emissions of IBM's POR C@sub 2@F@sub 6@-based cleans and the new one-step dilute NF@sub 3@/He clean following deposition of both phosphosilicate glass (PSG) and tetraethylorthosilicate (TEOS) oxide were quantified. For TEOS oxide deposition the one-step dilute NF@sub 3@/He clean reduced the MMTCE value of the clean by 99 % with respect to the POR C@sub 2@F@sub 6@ clean. For PSG deposition, the one-step dilute NF@sub 3@/He clean reduced the MMTCE value of the POR clean by 96 %. In addition, the one-step dilute NF@sub 3@/He clean significantly reduced the total combined volumetric emissions of F@sub 2@ and HF compared to the POR C@sub 2@F@sub 6@ cleans. This presentation will include an overview of the implementation of the NF@sub 3@/He clean, current production data including tool performance (particles, mean time between wetstrips, etc.), and clean time/emissions comparisons between the POR C@sub 2@F@sub 6@ cleans and the one-step NF@sub 3@/He clean.

3:40pm **IE-TuA6 Treatment of Wastes from Chemical Mechanical Polishing Operations**, ***S. Raghavan,*** *Y. Sun, J. Baygents,* University of Arizona **INVITED**

Chemical mechanical planarization (CMP) of dielectrics and metals has emerged as one of the most important techniques used in the fabrication of integrated circuits. In this technique, dielectric and metal films are globally and locally planarized using particulate slurries made from submicron-sized alumina and silica particles. A multi platen CMP tool can typically process 40 wafers per hour at a slurry consumption of approximately 100 ml/min/wafer. The aforementioned tool, if integrated with a cleaner, will require two to three gallons per minute of DI water. The mixing of CMP waste with the post-CMP cleaning waste typically results in a waste stream that is a very dilute dispersion of solids containing approximately 500 to 5000 ppm solids. In the case of metal CMP, the waste is likely to contain metal ions, unreacted oxidant such as hydrogen peroxide, residual corrosion inhibitors and other additives that are present in the slurry. Wastes from copper CMP may contain anywhere between 10 and 40 ppm of dissolved copper, in the uncomplexed and complexed form. By the year 2002, chemical mechanical planarization processes are expected to account for thirty percent of water consumed in a fabrication facility. Because of this statistics, increasing pressure is put upon fabrication facilities to treat the CMP wastes and recycle the water. Additionally, environmental regulations at the local and national level demand that solids and copper ions be removed before disposal of the water to publicly owned treatment facilities. In this presentation, an overview of the CMP waste problem will be provided and various techniques available for the treatment of CMP wastes will be critically reviewed.

4:20pm **IE-TuA8 Advanced Chemicals for Semiconductor Processing**, ***E.R. Sparks,*** *W. Wojtczak, S.A. Fine,* ATMI **INVITED**

Three of the challenges to semiconductor processing are shrinking dimensions, copper metallization, and low-k dielectric materials. These challenges have been successfully addressed with a new group of water-based chemicals that fortuitously have very favorable properties. - As lithographic dimensions shrink, etching and other processing parameters become more stringent. The residues created from photoresist during these proceses often incorporate fluorocarbon residues, and silicon and metal oxides that are impossible to remove with traditional chemicals. - New processes using copper damascene metallization have additional constraints, as many traditional chemicals are not benign to copper. - Higher speed devices are attainable with low-k dielectric materials, but these materials have special chemical requirements. Advances have been made to meet all three of these requirements by formulating chemical mixtures that are more benign, both environmentally and regarding health issues, than previously possible. These blends are water-based, water-rinsable, and free of regulated solvents, i.e., "green". The resulting technology has a very favorable cost of ownership due to lower costs related to abatement and disposal, compared to more traditional solvent blends.

5:00pm **IE-TuA10 High Throughput Process for Photoresist Stripping and Residual Polymer Removal in a Via Post-Etch Process**, ***M. Boumerzoug,*** *Q. Geng, H. Xu,* Ulvac Technologies Inc.*; S. Gu,* LSI Logic Corporation*; S. Goh,* Silterra (M) Sdn. Bhd.*; T. Meyer, J. Seaton,* LSI Logic Corporation

In fabricating advanced IC, a multi-level interconnect scheme is commonly used and plasma etch is applied to form metal lines and via holes. During the plasma etch, a sidewall polymer is formed to control the etch profile. After the etch, the sidewall polymer needs to be removed completely to

insure a good via contact resistance. Typically, a very aggressive amine based chemical solvent is needed to clean up the sidewall polymer. As the design rule shrinks and aggressive zero overplot of the metal line and via plug is used to minimize the die size, some degree of misalignment between via plug and metal lines is inevitable. Wet chemical based post etch cleaning starts to show problems for the misaligned via and metal because they may attack exposed Ti, W and Al. An advanced dry clean process has been developed for removing post etch polymer. In addition, the dry clean process offers a lower cost of ownership (COO) than the wet clean process and is much safer and environmentally friendly. This technology utilizes the combination of microwave downstream and non-damage ion assisted processes to strip chemically altered and damaged photoresist and clean residue according to the chemical composition of each layer. The ion-assisted process is also found useful in stripping the photoresist at high rate. After this dry process, no wet strippers are needed; thus, the high cost and environment and safety concern associated with chemicals can be eliminated. In some cases, this dry clean process becomes an enabling technology for avoiding Ti and W-plug attack occurring in the wet cleaning processes. Split lots of wafers, which have two layer metal, were processed by the all-dry processes and tested electrically. The via chain resistance, metal bridging yield, metal continuity and electrical CD are all equal or better than the control wafers which were processed by wet chemicals.

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