Dielectrics
Room 312 - Session DI+EL+MS-WeA

Alternate Gate Dielectrics
Moderator: R. Ramesh, University of Maryland

2:00pm **DI+EL+MS-WeA1 Materials Considerations for High-K Gate Dielectrics for Scaled CMOS**, ***G.D. Wilk,*** Lucent Technologies*; R.M. Wallace,* University of North Texas **INVITED**

Many materials systems are currently under consideration as potential replacements for SiO@sub 2@ as the gate dielectric material for sub-0.13 µm CMOS technology. A systematic consideration of the required properties of gate dielectrics, however, indicates that the key issues for selecting a high-k dielectric are permittivity and band offset, thermodynamic stability, crystal structure, and compatibility with the current or expected materials to be used in processing for CMOS devices. Many dielectrics satisfy some of these criteria, but very few materials actually satisfy all. A review of current work and literature in the area of high-k gate dielectrics is given, and some conclusions are drawn for various systems based on reported results and fundamental materials considerations.

2:40pm **DI+EL+MS-WeA3 New High k Thin Films with Improved Physical and Electrical Properties**, ***Y. Kuo,*** *J. Donnelly, J. Tewg,* Texas A&M University

When the minimum device dimension is shrunk to 100 nm, the conventional silicon oxide cannot fulfill many requirements of the device.@footnote 1@ For example, the thin gate dielectric layer (e.g., < 1.2 nm) will have a high leakage current and cannot stop the boron penetration. The dielectric constant of silicon oxide (e.g., 4.0) is too low for the small-size storage capacitor cell. Therefore, it is urgent to develop a new kind of thin film dielectric that has a high dielectric constant (high k) and can satisfy all stringent material, process, and device requirements. Metal oxides are ideal candidates for the gate dielectric application because their compositions are simple and their k values are high enough to last for next several generations of devices. In addition to the high interface states, a metal oxide has the problem of high leakage current, which is caused by the polycrystalline phase formation during the high temperature process.@footnote 2,3@ In this paper, we present new results on high k metal oxides that have high amorphous-to-polycrystalline transition temperatures. By adding a third element into tantalum oxide, e.g., Ti, Cu, and Mo, the film can exist in the amorphous phase in an extended temperature range. The leakage current at a high temperature is lowered. Material and electrical characteristics of the new film, e.g., by x-ray diffraction, ellipsometer, current-voltage and capacity-voltage curves, will be shown and discussed. The influence of the deposition process, i.e., reactive co-sputtering, to film properties will also be presented. These new high k dielectrics have the potential of being used as gate dielectrics in future MOS devices. @FootnoteText@ @footnote 1@ International Technology Roadmap for Semiconductors, 1999 ed., SIA, etc. @footnote 2@ S. R. Jeon, S. W. Han, and J. W. Park, J. Appl. Phys. 77, 5978, 1995. @footnote 3@ R. B. van Dover, R. M. Fleming, L. F. Schneemeyer, G. B. Alers, and D. J. Werder, IEDM, 823, 1998.

3:00pm **DI+EL+MS-WeA4 Chemical and Microstructural Separation of Homogeneous Plasma Deposited (ZrO@sub2@)@subx@(SiO@sub2@)@sub(1-x)@ films (x @<=@ 0.5) into SiO@sub2@ and ZrO@sub2@ Phases after Rapid Thermal Annealing in Ar at 900°C**, ***B. Rayner,*** *R. Therrien, G. Lucovsky,* North Carolina State University

Zr-silicate alloys along the pseudo-binary join from SiO@sub2@ to ZrO@sub2@ have attracted interest as high-k dielectrics for Si CMOS devices with equivalent oxide thickness extending to 0.6 nm. In this study alloy films were deposited on HF-last and pre-oxidized and/or nitridized Si(100) by remote plasma enhanced chemical vapor deposition using Zr(IV)-t-butoxide. Film and interface chemical composition, local atomic bonding, and film morphology were studied by Auger electron spectroscopy, Fourier transform infrared absorption, X-ray diffraction, and Rutherford back-scattering. These studies identified two alloy regimes: (i) SiO@sub2@-rich compositions to the compound silicate, ZrSiO@sub4@ (x = 0.5), where properties may be suitable for high-k applications, e.g., films are amorphous on deposition and remain so up to at least 800°C, and (ii) ZrO@sub2@-rich compositions in which films are either partially or totally crystalline on deposition, or after relatively low temperature (< 600°C) anneals. Alloys in the SiO@sub2@-rich regime are chemically-ordered as-deposited at ~350°C with predominantly Si-O-Si and Zr-O-Si bonds, but after annealing in Ar at 900°C for 60 s, separate chemically and microstructurally into SiO@sub2@ and ZrO@sub2@ phases. The ZrO@sub2@ phase is crystalline at the ZrSiO@sub4@ composition. This separation may limit integration of these films into devices which incorporate polycrystlline-Si gate electrodes requiring dopant activation at temperatures > 900°C. Capacitance-voltage and current-voltage characteristics will be presented for as-deposited and annealed films to illustrate the effects of chemical phase separation and crystallization in defining maximum post deposition processing temperatures.

3:20pm **DI+EL+MS-WeA5 A Study of ZrO@sub2@ and Zr-silicate Thin Film for Gate Oxide Applications**, ***S.-W. Nam,*** Yonsei University & Samsung Electronics Co., Korea*; J.-H. Yoo, H.-Y. Kim, D.-H. Ko,* Yonsei University, Korea*; S.-H. Oh, C.-G. Park,* Pohang University of Science and Technology (POSTECH), Korea*; H.-J. Lee,* Stanford University

We investigated the microstructures and electrical properties of ZrO@sub2@ and Zr-silicate thin films deposited by reactive DC magnetron sputtering on Si substrate for gate dielectric application. The films deposited on Si with various deposition conditions and annealing treatments were analyzed by spectroscopic elipsometry, XRD, AFM and XPS. The refractive index of the ZrO@sub2@ thin films increased upon annealing. The ZrO@sub2@ film deposited at low temperature and low power showed amorphous structure, which the films deposited at high temperature and high power showed crystalline structures. The growth of the interfacial oxide between ZrO@sub2@(or Zr-silicate) and Si substrate was observed by cross sectional HR-TEM. C-V and I-V measurements of the MOSCAP structures showed that the accumulation capacitance value and the leakage current level decreased upon annealing in O@sub2@ gas ambient, which is explained by the formation of the interfacial SiO@sub2@ layer.

3:40pm **DI+EL+MS-WeA6 Ultra-thin Zirconium Oxide Films Deposited by Rapid Thermal CVD for MOSFET Applications**, ***Y. Lin,*** *J.P. Chang,* University of California, Los Angeles

The increasingly tighter process specifications for the next generation microelectronic devices dictate the usage of metal oxides such as zirconium oxide as insulators for better process control and a more reliable dielectric/silicon interface.@footnote 1@ Zirconium t-butoxide is used with O@sub 2@ in this work to deposit zirconium oxide in a RTCVD system. The deposition temperature can be rapidly ramped to and controlled at 400-600°C, and the physical properties of the ZrO@sub 2@ films are characterized by XPS, XRD, AFM, TEM, and spectroscopic ellipsometry to determine the film compositions, chemical states, film microstructures, morphology, thickness, and index of refraction. Amorphous and nearly stoichiometric ZrO@sub 2@ has been deposited with less than 0.2nm variation in thickness across a 4" wafer. The dielectric constant is 3-4 times greater than that of SiO@sub 2@. Leakage current of a ZrO@sub 2@ film with an effective oxide thickness of 10 Å is three orders of magnitude lower than that of a 10Å thermal SiO@sub 2@ film. Post-deposition annealing at 500-700°C is shown to be effective in removing the majority of the incorporated carbon and further reduce the leakage current. However, there exists an optimal carbon doping level where carbon effectively passivates the electrically active defects and reduces the leakage current. We propose a simple kinetic model to describe the heterogeneous reactions responsible for the film deposition. NMOS transistors are fabricated and tested to determine the dielectric constant, leakage current, I-V and C-V characteristics of the zirconium oxide films. Moreover, stress induced leakage current and time dependent dielectric breakdown will also be detailed to assess the material reliability for its applications in microelectronics. @FootnoteText@ @footnote 1@G. D. Wilk, and R. M. Wallace, "Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon," Appl. Phys. Lett., 74(19), 2854(1999).

4:00pm **DI+EL+MS-WeA7 High-quality Ultrathin Fluorinated Silicon Nitride Gate Dielectric Films Prepared by Plasma Enhanced Chemical Vapor Deposition Employing NH@sub 3@ and SiF@sub 4@**, ***H. Ohta,*** *M. Hori, T. Goto,* Nagoya University, Japan

The silicon nitride (SiN@sub x@) film attracts much attention as scaled gate dielectric films in next generation@super ,@s ULSI. However, the conventional SiN@sub x@ film has a poor interface with silicon and is leaky due to a high trap density in the film. Recently, we have developed ultrathin fluorinated SiN@sub x@ films formed by ECR-PECVD employing NH@sub 3@/SiF@sub 4@. It is known that the average bond energy (5.73eV) of Si-F is higher than that of Si-H (3.18eV). Therefore, it is

expected that the Si-F bond in the film should have improved the quality of gate dielectric film. In this study, we have investigated properties of ultrathin SiN@sub x@ films (4nm) formed at 350°C. These films (fluorinated SiN@sub x@ films) contain fewer hydrogen atoms than the conventional SiN@sub x@ films formed by ECR-PECVD employing NH@sub 3@/SiH@sub 4@. As-deposited fluorinated SiN@sub x@ films indicated the excellent hysteresis loop (20mV) in the C-V curve, and reduced the leakage current by several orders of magnitude than the thermal SiO@sub 2@ in the identical equivalent oxide thickness (EOT). These film properties and the surface reactions for the SiN@sub x@ film formation with good quality are discussed on the basis of results of the in-situ XPS, in-situ FT-IR RAS, FT-IR, and thermal desorption mass spectroscopy (TDS). As a result, the control of fluorine concentration in the SiN@sub x@ films was found to be a key factor for forming the fluorinated SiN@sub x@ films with high quality at low temperatures. The fluorinated SiN@sub x@ is very effective for ultrathin gate dielectric films in next generation@super ,@s ULSI.

4:20pm **DI+EL+MS-WeA8 Elimination of Carbon Impurities in the Metalorganic Chemical Vapor Deposition (MOCVD) of Titanium Dioxide on Silicon**, ***M. Yoon***, *A.C. Tuan, V.K. Medvedev,* University of Washington*; J.W. Rogers, Jr.,* Pacific Northwest National Laboratory

A novel process has been developed for the deposition of titanium dioxide thin films on p-type Si(100) with high quality interfacial characteristics and the absence of carbon. Elimination of carbon contaminants in the titanium dioxide film and at the interface between the oxide and silicon is important because the presence of impurities can severely degrade the electrical properties of the device. This novel process consists of three stages of deposition in an ultra-high vacuum chamber. Initially, a continuous titanium layer is deposited on silicon using a titanium sublimator. This titanium layer is then oxidized using a gas phase oxygen source to form a TiO@sub x@ buffer layer. Subsequently, a titanium dioxide thin film is deposited by MOCVD using titanium tetrakis-isopropoxide (TTIP) at low temperature (below 650K). Auger electron spectroscopy (AES) analysis at each stage of growth shows no evidence of carbon contamination either within the titanium dioxide layer or at the TiO@sub 2@/Si interface. Additional AES measurements suggest that the titanium layer grows on silicon according to the Stranski-Krastanov mode, which permits uniform growth. A carbon-free titanium dioxide thin film was successfully deposited on silicon using this novel process.

4:40pm **DI+EL+MS-WeA9 Microscopic Understanding of the Interface for the Heteroepitaxy of Crystalline Oxides on Silicon**, ***S. Gan***, *D.E. McCready, D.J. Gaspar, Y. Liang,* Pacific Northwest National Laboratory

With SiO@sub 2@ approaching its fundamental limit as the gate dielectric in the existing Si-based CMOS technology, searching for alternative gate oxides with high dielectric constants is crucial for the next generation of devices. Recent work showed crystalline oxides such as SrTiO@sub 3@ (STO) is promising as an alternative to SiO@sub 2@ in MOS capacitors. One of the most important issues is how to integrate it into the existing Si-based technology, the first step of which is the growth of epitaxial oxides on Si substrates. Here we present our recent results on the study of the oxide-silicon interface, which plays a critical role in growing high-quality STO films. Employing scanning tunneling microscopy (STM), x-ray photoelectron spectroscopy (XPS), low-energy electron diffraction (LEED), we characterized the interfacial structure of each template layer (Sr and SrO) grown on Si in situ. The results revealed that the strontium covered silicon surfaces exhibit a series of reconstructions, including a (2x1) structure that provides the most stable interface for the growth of oxides. In addition, we used time-of-flight second ion mass spectrometry (TOF-SIMS) and x-ray diffraction (XRD) to investigate the interfacial chemistry and film structure. By combining these techniques, we correlated the interface structures with film properties, which allowed us to identify suitable interfacial templates for optimized growth. @FootnoteText@ Pacific Northwest Laboratory is a multiprogram national laboratory operated by Battelle Memorial Institute for the U.S. Department of Energy under Contract DE-AC06-76RLO 1830.

5:00pm **DI+EL+MS-WeA10 Formation of Ultrathin Yttrium Silicate by Thermal Oxidation of Yttrium on Silicon**, ***M.J. Kelly***, *J.J. Chambers, D. Niu, G.N. Parsons,* North Carolina State University

We show that direct thermal oxidation can be used to form thin (<50@Ao@) high-k metal silicate layers directly on crystalline silicon. Bulk thermodynamics indicates that several high-k metal oxides (including oxides of Hf, Zr, Al, Y, La, etc.) will be stable with respect to silicon dioxide formation when the oxide is in contact with silicon. However, most low temperature approaches (PVD, CVD, or MBE) for metal oxide deposition on silicon involve elementary reaction steps that include metal-silicon bond formation before oxidation, resulting in uncontrolled interface layers between the metal oxide and silicon. We can utilize this mechanism to form yttrium silicate films on silicon by first sputtering thin (<10@Ao@) metal films on silicon, vacuum annealing at 300-600Â°C to form a silicide, then oxidizing at 600-900Â°C. XPS, medium energy ion scattering, and IR indicate film composition is close to yttrium orthosilicate (Y2O3Â·SiO2) with some excess Y2O3, depending on anneal conditions. Oxidation kinetics (determined from thicknesses measured by TEM) indicate an initial fast oxidation rate (due to oxidation of metal silicide), followed by a slower process (due to oxidation of underlying silicon). CV analysis of 42@Ao@ films show oxide equivalent thickness ~12@Ao@, consistent with dielectric constant ~14. Leakage is <1A/cm2 at 1V in accumulation. IR and XPS indicate that films do not phase separate when annealed up to 900Â°C for 20 minutes. Thin (<10@Ao@) silicon oxide and nitride interface layers have been formed in-situ by remote plasma exposure before metal deposition and their effect on interface reaction kinetics have been analyzed by XPS and MEIS. Interfacial oxide is observed to have a negligible effect on interface reactions, but results suggest interface nitrogen tends to block silicide formation before oxidation. These results give important insight into controlling interface structure for implementing high-k materials into silicon devices.

Author Index

Bold page numbers indicate presenter