Plasma Science and Technology Division
Room 612 - Session PS1-ThA

High Fidelity Pattern Transfer

Moderator: K.H.A. Bogart, Lucent Technologies

2:00pm **PS1-ThA1 High Fidelity Pattern Transfer**, ***K. Kasama***, *K. Yoshida, N. Ikezawa, T. Uchiyama,* NEC Corporation, Japan **INVITED**

The design rule of ULSI devices is being shrunk rapidly, now approaching to 150~130nm region. Moreover, the requirement of pattern formation fidelity, such as CD accuracy, overlay accuracy, pattern profile and so on, also becomes very strictly. For example, in the case of gate electrode formation, CD accuracy of less than ±10% is required after dry-etching, i.e., within ±15nm for 150nm devices. However, large CD fluctuation is usually generated in lithography process, and its amount reaches to CD budget. So, very tight CD control is necessary in dry-etching. In this presentation, current status of optical lithography will be introduced. Especially, we will discuss CD fluctuations induced by exposure tool stability, optical proximity effect and device topographic effect. In order to improve pattern fidelity, high NA scan exposure system, optical proximity effect correction mask and anti-reflective layer have been adopted as new lithographic techniques. Next, the resist pattern transfer by plasma process will be discussed, by mainly focusing on gate electrode formation. To suppress pattern density dependence (micro-loading effect) as well as gate oxide thickness reduction, we investigated two step etching process by using high density plasma, TCP. In a main etch step, vertical etched profile is formed under the plasma condition of high etch rate and low micro-loading, and then high selectivity etching to gate oxide is applied as a soft landing step. We have achieved good CD control of less than 10% in the 120~150nm gate formation. Moreover, we will mention about resist pattern shrinkage technique during BARC(bottom anti-reflective coating) plasma etching.

2:40pm **PS1-ThA3 High Volume Self Aligned Contact Etch for SRAM**, ***U. Raghuram***, *J.E. Nulty,* Cypress Semiconductor

Self-Aligned Contact (SAC) technology is used by Cypress Semiconductor in SRAM cells to form contacts which connect local interconnect and diffusion regions. SAC contacts allow designers to reduce the cell size by reducing the poly pitch. SAC technology is made feasible by the selective etch of the interconnect dielectric such as borophosphosilicate glass to the nitride etch-stop. This paper describes the key parameters for a manufacturable SAC etch, namely, gas chemistry, backside helium cooling, and total gas flow/ pressure. Polymer fill in the contacts provides the required selectivity to the etch-stop layer in SAC etch. The polymer profile is controlled by the sticking coefficient, which is controlled by the wafer temperature. Two common mechamisms for SAC etch are incomplete etch, 'grass', caused by excessive polymer deposition, and loss of selectivity, 'punch through', caused by insufficient polymer protection. Freon-23/ Freon 134a based chemistry provides self limiting nitride etch-stop performance. Uniform and constant wafer temperature is critical for process window in an etch controlled by polymer deposition. Using electrostatic chuck technology resulted in a wider process window with respect to backside helium control. The process runs at relatively higher pressures (50-100 mT) and total flows (70-150 sccm). Addition of argon allows the process to run at a moderate pressure and flow. It also improves the process uniformity. Backside helium setting of 8-12 Torr provides good wafer temperature control. The process was first developed for 0.5 micron design rules. The Cypress SAC process has been transferred to two different medium density plasma etcher platforms. This process has also been extended with minor modifications to etch SAC contacts for at least four SRAM technologies ranging from 0.5 to 0.21 micron design rules.

3:00pm **PS1-ThA4 High Density Plasma Oxide Etching of SAC (Self-Aligned Contact) and 0.25 micron HARC (High Aspect Ratio Contact) Structures: Process and Repeatability Results**, ***L. Marquez***, *B. Bosch, O. Turmel, S. Darcy, J.M. Cook,* Lam Research

A major challenge of SiO@sub2@ etching for sub-0.25 micron design rules is the stability of the process both long and short term. The very small, often deep, features together with the requirement for high selectivity guarantee that a very high degree of control of both the hardware and the process is essential. Stable SAC and HARC (> 10:1 aspect ratio) processes have been developed in an inductively coupled, high-density plasma dielectric etch tool. The repeatability of the processes was found to be dependent on the stability of the reactor's surface temperature, the material properties of the reactor's walls and the overall cleanliness of the chamber. The trends (etch rate, selectivity, uniformity, etc.) of the processes have been investigated in terms of power, pressure, flow, chemistry and wall temperatures. It is necessary to understand these trends in order to optimize the various process parameters such as selectivity and uniformity. The impact of surface temperature and material properties on the process results will also be discussed. Several marathons with both the SAC and HARC processes have demonstrated the manufacturability of both the processes and the high density plasma dielectric etch tool. The results of these marathons will be presented.

3:20pm **PS1-ThA5 The Angular Dependence of SiO@sub 2@, Si@sub 3@N@sub 4@, and Poly-Silicon Etching Rates in Inductively Coupled Fluorocarbon Plasmas**, ***C. Hedlund***, Uppsala University, Sweden, Usa; *F. Engelmark, H.-O. Blom,* Uppsala University, Sweden; *M. Schaepkens, G.S. Oehrlein,* State University of New York at Albany

Modern plasma etching processes, like self aligned contact (SAC) etching and the damascene and dual damascene dielectric etching, put new demands on the patterning processes. In the fabrication of self-aligned contacts, for instance, the silicon dioxide etching process has to stop on the curved silicon nitride spacer surface. At this curved surface a reduced SiO@sub 2@ to Si@sub 3@N@sub 4@ selectivity commonly is observed. In order to investigate the behavior of the angular dependence of the etch rate and the surface chemistry we prepared structures with a precise angle between the structure surface and the normal of the wafer surface by highly selective wet chemical etching of crystalline silicon. These micro machined structures consisting of either V-grooves or free standing rectangular mesas are ten times smaller than the plasma sheath, resulting in a ion flux normal to the wafer surface. The angular dependence of SiO@sub 2@, Si@sub 3@N@sub 4@, and Poly-Silicon etch rates have been studied in inductively coupled fluorocarbon plasmas. Our data indicate that the reason for the lower selectivity at inclined Si@sub 3@N@sub 4@ and poly-silicon surfaces is the angular dependence of the fluorocarbon film deposition and etching rates. At selective SiO@sub 2@ to Si@sub 3@N@sub 4@ conditions a relatively thin fluorocarbon film is formed on curved surfaces and corners as compared to planar surfaces. The surface chemistry and film thicknesses have been investigated with spectroscopic ellipsometry and. X-ray electron spetroscopy (XPS). The results will be presented along with SEM micrographs of etched structures.

3:40pm **PS1-ThA6 Process Optimization of Plasma Polymerized Resists for Advanced Lithography Applications**, ***O. Joubert***, CNET/CNRS, France; *C. Monget,* CNET France Telecom, France; *L. Vallier,* CNET France Telecom; *T.W. Weidman,* Applied Materials

CVD photoresist processes based on the plasma polymerisation of organosilane precursors such as methylsilane or dimethylsilane are currently investigated as a technique to extend 248 and 193 nm lithography. Upon exposure to UV light in air, these materials are oxidized generating areas which become more etch resistant to halogen based plasma than unexposed areas, providing a versatile approch to negative tone processes. Films have been deposited in a DXZ chamber from Applied Materials dedicated to dielectric deposition. Exposures have been performed using 248 nm (ASML /300) and 193 nm steppers (ASML /900 and Exitech microstepper). Film development was performed in high density plasma sources using mixtures of Cl@sub 2@, HBr and O@sub 2@. In all cases, developed CVD resist images are transferred through 500 nm of hard baked organic resist using SO@sub 2@/O@sub 2@ gas mixtures. This work reports the lithographic performance at 248 and 193 nm obtained with these dry resists (resolution down to 0.18 µm L/S at 248 nm and 0.13 µm L/S at 193 nm is achieved). Photosensitivity of the films, which can be tuned using the deposition parameters is strongly correlated to the film structure and density. In particular, FTIR analyses show that the photosensitivity increases with the methyl groups content, which favors an increase of the oxygen permeability in the film. The plasma development step is the most critical step of the process since the most serious issues in the dry lithographic process to achieve a good CD control across the wafer. Etch process parameters such as selectivity and uniformity are the more relevant parameters to control the final line width and profile before transfer into the underlaying organic layer. The performance and limitations of the all dry CVD process will be presented. @FootnoteText@ @footnote 1@ This work has been carried out within the GRESSI Consortium between CEA-LETI and France Telecom-CNET

4:00pm **PS1-ThA7 DUV Resist Degradation and Surface Roughening under Plasma Exposure**, ***W.H. Yan***, Microelectronic Division, IBM Corp.; *W. Moreau, R. Wise, Y. Cui,* IBM Corp.

This study investigate the plasma etch characteristic of several different types of DUV photoresist. It has been established that these photoresists suffer from degradation under exposure to common etch processes. We have demonstrated that resist degradation and surface roughening depend on resist polymer composition and etching process conditions. Results from this study clearly indicated: (1) Acrylate component in the polymer breakdown via chain scission during etching. That polymer breakdown causes resist surface pitting. (2) Ion bombardments, etch gas radicals, atoms and polymer deposition from etching reaction in the etching chamber further roughen the resist surface. (3) Heat and UV light in the etching chamber, on the other hand, crosslink resist polymer. The degree of crosslinking highly depends on resist polymer composition. We also investigated UV hardening, E-beam treatment as well as their impacts on resist etch resistance and surface roughening. Results showed that these treatments improve resist etch resistance, but not surface roughness. SEM and AFM were used to study resist surface and sidewall roughness. Gel Permeation Chromatography (GPC) was employed to analyze resist reaction under plasma exposure. The mechanism of resist roughness and its dependence on resist composition was discussed.

4:20pm **PS1-ThA8 Transfer Etching of Bilayer Resists in Oxygen-based Plasmas**, ***A.P. Mahorowala***, *K. Babich, Q. Lin, D.R. Medeiros, K. Petrillo, J. Simons, M. Angelopoulos,* IBM T.J. Watson Research Center; *G.W. Reynolds, J.W. Taylor,* University of Wisconsin, Madison

Thin film imaging offers the possibility of extending 248 nm lithography to sub-150 nm resolution. We have been working on a 248 nm bilayer resist scheme which utilizes a thin Si-containing resist on top of a thick, planarizing underlayer. The image is developed in the top layer and then transferred to the underlayer via an oxygen-based plasma etch. This paper will focus on two aspects of the critical transfer etch step - 1) etch resistance of the imaging resist and 2) control of profiles and resist roughening. The imaging resist thickness loss rate during the transfer etch is characterized by a rapid decrease in the first 10 seconds followed by a slow rate for the remaining etch. The relative importance of three phenomena occurring when Si-containing resists are exposed to oxygen-based plasmas - 1) oxidation of silicon, 2) deprotection of resist moieties, and 3) plasma etching of resist, will be discussed. FTIR studies on resist films indicate minimal film deprotection-related losses. XPS spectra show that the extent of surface oxidation increases initially and then becomes constant. Thus, this category of resists follows the model proposed by Watanabe and Ohnishi describing the etching of Si-containing resists as a combination of the oxidation of the silicon species and sputtering of the oxide-type layer formed. Post-transfer etch profiles using an oxygen plasma will be shown, and methods to reduce imaging layer resist faceting and thickness loss either by modifying the imaging layer silicon content or shifting to plasma chemistries causing sidewall passivation will be discussed. The effect of different etching chemistries and conditions on imaging layer roughening and striation formation on underlayer sidewalls will be explained with the aid of SEM micrographs and AFM images of etched feature sidewalls. The printing of 125 nm line/space patterns, and 150 nm trench features with 10:1 aspect ratios, in the underlayer will be demonstrated.

4:40pm **PS1-ThA9 Integration of Metal Masking and Etching for Deep Submicron Patterning**, ***C.T. Gabriel***, *R. Kim, D.C. Baker,* VLSI Technology

Although copper damascene interconnects offer many advantages over conventional subtractive etched Al alloys, the challenges and costs associated with converting to copper have combined to extend the useful life of Al alloy etching into the deep submicron regime. As a result, metal masking and etching are facing new challenges. DUV photolithography has replaced the conventional i-line technique for patterning fine metal pitches, but some DUV photoresists are less able to withstand the aggressive plasma environment than their i-line counterparts. Reflectivity increases at DUV wavelengths, so dielectric anti-reflective films are added on top of the metal stack. The mask-open process, where the dielectric film is plasma etched prior to etching the metal stack, alters the photoresist further and influences the subsequent metal etch. Aspect ratio dependent etch effects increase when etching narrow spaces resulting from tightened metal pitches, and gas additives may be required to protect the metal sidewalls. These effects are characterized and the challenges of deep submicron metal etch process development are discussed. The option of true hardmasked etching of the metal stack is also investigated.

5:00pm **PS1-ThA10 Manufacturable Aluminum RIE Processes for 150 nm and Beyond**, ***G. Stojakovic***, *X.J. Ning,* Siemens Microelectronics Inc. at IBM/Siemens/Toshiba DRAM Development Alliance; *E.W. Kiewra,* IBM Microelectronics at IBM/Siemens/Toshiba DRAM Development Alliance; *W. Kocon,* IBM Microelectronics

Three different aluminum etch processes - all proven to be manufacturable - have been developed for 150nm line/150space structures. The three schemes are: Organic ARC with photoresist as an etch mask, inorganic silicon oxynitride dielectric ARC (DARC) with photoresist as an etch mask, and a tungsten cap layer as a hard mask. The total metal stack height used in this work was 435 nm, with top and bottom Ti/TiN diffusion barriers. The designed aspect ratio of the wire for a 175 nm technology is 2.5, with a worst case of approximately 3.2. For 150 nm lines, this aspect ratio is substantially higher. For the two processes that use photo resist as the etch mask, the main task of the RIE process is to minimize the consumption of the resist during etch (i.e. maximize the etch selectivity of metal to resist). The metal etch tool used in this work was a commercially available plasma reactive ion etch system. The etch sequence starts with an ARC, DARC, or W hard mask open, followed by a Cl2/BCl3 based Al stack etch. An overetch is performed after a triggered end-point. Subsequent processing includes a down-stream H2O/oxygen plasma ash, followed by a water rinse. The key process parameters, such as gas flow rate, flow ratio of gases, and temperature that affect the metal profile and yield are discussed. It is shown that the RIE process can clear a sub-100 nm space for metal stacks having a height of over 400 nm. This indicates that aluminum RIE can be extended for even smaller structures. In the schemes that use photoresist as etch mask, the thickness of total metal stack is limited by the thickness of the photoresist. In the scheme that uses a PVD W hard mask, the total metal thickness is not a limiting factor for metal etch. The electrostatic chuck temperature plays a major role influencing metal profile and shorts yield.

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