Plasma Science and Technology Division
Room 609 - Session PS-MoM

Plasma Damage

Moderator: C.T. Gabriel, VLSI Technology

8:20am **PS-MoM1 Mechanisms and Dependencies of Gate Oxide Degradation Due to Electron Shading**, *G.S. Hwang,* ***K.P. Giapis,*** California Institute of Technology

We present results form self-consistent Monte Carlo simulations of charging during etching of dense antennas in uniform high-density plasmas. The simulations include sheath dynamics, ion and electron transport in the trench spaces, feature charging, electron tunneling through thin gate oxides and surface charge dissipation. Charging maps are used to illustrate how electron shading causes differential microstructure charging and subsequently electron tunneling from the substrate. The magnitude of this current is employed as a measure of the extent of damage to the gate oxide. The calculations explain experimental trends regarding electron and ion temperatures and suggest ways to reduce the damage by manipulating plasma parameters. A surprising sub-linear relationship between damage and antenna area is explained by a decrease in the net ion current density collected by the structure due to charging potential changes.

8:40am **PS-MoM2 Calculation and Measurement of Ion and Electron Shading Parameters and Comparison with Computer Simulation**, ***S.C. Siu,*** *R. Patrick, V. Vahedi,* Lam Research Corporation

Electron shading is recognized as a major mechanism for plasma process induced damage in commercial plasma etch chambers. As the semiconductor industry moves to smaller feature sizes and thinner gate oxides, shading induced damage becomes a greater concern. The shading effect is known to be more severe with higher aspect ratio features and high density plasmas. Recently, V. Vahedi, et al, derived an analytic model@footnote 1@ capturing the main parameters involved in electron shading. Two of these parameters, the ion and electron shading coefficients k@sub i@ and k@sub e@, have not been measured to date, but are crucial to the model. This study uses patterned and unpatterned SPORT@footnote 2@ wafers to measure and derive these shading parameters. In addition, a PIC simulation was used to predict values for these shading parameters. The simulation is able to account for charged resist structures that cause electron shading. Comparisons were made between the simulation and the experimental results. @FootnoteText@ @footnote 1@V. Vahedi, et al, "Topographic Dependence of Plasma Charging Induced Device Damage." 2nd International Symposium on Plasma Process-Induced Damage, May 13-14, 1997, Monterey California. @footnote 2@S. Ma and J.P. McVittie, Proceedings of the Symposium on Process Control, Diagnostics and Modeling in Semiconductor Manufacturing I, 95-4, pg 401, (1995).

9:00am **PS-MoM3 Direct Experimental Determination and Modeling of VUV induced Dielectric Conduction during Plasma Processing**, ***M.V. Joshi,*** *J.P. McVittie, K.C. Saraswat,* Stanford University

The processing plasma provides a source of high intensity VUV (vacuum ultra-violet) light which is incident on IC dielectrics. It also sets up considerable electric fields across these dielectrics due to either non-uniformity or electron shading induced plasma charging. This is expected to cause photo-current flow in these dielectrics. These photo-currents can damage the underlying devices through a variety of mechanisms and change the charging profiles due to electron shading during plasma processing. Thus determination of the relationships between incident photon density, photon wavelength, applied electric field and photo-current density is vital not only to understanding and controlling photo-current damage to devices during plasma processing but also to accurately model electron shading damage mechanisms. In this work we study the photo-currents that flow through the bulk of the dielectrics as opposed to those flowing on the surface. Bulk photo-conduction would explain the damage seen during dielectric depostion in a plasma chamber. We use a high density plasma as the source of VUV light and a independent very low density plasma separate by a thin filter/window to provide the electric fields and also to act as the current source for the VUV induced photo-currents. This allows independent variation of UV intensity and plasma charging electric fields. The probe consists of a bare polysilicon pad and a nearby similar pad covered with the dielectric. These pads are biased using a voltage source and current drawn through them is measured allowing the determination of the current density - electric field characteristic for the given dielectric independent of the biasing plasma. We measured photo-current density versus applied electric field, dielectric thicknesses, dielectric types, incident photon density, incident photon wavelength, transient effects and in dual dielectrics. We propose a model to explain these effects based on hole trapping and electric field dependent hole-electron recombination cross-section in the dielectric. This model allows prediction of VUV photo-conduction damage in realistic semiconductor processing structures.

9:20am **PS-MoM4 Investigating Ion Density and Electron Temperature Effects on Plasma Damage during Pulsed and Continuous Wave Metal Etching**, ***K.H.A. Bogart,*** Lucent Technologies*; J.I. Colonell,* Praelux*; M.V. Malyshev, V.M. Donnelly, J.T.C. Lee,* Lucent Technologies

Plasma induced damage across gate oxides has been shown to decrease with the use of pulsed rf source power, although the basis for the reduction in damage is not yet well understood. During the pulsed plasma off time, positive ion density (n@sub i@@super +@), electron temperature (T@sub e@), and electron density generally decrease, reducing the current flux to the wafer and the potential difference across the substrate sheath. Near the end of the off time, negative ions are thought to cross the diminished sheath and neutralize charge on the wafer surface, and also to be the predominant negative charge carrier in the plasma. Langmuir probe measurements of n@sub i@@super +@ and T@sub e@ were made on a LAM 9600-PTX commercial metal etcher using blanket SiO@sub 2@, Al, and TiN films as well as during etching SiO@sub 2@-masked TiN/Al/Ti/TiN while reactor pressure (5-30 mTorr), rf source power (0-400 W), rf substrate bias power (0-200 W), pulse duty cycle (0.5 - 1), and pulse period (0.100 - 1000 ms) were varied. Plasma induced damage was quantified on wafers with 0.25 µm linewidth technology NMOS and PMOS damage testers etched under the conditions listed above. For a 50% duty cycle, 100 µs pulse period, typical I-V curves (asymmetric about zero current) were collected with substrate bias applied. Without substrate bias, I-V curves characteristic of an ion-ion plasma (symmetric about zero current) were observed from 0-15 µs and from 80-100 µs. I-V curves acquired with only substrate bias power (continuous RIE mode) were similar in shape to I-V curves taken at the end of the pulse off time with bias applied. T@sub e@'s decrease and then increase near the end of the off time, indicating that the substrate rf bias power is sufficient to sustain a plasma during the off time, and that negative ions are not able to cross the sheath. Implications for plasma damage mechanisms will also be discussed.

9:40am **PS-MoM5 Sources of Plasma Induced Damage in Back-End VLSI Processing**, ***S.W. Downey,*** *D.W. Hwang, N. Layadi, P.W. Mason, A. Yen, V.M. Donnelly, M.V. Malyshev,* Lucent Technologies, Bell Laboratories*; J.I. Colonell,* Praelux, Inc. **INVITED**

The possibility of plasma induced damage of devices during wafer processing exists in both etch and deposition steps using gaseous discharges. A variety of mechanisms exist for deleterious current flow through a thin (25 @Ao@) transistor gate oxide. Plasma induced damage, as measured by gate leakage currents or shifts in threshold voltages, are given for several etch and deposition processes. Device damage during metal etch is shown to be related to aspect ratio and measured electron temperature. Evidence of current or voltage-limited conditions can be extracted by modeling. Cleaning and photoresist stripping plasmas can also cause damage if not properly designed or operated. Charging of photoresist while stripping is shown to be avoidable. Damage from plasma based metal deposition tools and via etchers is also problematic and difficult to decouple. Data will show that damage is sensitive to both hardware and process parameters, but improved hardware can yield a larger damage free process window.

10:20am **PS-MoM7 Charge Density Measurements in a Metal Etch Strip/Passivation Chamber**, ***R.L. Jarecki,*** *M.G. Blain,* Sandia National Laboratories*; J.S. Papanu,* Applied Materials, Inc.

Manufacturers have increasingly incorporated chambers capable of resist stripping as well as in situ passivation of etch residues on their metal etch tool platforms to mitigate corrosion resulting from exposure to atmospheric moisture. Such chambers typically feature a downstream microwave collisional plasma source with a pressure in the 0.5 to 10 Torr range using multiple-step chemistries based mainly on O@sub 2@ (for fast resist strip) and H@sub 2@O (for passivation by chlorine scavenging). Although "downstream" plasma strip processes are usually presumed to be almost charge-free due to the rapid decay of plasma density away from the source, it may be advantageous in practice to allow some level of charge to survive in order to increase the flux of etchant species to the wafer, and hence throughput. This study reports the direct measurement of ion

current densities observed via Langmuir probe in a commercial in situ strip and passivation chamber, for various gas feeds and hardware configurations, to help assess the level of charging damage to actual devices. Wafer level ion current densities below 2x10@super -8@ A/cm@super 2@ for typical strip processes and 8x10@super -10@ A/cm@super 2@ for passivation processes were observed with a standard gas distribution baffle configuration, while modified baffle configurations resulted in somewhat higher ion currents. Increases in power or total flow rate tended to increase current density. Correlation of probe measurements to surface photovoltage and antenna structure data will also be discussed@footnote 1@. @FootnoteText@ @footnote 1@Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract No. DE-AC04-94AL85000.

10:40am **PS-MoM8 Evaluation of Tests to Examine Charging Damage in Ion Implantation and Plasma Processes**, ***M.J. Goeckner,*** Varian Semiconductor Equipment Associates*; J. Erhardt,* AMD Inc.*; S.B. Felch,* Varian Semiconductor Equipment Associates*; K. Ahmed,* AMD Inc.

Charging damage is a critical issue in both plasma processing and ion implantation systems. Charging damage is typically studied with one of several distinct types of test structures. One of the more common is an "antenna" MOS capacitor test structure. After the device is subjected to the charging environment, plasma or implantation, the gate dielectric is then analyzed for damage. For this paper, we will examine three analysis techniques on various dielectrics. These analysis techniques are: measurement of temporal change in induced voltage at a low current density (dV/dt); measurement of induced leakage current at a low voltage (~2 V); and measurement of induced voltage at a high, stressing, current density (~1 A/cm@super 2@). Damage to the dielectric will be induced with a controlled damage current, of known length and strength. Dielectrics will range from 100 Å oxide to sub-40 Å nitrided oxides. The purpose of this work is to determine the most appropriate technique for characterizing plasma charging dielectric degradation in the ultra-thin dielectric regime, as well as to gain a baseline understanding of the damage under controlled conditions. It is envisioned that the results of this study can be used as a gauge for future experiments, as well as to provide an estimate of the damage currents in actual ion implantation and plasma processing environments.

11:00am **PS-MoM9 Study of Synchrotron Radiation-Induced Surface-Conductivity of SiO@sub 2@ for Plasma Charging Applications**, ***C. Cismaru,*** *J.L. Shohet,* University of Wisconsin, Madison*; J.P. McVittie,* Stanford University

During plasma processing, charging of dielectrics plays the leading role within the damage mechanisms. The charging potentials are determined by specific plasma and processed device parameters. Dielectric conductivity induced by vacuum ultraviolet (VUV) irradiation is one mechanism to affect dielectric charging not very well understood. In this work we investigate electrical surface conductivity in SiO@sub 2@ exposed to monochromatic synchrotron radiation for plasma charging applications. Special test structures were exposed to controlled fluxes of monochromatic synchrotron radiation in the range of 500 Å to 3000 Å (approx. 4 eV to 25 eV), the energy band of most plasma VUV radiation, at the Synchrotron Radiation Center, University of Wisconsin-Madison. During the exposure, radiation-induced currents in SiO@sub 2@ were monitored while controlling the electric field across the sample. Results show different characteristics of the photoinduced currents depending on the intensity of the electric field, thickness of the oxide, and radiation wavelength. Implications of these results on plasma charging of dielectrics will be discussed. This work was supported in part by the National Science Foundation under Grant No. EEC 8721545 and the Semiconductor Research Corporation under Contract No. 98-1J-106. The Synchrotron Radiation Center is a national facility, funded by the National Science Foundation under Award No. DMR-9531009.

11:20am **PS-MoM10 Effect of Surface Oxide Loss on Surface Potential Measurement (SPM) Accuracy for Plasma Charging Damage Characterization**, ***S. Ma,*** *K. Nauka, R. Kavari,* Hewlett-Packard Company

It is well recognized that the surface potential measurement (SPM) technique can be used as a process diagnostic tool for evaluating plasma-induced charging damage in MOS devices. To date, it is the simplest and cheapest non-invasive method using blank oxide wafers to monitor cumulative wafer charging after plasma exposure. Despite of its convenience, SPM's results do not always correlate well with MOS device charging damage data, especially in sputter clean, metal etch and oxide etch processes. There is limited understanding currently available to explain why the weak correlation sometimes exists. This paper examines the reason why surface potential measurement (SPM) results after plasma exposure do not always correlate to the results of plasma induced charging damage measurement on devices. One very important explanation has been found to be non-uniform surface oxide loss during plasma exposure on test wafers. From biased oxygen plasma exposure experiments in a M0RI source high density plasma etcher, the SPM results lost their correlation to antenna capacitor device damage when the substrate bias was sufficient to etch the surface oxide. As the amount of surface oxide loss increases, deposited surface charge distribution correlates better to surface oxide loss than to the damaged antenna capacitor data. Longer plasma exposure time with more oxide loss also shifts the SPM results to a higher averaged value. Compared to the device damage data, the critical surface oxide loss causing misleading SPM results is estimated to be around 70Å. Therefore, this characterization method is applicable to plasma induced charging damage for limited processes that do not cause severe surface oxide loss such as resist ashing, high oxide selectivity poly etch, etc.

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