Manufacturing Science and Technology Group
Room 4C - Session MS-WeP

Poster Session

MS-WeP1 Effects of Trapped Charges on Hg-Schottky Capacitance-Voltage Measurement of N-type Epitaxial Silicon Wafers, *Q. Wang, **D. Liu**, J.T. Virgo,* Mitsubishi Silicon America Corp.

The accurate carrier concentration profiling is very critical during silicon wafer process such as dopant profiling measurements of epitaxial layer or ion implanation etc. The mercury probe (Hg-Schottky capacitance-voltage (CV)) is a standard method in this application. This method is however, very sensitive to the silicon wafer surface condition and is a challenging issue in semiconductor industry. A poor Schottky contact will produce an erroneous and misleading result. It was believed that the surface chemical preparation was an essential step to have a relatively accurate CV reading. Our recent study, however, showed that the surface chemical preparation is not the only factor. The electrical charges on surface are equally important to the CV measurement. This work studied this effect on the Schottky CV measurements in detail. A new method has been developed in which an electrical surface preparation has been used prior to the CV measurement. The new method significantly improved the accuracy and repeatability of CV measurement.

MS-WeP2 A Two-Dimensional Modeling Study of Pattern Dependent Etching@footnote 1@, ***B. Lay**, M.J. Kushner,* University of Illinois, Urbana

Pattern dependent etching has become an increasingly important problem as feature sizes have decreased. It has been observed that a large exposed region on a die in close proximity to fine features tend to decrease the etch rates of the small features. In order to have process-independent uniform etching, the cause of this phenomenon must be determined. Previous studies have shown that gas phase processes alone, particularly at low pressures (< 10-20 mTorr), are unable to explain these observations. In this paper, the results of a numerical study of pattern dependent etching will be presented. A 2-dimensional computer model has been developed which addresses current flow through both the solid wafer material and the plasma. The Plasma-Solid-Simulator (PSS) solves Poisson's equation coupled with the continuity equations for electrons and ions in the plasma, and current density in the bulk, on a triangular mesh. The equations are linearized and implicitly integrated using Newton's method. The PSS calculates the conduction and displacement currents flowing through a partially exposed wafer during the etching process and relates them to etching characteristics. Parametric results from the PSS will be discussed as a function of plasma power and pattern layout. The observed increase in electric fields surrounding the unmasked portions of the wafer may lead to additional electron heating. @FootnoteText@ @footnote 1@This work was supported by SRC, AFOSR/DARPA, Applied Materials and LAM Research

MS-WeP3 Plasma Etch-Back Coupled to Chemical Mechanical Polishing for Sub 0.18 µm Shallow Trench Isolation Technology, ***A. Schiltz**,* France Telecom, CNET-CNS, France*; L. Palatini,* ESPEO - Orleans University, France*; M. Paoli, M. Rivoire, A. Prola,* France Telecom, CNET-CNS, FRANCE

This paper presents a new etch-back planarization technique with counter-masking to pre-planarize Shallow Trench Isolation substrates before Chemical Mechanical Polishing (CMP). A pre-planarization step is necessary since CMP alone cannot provide effective planarization for sub 0.18 technology due to dishing effect . The pre-planarization step uses the principle of Two Layer Planarization (TLP)@footnote 1@ technique which consists in spin-coating a first photoresist layer, using a counter-mask for the lithographic step, flowing and curing the resist blocks in STI topographies, spin-coating a second photoresist layer to planarize the residual topography and transferring the final flat surface into the substrate using plasma etch-back. In difference with previous techniques, we used a special mask with oversizing and exclusion of all STI critical dimensions smaller than 1.55 µm, the zones with the smaller STI dimensions being masked using a special narrow lines grid. Such a masking strategy avoids any misalignment problem, the resized first photoresist blocks are reflowed in STI topographies, leading to an easy planarization by the second resist layer. Additionally, the lithographic step is a non-critical step using conventional i-line resist. The final surface is transferred into the oxide substrate using (Ar/CF4/ O2) gas mixture in a LAM 4520 plasma etching equipment. To allow simultaneous etching of resist and oxide, various gas mixtures of Ar/x/O2 or Ar/x/y/O2 were tested, with x and y being chosen among following fluorine gas : CF4 - SF6 - C4F8 - CHF3. The (Ar/CF4/O2) gas mixture was observed to fulfill the etch back requirements with better performance. Equality of etch rate in resist and in oxide can be adjusted by the O2/CF4 gas ratio. A design of experiment (DOE) was used to determine the optimum conditions of plasma transfer of the planarized profile into the substrate. No ARDE (aspect ratio dependent etching) was observed, but loading effect was observed. Equality of etch rate in resist and in oxide during profile etch back transfer depends on oxide/resist surface ratio and therefore on the STI mask density. Then, equality of etch rate can be adjusted by the O2/CF4 gas ratio. Finally, the pre-planarized wafer is polished by CMP, resulting in an effectively planarized topography with residual topography smaller than 50 nm. The technique is a non-critical lithographic technique scaleable for technologies below 0.18 µm. @FootnoteText@ @footnote 1@ A. Schiltz and M. Pons, J. of the Electrochem. Soc., Vol. 133, 1, 178 (1986)

MS-WeP4 Composition of Si/Ge Films in Structures, ***S. Soukane**, T.S. Cale,* Rensselaer Polytechnic Institute*; C. Werner, A. Kersch,* Siemens, Germany*; M. Bloomfield,* Rensselaer Polytechnic Institute

In order to achieve optimum performance in SiGe base bipolar technology, the film composition must be carefully controlled.@footnote 1@ A detailed surface reaction mechanism for the chemical vapor deposition of SiGe on Si(100), using mixtures of hydrogen, dichlorosilane, hydrogen chloride and germane (H2, SiH2Cl2, HCl, GeH4) is discussed in this paper. The kinetic model involves a set of twelve reactions with several intermediate surface species, and includes both deposition and etching.@footnote 2@ Two reactions describe the migration of adsorbed chlorine and adsorbed hydrogen between silicon and germanium sites. Deposition simulations over device topographies are used to test the proposed kinetic model. Deposited film profiles, concentrations of each surface species, and composition (Si/Ge ratio) as a function of position in the simulated films, are predicted using the proposed chemical model in EVOLVE.@footnote 3@ We compare simulation results with available experimental data. @FootnoteText@ @footnote 1@1SiGeBase Bipolar Technology with 74 GHz fmax and 11 ps Gate Delay, T. F. Meister, H. Schafer, M. Franosch, W. Molzer, K. Aufinger, U. Scheler, C. Walz, M. Stolz , S. Boguth, and J. Bock, IEDM 95, IEEE, p.95-739 @footnote 2@2Kinetic Modeling of SiGe Deposition with SiH2Cl2 and GeH4, M. Hierlemann, C. Werner and H. Schafer, Abstract No. 726 in Electrochem. Soc. Abstracts Vol. 96-1, 1996, p. 900. @footnote 3@3EVOLVE is a low pressure transport and reaction simulator. EVOLVE 5.0b was released in November, 1998 (copyright T. S. Cale, 1989-1998).

MS-WeP5 Development of New Etching Algorithm for Ultra Large Scale Integrated Circuit and Application of ICP(Inductive Coupled Plasma) Etcher, ***Y.-C. Lee**, K.-R. Byun, S.-H. Park, J.-W. Kang, E.-S. Kang, O.-K. Kwon, H.-J. Hwang, T.-W. Kim,* Chung-Ang University, Korea

We proposed proper etching algorithm for ultra-large scale integrated circuit device and simulated etching process using the proposed algorithm in the case of inductive coupled plasma (ICP) source. Proposed algorithm calculates interactions both in plasma source region and in target material region, and uses binary collision approximation (BCA) method when ion impact on target material surface. Proposed algorithm considers the interaction between source ions in sheath region (from Quartz region to substrate region). After the collision between target and ion, reflected ion collides next projectile ion or sputtered atoms. In ICP etching, because the main mechanism is sputtering, both SiO2 and Si can be etched. Therefore, to obtain etching profiles, mask thickness and mask composition must be considered. Since we consider both SiO2 etching and Si etching, it is possible to predict the thickness of SiO2 for etching of ULSI. In this work, selectivity of Si and SiO2 is more than 50. The distribution of ions is calculated by Monte Carlo method and analytic model (plasma density 1012/cm3, pressures 1âˆ¼20mTorr), and the energy (ion flux corresponding to Maxwellian velocity distribution) increases by potential difference in sheath region. Projectile ion moves in time step, has direction and energy. When ion collides targets or ions, direction and energy is changed by impact parameter from binary collision approximation method. Proposed algorithm is efficient for computer calculation and easy to apply other cases. Results of etching simulation using proposed algorithm agree to results of SEM. In conclusion, in the case of ICP type reactor, proposed algorithm is appropriated to obtain etching profiles for ULSI process.

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