

Manufacturing Science and Technology Group Room 611 - Session MS-TuA

Interconnect and Integration

Moderator: S. Shankar, Intel, Inc.

2:00pm **MS-TuA1 CD Control Optimization Methodology on Shallow Trench Isolation Substrate for Sub-0.25 μ m Technology Gate Patterning**, M.H. Fan, H. Gerung, P. Yelehanka, A. Cheng, M.S. Zhou, C. Chi, Chartered Semiconductor Manufacturing Ltd., Singapore; C.H. Tan, J. Xie, Institute of Microelectronics, Singapore

The impact of post-Shallow Trench Isolation (STI) Chemical Mechanical Polishing (CMP) on gate critical dimension (CD) control for submicron technology had been studied. The response of the gate CD depends upon STI process scheme whether it is recess (STI lower than active) or elevated (STI higher than active). Two subjects had been studied: first, CD uniformity as the function of STI step height with active and secondly, CD uniformity as the function of the size of the active area. The topology step height and active size affect the resist coating and organic BARC thickness uniformity. BARC thickness uniformity affects the substrate reflectivity, which leads to variation in the effective exposure dose. This dose variation leads to CD swing across the wafer and resulting in non-uniform CD. We used AFM surface scan to study the topographical variations caused by CMP process on different active area size. A new simulation technique using topographical swing curves and CD error contour plot was applied in this work to optimize BARC and resist thickness. Prolith/2 from FINLE was used for process simulation and excellent agreement was found between simulation and experimental results. Better CD control can be achieved by avoiding extreme recessed or elevated STI topology.

2:20pm **MS-TuA2 Patterning of Xerogel in High Density Fluorocarbon Plasmas**, T.E.F.M. Standaert, State University of New York at Albany; C. Hedlund, Uppsala University, Sweden; E. Joseph, G.S. Oehrlein, State University of New York at Albany; W.N. Gill, P.C. Wayner, J.L. Plawsky, Rensselaer Polytechnic Institute

The upcoming generations of integrated circuits will employ low dielectric constant (k) materials as interconnect isolation. Compared to conventional oxides, low k materials contribute less to circuit delays. Porous spin-on-glasses (k<2.5), e.g. Xerogel, are of particular interest for high speed devices. We present a detailed study on the patterning of Xerogel films with a porosity varying from 64% to 83%. The films were etched in a high density plasma tool using fluorocarbon gases. This allows for a high etch rate. For example, the etch rates in a CHF₃ discharge of a 78 % porous Xerogel film and a thermal oxide film are 2750 and 400 nm/min, respectively. The high etch rates can only partially be explained by the porosity of the films. Namely, the etch yield (number of atoms removed per ion impact) varies with porosity. For example, the yields in a CHF₃ discharge of a 78% porous Xerogel film and a thermal oxide film are 0.88 and 0.58, respectively. One possible explanation for this difference are residual organic groups present in the Xerogel films. We have also characterized the surface modifications after a partial etch by X-ray Photoelectron Spectroscopy (XPS). Finally, we compare the patterning of the Xerogel films to thermal oxides.

2:40pm **MS-TuA3 Surface Science of Tungsten CMP Removal**, D.J. Stein, D.L. Hetherington, Sandia National Laboratories; J.L. Cecchi, University of New Mexico

Chemical mechanical polishing (CMP) is the predominant method for planarization and metal damascene processing during manufacture of submicron integrated circuits (IC). Tungsten CMP is used to remove excess tungsten after non-selective chemical vapor deposition in contacts and vias. We have investigated possible mechanisms of tungsten removal under typical IC manufacturing conditions. Previous models for tungsten CMP suggested that the dominant removal mechanism was the formation of a blanket oxide which was removed by mechanical abrasion. We used an electrochemical cell that allowed measurements of the tungsten oxidation rate and the removal rate. We found that the oxidation rate was between 0.01 and 0.1 of the tungsten removal rate, indicating that blanket oxidation does not play a significant role in tungsten removal. To elucidate the mechanisms responsible for tungsten removal, we undertook a number of additional investigations, including AFM and TEM imaging, correlations of the polish rate and process temperature dependence with the slurry constituent concentrations, and in-situ measurement of the friction and adhesion

between the slurry colloid and the tungsten surface. We interpret our data with a heuristic model. It is shown that the empirical form of the heuristic model fits all of the data obtained. The mechanism also agrees with the limiting cases that were investigated. This mechanism captures the observed relationship between polish rate, pressure, velocity, and slurry chemistry. B. Kaufman et al., J. Electrochem. Soc. 138, 3460, 1991. Stein et al., J. Electrochem. Soc. 145, 3190, 1998. Stein et al., J. Electrochem. Soc. 146, 376, 1999. submitted to J. Mater. Res. accepted for publication in J. Electrochem. Soc.

3:00pm **MS-TuA4 Yield Improvement Through Multizone Uniformity Control of a CMP Process Utilizing a Pre and Post-Measurement Strategy**, J. Moyne, K. Khan, University of Michigan; J. Colt, J. Chapple-Sokol, R. Nadeau, P. Smith, IBM; T. Parikh, SEMATECH

Achieving good uniformity process control in Chemical Mechanical Polishing (CMP) requires a representative uniformity metric and strong models relating this metric to process tunable inputs. Previous efforts in CMP uniformity control have yielded acceptable results utilizing a Center-to-Edge (CTE) first order non-uniformity metric. Closer analysis of post CMP process non-uniformity, however, reveals significant higher order non-uniformity components such as the center "dimple" and outer "doughnut" regions. These non-uniformity characteristics are due in large part to upstream CVD processing. Utilizing a multi-zone approach to uniformity modeling, a more accurate mathematical model of CMP uniformity has been identified. An optimization function has been developed based on minimizing the removal profile slopes as well as the absolute value of the area under the removal curve. The model and function have been utilized to customize a thickness and uniformity multivariate run-to-run software control solution for the process. The controller is based on the Generic Cell Controller structure, which is a proven enabler for run-to-run control for a number of processes including CMP, vapor phase epitaxy, and etch. The control algorithm is a zero'th order adjustable linear approximation two-stage algorithm with EWMA noise filtering. This algorithm, which supports first order linear and non-linear models, has been demonstrated to be effective in CMP CTE and thickness multivariate control. The control solution has been enhanced to utilize both pre and post CMP process metrology along with process models to suggest process recipe modifications on a run-to-run basis. Results indicate improved control of CMP process non-uniformity qualities of interest. Further, the results quantify the significant benefit of utilizing pre-metrology (feedforward) information in addition to traditional post metrology (feedback) in determining control recipe advices.

3:40pm **MS-TuA6 Modeling, A Tool for Technology Development**, J.L. Garcia-Colevatti, Intel Corporation

Technology CAD, TCAD, is a term that describes a collection of model-based tools and methodologies that are used to assist process technology development, IC manufacturing control and the coupling of process specific behavior to products design. Different levels of model complexity, physics content and accuracy are needed depending on the development stage of a particular technology. The continuous need to understand and solve ever more difficult problems rapidly without escalating costs has forced us to draw and integrate results from multiple disciplines, enabling us to keep up with the relentless pace of silicon technology evolution. This presentation will review the scope of these tools, the infrastructure required for their rapid development and deployment and the benefits that result from their application to the exploration, development and manufacturing of new process technologies.

4:20pm **MS-TuA8 Simulations of TiN Barrier Films Deposited by I-PVD on High Aspect Ratio Features: Macrostructure and Composition**, M. Li, S.K. Dew, M.J. Brett, University of Alberta, Canada; T.J. Smy, Carleton University, Canada

TiN films are extensively used as barrier layers for aluminum, tungsten, as well as copper in modern VLSI metallization processing. However, the properties of TiN are significantly dependent upon the microstructure and composition of the film. Physical vapor deposition is a technology commonly adopted for TiN barrier deposition, but recently the ionized variant, I-PVD, has attracted interest for deep sub-micron processes. In this work, by considering the adsorption and desorption of ionic and neutral nitrogen species, N and N₂, and the reflection within the micro-features, the film growth simulator, GROFILMS, is used to study the film microstructure and composition over high aspect ratio topography in an I-PVD system. The effects of the film deposition conditions such as the total

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titanium flux, fraction of titanium ions, partial pressure of nitrogen, degree of nitrogen dissociation, substrate bias and film deposition temperature are investigated. In particular, the simulations demonstrate that ion impact energy and surface diffusion are two major processes determining the properties of TiN barrier films through control of the film density.

4:40pm MS-TuA9 Investigation of Si and SiO₂ Etch Mechanisms Using an Integrated Surface Kinetics Model, D. Zhang, M.J. Kushner, University of Illinois, Urbana

Computer aided development of new plasma etching processes requires a fully integrated plasma equipment and surface chemistry model to account for the interaction between bulk and surface processes. This is particularly important when different surfaces in the reactor (i.e., wafer, photoresist, walls, window) react differently with plasma generated species. To address these plasma-surface interactions throughout the etch chamber, and their influence on bulk plasma properties, the Surface Kinetics Model (SKM) was developed and integrated into the Hybrid Plasma Equipment Model (HPEM), a 2-D plasma simulation tool. The SKM simulates the surface coverage and reactions of surface residence species using the flux of reactants from the HPEM. Ion energy and passivation layer thickness dependent processes are included. Patterned wafers can be addressed by partitioning the surface sites. The SKM was used to investigate the surface reaction mechanism for the fluorocarbon etching of SiO₂. The model includes formation of a passivation layer by CF_x radicals, its etching by F atoms and its sputtering by ions. The SiO₂ etch process is represented by 3 (or more) steps, which starts with formation of a CF_x-SiO₂ complex which, with ion-energy activation, desorbs CO_x or COF_x products which diffuse back through the passivation. The remaining =SiF_x surface site is successively passivated by F atoms diffusing through the passivation, until ion activation desorbs the SiF_x. Results will be discussed for C₂F₆ etching of SiO₂ in inductively coupled, rf biased reactors as a function of ICP and bias power, demonstrating the dependence of etch rates and selectivity on passivation layer thickness. This work was supported by SRC and LAM Research.

5:00pm MS-TuA10 Design of a Dual Frequency PECVD Reactor for Advanced Integrated Circuits Processing, S. Raoux, M. Mudholkar, W.N. Taylor, M.A. Fodor, J. Huang, D. Silvetti, K. Fairbairn, Applied Materials

A capacitively-coupled PECVD reactor was designed using a high-temperature AlN ceramic heater with an embedded RF electrode. The first electrode (at the wafer) is biased at low frequency (350kHz) to control ion bombardment during film growth. The second RF electrode (or showerhead) is biased at 13.56MHz and has conical holes providing a (soft) hollow cathode effect for intense molecule dissociation and ionization efficiency. In this paper, we present advances in Si₃N₄ film deposition using a dual frequency RF plasma and SiH₄, NH₃ and N₂ as precursor gases. We investigate the relation between ion energy and dual frequency plasma impedance, and correlate plasma potential with the film density and etch integrity. A SPICE (Simulation Program with Integrated Circuits Emphasis) model of the plasma reactor was determined. The model is compared to experimental data, and it is shown that the film stress is correlated to the phase angle (I/V) of the low frequency bias and to the heater electrode capacitance. We will present applications of this reactor for deposition of low-temperature (400C) Inter-Metal-Dielectric films and High Temperature processes (550C) for Pre-Metal-Dielectric films.

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