Tuesday Afternoon, October 26, 1999

Flat Panel Displays Topical Conference
Room 604 - Session FP+OE+EM-TuA

Thin Film Transistor Materials and Devices

Moderator: G.N. Parsons, North Carolina State University

2:00pm **FP+OE+EM-TuA1 Nanoprobing Electrical Transport in Organic Semiconductors*, C.D. Frisbie,*** University of Minnesota **INVITED**

Commercial interest in mechanically flexible plastic electronics is the key motivator behind efforts to fabricate transistors, light-emitting diodes, and lasers from organic thin films. Continued development depends on increasing comprehension of factors affecting charge carrier mobility. In particular, the importance of film microstructure on transport in organic films has been recognized, but is currently not well understood. In this talk, I will describe experiments designed to address microstructural effects on conductivity in polycrystalline organic films. Our approach is to probe transport in individual grains, or even small collections of grains, which we characterize by atomic force microscopy (AFM). Experiments have focussed on crystalline grains of the molecular semiconductor sexithiophene (6T). Isolated grains of 6T are grown by vacuum sublimation onto SiO2/Si substrates. The crystals range from 1-6 molecular layers (2-14 nm) in thickness with diameters on the order of a micron. In one approach, these thin crystals are contacted with source and drain electrodes fabricated by electron-beam lithography; heavily doped Si underneath the SiO2 serves as a gate electrode. The resulting transistor structures are used to probe field effect conductance and carrier mobility as a function of temperature (5-300K) and the number of discrete molecular layers in the crystals. The second experiment uses a conducting AFM probe as a positionable electrical contact to grains contacted by a fixed electrode at the other end. This configuration allows variation of the tip-electrode separation, yielding the single grain resistivity and an estimation of the organic-metal contact resistance. Resistances associated with defects, e.g., a single grain boundary between adjacent crystals, may also be measured. In both types of experiments, the conjunction of AFM imaging with transport measurements is critical to correlating transport properties with specific microstructures.

2:40pm **FP+OE+EM-TuA3 Photolithographically Defined Pentacene Thin Film Transistors on Flexible Plastic Substrates*, D.J. Gundlach,*** *C.D. Sheraw, H. Klauk, J.A. Nichols, J-R. Huang, T.N. Jackson,* The Pennsylvania State University

We report photolithographically-defined pentacene thin film transistors (TFTs) on flexible plastic substrates with performance similar to hydrogenated amorphous silicon (a-Si:H) devices. Organic TFTs fabricated on flexible plastic substrates are of interest for mechanically rugged, low-cost broad-area electronic applications. Pentacene TFTs with performance similar to a-Si:H TFTs have been reported,@footnote 1@ however, such devices are typically fabricated on oxidized silicon or glass substrates. Since photolithographic processing of organic semiconducting materials is problematic, such devices, including more recent devices on polymeric substrates,@footnote 2@ typically use source and drain contacts deposited through a shadow-mask after the organic active layer deposition. We have fabricated photolithographically-defined pentacene TFTs on polyethylene naphthalate (PEN) and polyimide (PI) films. For ease of processing, the films were mounted to silicon wafers using a pressure sensitive silicone adhesive and pre-shrunk by heating to 150°C for 1 hour in vacuum. A 30 nm thick Ni gate electrode, 160 nm thick SiO@sub 2@ gate dielectric, and 80 nm thick Pd source/drain contacts were deposited by ion-beam sputter deposition. The TFTs were completed by thermally evaporating pentacene onto substrates heated to 60°C. All deposited layers were photolithographically-defined using a two-layer resist lift-off process. Field-effect mobility larger than 0.3 cm@super 2@/V-s was extracted for TFTs on both PI and PEN film, current on/off ratio was greater than 10@super 5@, and subthreshold slope was less than 1.5 V/decade, all obtained using drain-to-source and gate-to-source biases of -30 volts or less. @FootnoteText@ @footnote 1@ Y-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Electron Device Lett., vol. 18, pp. 606-608, 1997. @footnote 2@ C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, Science, vol. 283, pp. 822-824, 1999.

3:00pm **FP+OE+EM-TuA4 Reduced Process Complexity Organic Thin Film Transistors*, H. Klauk,*** *D.J. Gundlach, M. Bonse, T.N. Jackson,* The Pennsylvania State University

The performance of organic thin film transistors (TFTs) has improved dramatically over the past few years and recently, pentacene TFTs with carrier mobility of 0.6 cm@super 2@/V-s were demonstrated on glass substrates.@footnote 1@ The TFT device structure used in this earlier work required 4 material depositions and 4 lithography steps: one each for the gate, the gate dielectric, the source/drain contacts, and the pentacene active layer. Patterning of the pentacene layer is important to avoid leakage since pentacene TFTs often have large positive threshold voltage. We report here a simplified device structure for depletion-mode pentacene TFTs. Only 3 material depositions and 3 lithography steps are required and the same metal deposition is used for the gate electrode and the source/drain contacts. Gate-to-source and gate-to-drain overlap are not required, since the pentacene layer is normally conducting, thus allowing a drain current to flow at zero gate bias; devices are turned off by applying a positive gate bias. Palladium was used for the gate and source/drain metal, and low-temperature (80°C) ion-beam sputtered SiO@sub 2@ was used as the gate dielectric; both layers were patterned by lift-off. To pattern the pentacene active layer, a double-layer photoresist technique was used to create a reentrant profile over which the pentacene was deposited by evaporation. Upon deposition, the pentacene layer breaks over the resist profile, leaving isolated TFT areas. At a relatively low drain-source voltage of -20 V, devices have carrier mobility as large as 0.3 cm@super 2@/V-s, on/off current ratio near 10@super 5@, subthreshold slope as low as 0.9 V/decade, and threshold voltage between +10 V and +17 V. @FootnoteText@ @footnote 1@ Hagen Klauk, David J. Gundlach, Jonathan A. Nichols, and Thomas N. Jackson, "Pentacene Organic Thin-Film Transistors for Circuit and Display Applications," IEEE Transactions on Electron Devices, vol. 46, no. 6, June 1999.

3:20pm **FP+OE+EM-TuA5 Soft Lithographic Patterning and Low Temperature Film Deposition: Methods to Fabricate Amorphous Silicon Thin Film Transistors at Low Temperature*, H.-C. Jin,*** *J.R. Abelson, M.K. Erhardt, R.G. Nuzzo,* University of Illinois, Urbana

We fabricate amorphous silicon thin film transistors on glass substrates at low temperature (125@super o@C) using "soft" lithographic patterning in place of traditional photolithography. In soft lithography, polymer templates are formed on the film by holding an elastomer block containing the desired pattern in contact with the substrate, flowing an uncured precursor into the micro-channels of the pattern, then curing the polymer. Such templates replace photoresist for all etch and deposition steps, and have been successfully used for the fabrication of multilayer device architectures with micron-scale feature resolution. It appears possible to pattern sub-micron features, as well as large area and curved substrates. In this talk, we show the patterning methodology, preliminary results for TFT devices on planar and curved substrates, and discuss future prospects.

3:40pm **FP+OE+EM-TuA6 Low Damage Etching Utilizing Activated Hydrogen Beam for ITO Transparent Electrode in Flat Panel Display*, T. Miyata,*** *T. Minami, M. Ishii,* Kanazawa Institute of Technology, Japan

Recently, low damage dry etching has become necessary for transparent electrode patterning in flat panel display fabrication. This paper introduces a newly developed low damage and high rate etching technique utilizing an activated hydrogen beam to etch Sn-doped indium oxide (ITO) transparent conducting films. The etching was carried out using an apparatus consisting of an etching chamber and an activating chamber interconnected with a 0.9 mm-diameter orifice; the pressure in the activating chamber was higher than that in the etching chamber. The hydrogen gas introduced into the activating chamber was first activated by applying microwave power and then introduced through the orifice into the etching chamber. The etching was accomplished by the activated hydrogen beam acting on patterned photoresist coated ITO films placed on a sample holder. The etching rate was strongly dependent on conditions such as sample temperature, orifice-sample separation and pressure in the etching chamber. It should be noted that the ITO film was only etched at sample temperatures above 160@super o@C and the etching rate increased as the sample temperature was increased. A maximum etching rate above 50 nm/min was obtained at a sample temperature of 220@super o@C. These results suggest that ITO films are mainly etched by chemical reactions.

4:20pm **FP+OE+EM-TuA8 Excimer Laser Processing for a-Si and poly-Si Thin Film Transistors for Imager Applications**, ***J.P. Lu***, *P. Mei, R.T. Fulks, J. Rahn, J. Ho, Y. Wang, J.B. Boyce, R.A. Street,* Xerox Palo Alto Research Center **INVITED**

Pulsed Excimer-Laser Annealing (ELA) has become an important technology to produce high performance Thin Film Transistors (TFTs) for large area electronics. The application of these advanced TFTs in flat pannel displays@footnote 1@ and flat panel imagers for two-dimensional X-ray imaging have attracted much interest. TFTs made from laser crystallized poly-Si thin films with mobility higher than 100 cm@super 2@/Vs can be consistently achieved and are well suited for the integrated driver circuits. Recently, leakage currents as low as 2fA/µm at 5V for these poly-Si TFTs have been achieved and enable one to consider making flat panel imagers using a full poly-Si process. Laser doping@footnote 2@ or dopant activation is another important application of the ELA process. Using a laser doping process, we have fabricated a-Si TFTs with self-aligned poly-Si source/drain contacts. These new devices have reduced source/drain parasitic capacitance and their channel length can be easily scaled down without stringent lithography requirements. Excellent DC performance, such as low leakage current (0.02fA/µm), sharp turn on (0.44V/decade) and high mobility of a-Si TFTs are preserved. In addition, good AC performance of these self-aligned a-Si TFTs has been demonstrated in four phase dynamic shift registers operating at 250kHz. In this talk, these two areas will be reviewed along with a report on the current status in developing poly-Si TFTs and self-aligned a-Si TFTs using ELA process for flat panel imager applications. @FootnoteText@ @footnote 1@ J. G. Blake, M. C. King, J. D. Stevens III, and R. Young, Solid State Technology, p151, May 1997. @footnote 2@ P. Mei, G. B. Anderson, J. B. Boyce, D. K. Fork, and R. Lujan, Thin Film Transistor Technologies III, Electrochemical Soc. Proc., PV 96-23, p51 (1997).

5:00pm **FP+OE+EM-TuA10 Solid-phase Crystallization of Hydrogenated Amorphous Silicon-Germanium Alloy Films**, ***O.H. Roh***, *I.H. Yun, J.-K. Lee,* Chonbuk National University, Korea

We have investigated the solid-phase crystallization of hydrogenated amorphous silicon-germanium alloy (a-Si@sub 1-x@Ge@sub x@:H) films by using electron spin resonance (ESR) and x-ray diffraction measurements. The films were deposited on Corning 1737 glass in a plasma-enhanced chemical vapor deposition system using SiH@sub 4@ and GeH@sub 4@ gases. The substrate temperature was 200°C and the r.f. power was 3W. The films were then annealed to be crystallized at 600°C in a N@sub 2@ atmosphere. The total spin density first increased with annealing time due to hydrogen evolution, and then rapidly decreased as the film was crystallized. The Ge dangling bond spin density increased faster with annealing time than the Si dangling bond spin density. However, it was observed that the H evolution from Si-H bond and Ge-H bond was strongly affected by the Ge composition of the films.

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