Electronic Materials and Processing Division
Room 608 - Session EM1-ThA

Chemical Mechanical Planarization

Moderator: Y.J. Chabal, Bell Laboratories, Lucent Technologies

2:00pm **EM1-ThA1 Surface Chemical Changes during Cu Chemical Mechanical Polishing**, ***S. Seal***, *D. Tamboli, V. Desai,* University of Central Florida*; S. Joshi, G. Shinn,* Texas Instruments

The current USLI manufacturing technology is continued to be driven towards miniaturization of integrated circuits (< 0.1 micron feature size). As the devices and circuits have increased their complexity, densification and miniaturization, CMP has emerged to be the key technology for feature sizes of 0.35 micron and below to meet the stringent requirements for next generation microelectronic devices. Cu CMP@footnote 1@ is the "technology" for producing submicron Cu line in multilevel metallization structures and satisfies the global planarization, the most important issue for lithography. During Cu CMP, oxidation, dissolution and surface modification take place due to slurry/wafer interaction. While electrochemical measurements are performed to determine corrosion rate, degree of surface passivation and dissolution, detailed surface chemistry is carried out using XPS and AES techniques. Special emphasis is focused on monitoring changes in copper oxide/hydroxides stoichiometry. The surface chemical changes are correlated to Cu polishing rate and slurry chemistry @FootnoteText@ @footnote 1@J. M. Steigerwald, S. P. Muraraka and R. J. Gutmann, Chemical Mechanical planarization of Microelectronic Materials, John Wiley and Sons, Inc. 1997.

2:20pm **EM1-ThA2 Effect of Thin Film Properties on Copper Removal in CMP**, ***D. Tamboli***, *S. Seal, V. Desai,* University of Central Florida*; S. Joshi, G. Shinn,* Texas Instruments

Currently there is a significant efforts directed towards integrating copper interconnect technology into semiconductor device fabrication because of advantages such as lower RC delays and superior electromigration performance with the use of copper. CMP of copper is a relatively new technology. It is also extremely challenging because of low hardness of Cu films (which makes it prone to defects such as scratches, dishing etc.) and its poor electrochemical properties. Performance of Cu-CMP process is greatly dependent on properties of the deposited copper films. In this study, we report the effect of thin film properties on CMP performance of Cu. As deposited Cu films are first characterized using techniques such as XPS, glancing angle XRD (to measure internal stress), AFM (to study grain morphology), nano-indentation and 4-probe sheet resistivity measurement, and electrochemical polarization measurements. These wafers are then polished. CMP performance as measured by removal rates and in-situ dissolution rate measurements is then correlated with the thin film properties of Cu.

2:40pm **EM1-ThA3 Damascene Patterning of Advanced Interconnect Structures**, ***R.J. Gutmann***, Rensselaer Polytechnic Institute **INVITED**

Advanced IC interconnect structures incorporate damascene patterning (in-laid metal) to improve packing density and reduce manufacturing cost. Chemical-Mechanical Planarization (CMP) of copper or aluminum is used to delineate the trenches and/or vias after dielectric etching and metal deposition. The Damascene patterning process is presented, with an emphasis on CMP issues. The role of the metallic liner and the interlevel dielectric (ILD) are highlighted, the effect of alternative CMP consumables (slurries and pads) discussed, and the interaction between the CMP process and post-CMP cleaning in establishing a robust manufacturing capability presented. Examples used to highlight these issues will include dual Damascene patterned copper interconnects with polymer ILDs and tantalum liners and single Damascene patterned copper and aluminum interconnects with oxide ILDs and magnetic liners. The possibility of scaled copper interconnects without conventional conducting liners will be presented.

3:20pm **EM1-ThA5 Tungsten CMP Process Post Tungsten Etch Back Process to Improve the Reliability for Sub-Micron Device Technology**, ***A. Sidhwa***, *H. Minssieux, C. Spinner,* STMicroelectronics, Inc.

In this paper we will discuss the importance of the CMP process used on wafers after the Tungsten Etch Back step. The purpose of the CMP step was to polish of the remaining Tungsten residue from the etch back process along with the Ti/TiN (barrier) layer and stop on the PMD layer. In the back end of the process, metal residues have been a killer defect that can cause significant decrease in the wafer yield. Residue remaining on the underlying surface may cause shorting of the conductive film and create defects that can affect planarity of the top film. Residues seen after tungsten etch back were due to incomplete tungsten etch back process in uneven areas. These residues can impact the metallization, patterning, and etch processes by causing broken metal lines or lines with defects. It is a known fact that during the tungsten etch back process; it is difficult to etch tungsten of the uneven surfaces due to under layer effects. Hence, high defects can be obtained after the WEB (tungsten etch back) step. If the CMP is performed to polish the remaining tungsten residue along with the barrier, most of the defects that were observed by the KLA after WEB step can be completely removed. The number of defects can be reduced drastically after CMP process. A considerable yield improvement due to CMP touch up process can be obtained. In this paper we show a short loop wafer yield map with high defects and compared to the KLA map performed after WEB process, the yield loss on the short loop wafer is directly correlated to the defects observed at the center of the wafer. This paper will show the defects before CMP and defects after CMP touch up step. Also it will discuss the impact on the electrical data and the SWEAT electromigration data due to Tungsten CMP touch up process.

4:20pm **EM1-ThA8 Etching and Cleaning of Silicon Wafers using HF Vapor Process in the Monolayer Etching Regime**, *Y.-P. Han,* ***H.H. Sawin***, Massachusetts Institute of Technology

We have studied the oxide etching mechanisms of a gas phase HF etching process in a condensed (liquid phase) and a non-condensed regime (gas phase). In the condensed regime, the etching rate of oxide is greatly affected by the flow rate of the reactant stream and the total pressure of reactor, which can change the mass transfer rates of both reactants and products. In the non-condensed regime, the oxide can be etched in both multilayer and monolayer adsorption states depending on process conditions. The gas phase mass transfer rate limits the etching rate in the multilayer adsorption regime while surface reactions are the rate limiting step in the monolayer regime. The rate limiting steps for etching have been studied at various conditions by changing the temperature of the reactor, the partial pressure of the reactants and the flow rate. In the monolayer etching regime, the etching kinetics can be described by a Langmuir-Hinshelwood adsorption mechanism with competitive adsorption between HF and water. The monolayer etching regime shows many advantages over other etching regimes. We have observed a smoother etched oxide surface, a low selectivity against TEOS, and uniform etching over entire 4" wafer. The native oxide grown on the silicon wafer is removed within a minute, as confirmed by contact angle measurement and XPS. Additionally, aluminum lines are not etched or corroded in the monolayer regime, which implies this process can be applied to metal layers. Since there is no condensed layer on the wafer and chamber wall, the pumping speed is rapid enough for use in a vacuum cluster tool under a hard vacuum environment. We believe that the monolayer HF vapor etching process is applicable to in situ contact cleaning and in situ polymeric residue removal process on metal layers.

4:40pm **EM1-ThA9 Chlorosilane Treatment of SiO@sub 2@-Covered Si Surfaces for Modification of their Chemical Reactivity in Si CVD**, ***T. Yasuda***, *M. Nishizawa, S. Yamasaki,* Joint Research Center for Atom Technology (JRCAT), Japan

SiO@sub 2@ surfaces are chemically inert against silane molecules. This nature has made SiO@sub 2@ the most preferred mask material for selective CVD of Si, while there are other device processes that require enhanced nucleation of Si on SiO@sub 2@. Thus a technique to control the chemical reactivity of the SiO@sub 2@ surface should be useful in many aspects of device processing. This paper shows that such control is possible by treating the SiO@sub 2@ surface with a proper chlorosilane gas, SiH@sub n@Cl@sub 4-n@. Experiments were carried out using Si(001) wafers covered by an ultrathin SiO@sub 2@ layer formed by plasma or UV-ozone oxidation. Our previous studies showed that this layer acts as a mask in Si CVD using Si@sub 2@H@sub 6@.@footnote 1@ An exposure of the SiO@sub 2@-covered sample to SiCl@sub 4@ at 500 K formed surface-SiCl@sub x@ groups as confirmed by on-line Auger electron spectroscopy. We have found that Si deposition is strongly suppressed on the SiCl@sub 4@-treated SiO@sub 2@ surface under our standard CVD condition (0.05 Pa Si@sub 2@H@sub 6@; 853 K). Density of the Si nuclei is much smaller (~10@super 8@ cm@super -2@) than those observed on the as-oxidized surfaces (~10@super 9@cm@super -2@). This indicates that the surface-SiCl@sub x@ group is inert against Si@sub 2@H@sub 6@. In contrast, Si nucleation is greatly enhanced by a SiH@sub 2@Cl@sub 2@ treatment, the nucleation density reaching 6 x 10@super 10@ cm@super -2@. We

have also found that electron-beam irradiation of the chlorosilane-treated surfaces prior to the CVD processing enhances Si nucleation. The minimum electron dose to induce this effect was 10 mC/cm@super 2@. Taking advantage of this effect we have achieved "resistless" selective deposition on the beam-defined parts of the SiO@sub 2@ surface. This study, partly supported by NEDO, was carried out at JRCAT under the joint research agreement between NAIR and ATP. @FootnoteText@ @footnote 1@ T. Yasuda et al., Appl. Phys. Lett. 74, 653 (1999).

5:00pm **EM1-ThA10 The Passivation of Si(100)-2x1 with Alcohols**, ***T. Bitzer***, *A. Lopez,* St. Andrews University, United Kingdom*; N.V. Richardson,* St. Andrews University, United Kingdom, UK

Wet chemical etching is a fundamental process in the production of nano-structures on silicon wafers. It has been found that the addition of alcohols such as iso-propanol to an aqueous KOH etchant moderates the etching process, which improves the surface finish.@footnote 1@ In this study, we simulated the conditions at the silicon wafer/etchant interface inside ultra high vacuum (UHV) by the passivation of the Si(100)-2x1 with alcohols ((CH@sub 3@)@sub n@CH@sub 3-n@OH, n=1,2,3), such as ethanol, iso-propanol and tert-butyl alcohol, and post-exposure to H@sub 2@O. Vibrational spectra, taken with high resolution electron energy loss spectroscopy (HREELS), show that alcohol species chemisorb via a deprotonation of the OH group. The alkoxy species are bonded to the silicon dimer through a Si-O-C linkage. We found that post-exposure to H@sub 2@O does not result in a removal of alkoxy species but rather in an oxidation of the Si-Si bond of the silicon dimer. After prolonged H@sub 2@O exposure, 2x1 diffraction spots are absent in LEED. The findings will be compared with the reactivity of alcohols on hydroxylated Si(100)-2x1.@footnote 2@ @FootnoteText@ @footnote 1@ S. A. Campbell, K. Cooper, L. Dixon, R. Earwaker, S. N. Port and D. J. Schiffrin, J. of Micromech. and Microeng. 5, 209 (1995) @footnote 2@ T. Bitzer, N. V. Richardson and D. J. Schiffrin, Surf. Sci. Lett. 382, L686 (1997).

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