Electronic Materials and Processing Division
Room 608 - Session EM-WeA

Novel Materials and Devices for Computation and Communication

Moderator: H.A. Atwater, California Institute of Technology

2:00pm **EM-WeA1 Materials and Devices for Optical Communication***, K.J. Vahala,* California Institute of Technology **INVITED**

The performance requirements of commercial lightwave communication systems have systematically exceeded expectations for over a decade. Driven by explosive Internet growth, current commercial trunk-line systems are approaching 1 Terabit/sec of aggregate bandwidth on a single optical fiber and use as many as 80 channels (wavelengths). Optical switching, channel add/drop, wavelength conversion, and other functions are needed in these systems and there is a premium on functions that can be all-optical and preferably fiber based. This talk will over view some of the materials and devices that are now finding use in telecom systems. It will also suggest some performance issues in these systems that are material-related.

2:40pm **EM-WeA3 Nano-Crystal and Quantum-Dot Memories: Implications Small Dimensions, Quantum Confinement and Interface States***, **S. Tiwari**,* Cornell University*; A. Kumar, J.J. Welser,* IBM T.J. Watson Research Center **INVITED**

For field-effect devices, one of the most significant effects of scaling of critical dimensions to the 1--10~nm range is a reduction in collective effects whose reproducibility has been so profitably applied over the last many decades. Examples of such collective phenomena are the number of electrons flowing through the channel, the number of electrons transferred during a CMOS switching event, and the number of dopants used to control the threshold voltage. A larger number of electrons flowing in the channel leads to smaller fluctuations in the current, a larger number of electrons transferred during switching leads to smaller fluctuations in the switching voltage levels, and a larger number of dopants leads to smaller fluctuations in the threshold voltage. The scaling of device dimensions has been driven by higher function and lower cost gained from an increase of device density and performance, a lowering of power density, and mixing of logic and memory technologies. Logic and memory have to co-exist at such small dimensions, and the various forms of memory have to be capable of providing a range of performance from high speed to low power and non-volatility. Nano-crystal and Quantum-Dot memories, examples of flash memories, are small dimension structures that utilize quantum-dot(s) between the gate and the channel of a field-effect transistor to store electron(s), which screen the mobile charge in the channel and thus induce a change in the threshold-voltage or conductivity. These quantum-dots are transmissively coupled to the channel and isolated from the gate. Their reduced dimension and confinement brings forth two important features that are absent in the conventional silicon field-effect transistors: a reduced density of states, restricting the states available for electrons and holes to tunnel, and the Coulomb blockade effect, arising from a larger electrostatic energy associated with placing a charged particle onto a smaller capacitance.

3:20pm **EM-WeA5 Fabrication and Manipulation of Silicon Nanocrystals for Non-Volatile Memory Applications@footnote 1@***, **L.D. Bell**,* Jet Propulsion Laboratory, California Institute of Technology*; E.A. Boer, D.H. Santamore, H.A. Atwater, K.J. Vahala, M.L. Ostraat, R.C. Flagan,* California Institute of Technology **INVITED**

Silicon-based devices continue to decrease in size, and fast, low-power devices sensitive to small numbers of electrons are now feasible. MOS structures with large arrays of Si nanocrystals can form the basis for a floating gate memory that is extremely fast, reliable and non-volatile, and in which charge stored may be as little as one electron per nanocrystal. To date, these devices have exhibited a distribution of charge transit times during writing of nanocrystal ensembles, which limits speed and array uniformity. This could be related to nanocrystal interface states, a dispersion in oxide thicknesses, or nanocrystal size variations. To address these limitations, we have developed an aerosol vapor synthesis/deposition technique for Si nanocrystals with active size classification, enabling narrow distributions of nanocrystal size. One goal of these experiments was to use atomic force microscopy (AFM) to perform nanocrystal manipulation and charging on a single-particle basis. Si nanocrystal structures (such as lines and arrows) have been formed by contact mode AFM and subsequently imaged in non-contact mode without additional particle motion. Single nanocrystal charging by a conducting AFM tip has been observed, detected as an apparent height change due to electrostatic force followed by a slow relaxation as the charge dissipates. To investigate the charge trapping characteristics of nanocrystals in device structures, we have made samples of Si nanocrystals embedded in thermally grown SiO@sub 2@ films by ion implantation of Si, followed by annealing at 1100°C. A conducting AFM tip has been used to inject charge into these samples and to observe the charge dissipation as a function of time. The relative contributions of surface defects, bulk irradiation damage and nanocrystals to the resultant trapped charge have been studied and have been shown to be dependent on processing parameters. @FootnoteText@ @footnote 1@Research supported by JPL DRDF and NASA.

4:00pm **EM-WeA7 Architectonics of Defect-Tolerant Molecular Circuitry***, **R.S. Williams**,* Hewlett-Packard Labs **INVITED**

Economic and physics considerations indicate that the exponential scaling of CMOS will saturate in a decade. However, the power efficiency of present electronics technology is at least a billion times smaller than the non-reversible thermodynamic limit.@footnote 1@ Thus, there is a huge incentive to invent new devices with nanometer dimensions. In addition, vast quantities of these devices must be manufactured and interconnected inexpensively. Two lines of complementary research are necessary for future nanoelectronics: the development of quantum-state switches and the design of circuit elements that can be assembled into complex systems via chemical processes. A recent proposal for the construction of molecular-electronic computers involves the explicit incorporation of defect tolerance, which is the capability to operate perfectly even in the presence of manufacturing mistakes, into the architecture of the circuit.@footnote 2@ An example of such a defect-tolerant computer was built and tested at Hewlett-Packard Laboratories with standard Si technology. The Teramac experimental supercomputer replaced logic with memory whenever possible and relied on sophisticated computer algorithms to identify and route around defects. This architecture is currently being explored as the basis for molecular-electronic memory, logic, signal routing and multiplexing/demultiplexing in a joint research project involving HP Labs (the Quantum Structures Research Initiative), UCLA (the research groups of Profs. J. R. Heath, F. Stoddart and V. Roychowdhury) and UC Berkeley (Prof. Paul McEuen). Experimental results on prototype devices and circuits will be presented and discussed. @FootnoteText@ @footnote 1@ R. P. Feynman, Feynman Lectures on Computation, edited by A. J. G. Hey and R. W. Allen (Addison-Wesley, 1996). @footnote 2@ J. R. Heath, P. J. Kuekes, G. S. Snider and R. S. Williams, "A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology," Science 280 (1998) 1716.

4:40pm **EM-WeA9 Carbon Nanotubes - a New Class of 1D Conductors***, **P.L. McEuen**,* University of California, Berkeley and LBNL **INVITED**

Carbon nanotubes are single graphene sheets rolled into nanometer diameter cylinders. They are a new class of one-dimensional conductors that can be either metallic or semiconducting, depending upon their structural details. In this talk, I will discuss experiments by our group to probe the electrical properties of these fascinating systems. Wires are attached to individual tubes and a nearby gate is used to control the charge per unit length of the tube. If the tube is semiconducting, the resulting device operates as the world's smallest transistor. For a metallic tube, behavior characteristic of a correlated electron state known as a Luttinger liquid is found. Short tubes act like one-dimensional boxes for electrons whose quantized energy levels and spin states can be probed. Crossed metal and semiconducting tubes act as ultra-small Schottky diodes. As these experiments show, nanotubes offer an unprecedented opportunity to explore the physics and technology of the one-dimensional electron gas.

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